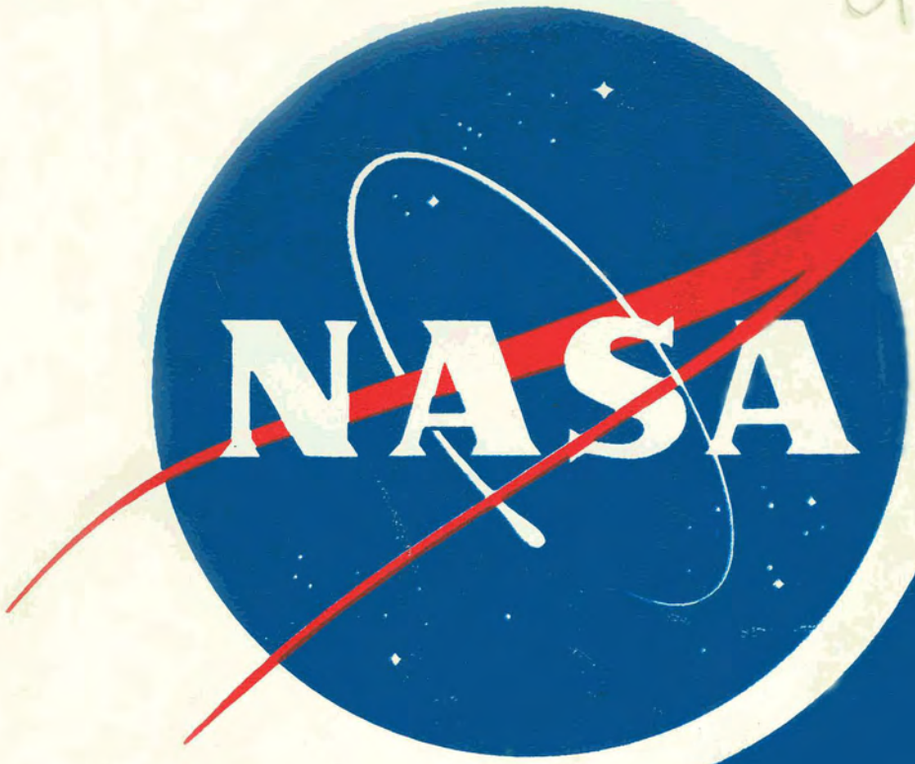

ASTRIONICS SYSTEM HANDBOOK

SATURN LAUNCH VEHICLES

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

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But should be
entered in VII.1 + XI.7

ASTRIONICS SYSTEM HANDBOOK

SATURN LAUNCH VEHICLES

1 August 1965

PREFACE

This second revised edition of the Astrionics System Handbook has been developed under the direction and overall supervision of Dr. Rudolf Decher of the Astrionics Systems Engineering Office.

This description of the Saturn Astrionics System has been generated by personnel of the Astrionics Laboratory, the staff of the Astrionics Systems Engineering Office, and by personnel of the International Business Machines Corporation working under Contract NAS8-14000.

The handbook will be updated and expanded as it becomes necessary due to changes or refinements in the system concept and hardware. Sections not contained in the first release of this document will be made available within three months.

Ludie G. Richard

LUDIE G. RICHARD
Chief,
Systems Engineering Office
Astrionics Laboratory

LIST OF EFFECTIVE PAGES

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2-i	Original
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3.4-10 Blank	Original
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3.5-1 thru 3.5-4	Original
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4.1-1	Original
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5.4-9 thru 5.4-18	Original
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5.6-1 thru 5.6-3	Original
5.6-4 Blank	Original
5.6-5	Original
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5.6-7	Original
5.6-8 Blank	Original
5.7-1 thru 5.7-4	Original
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5.8-4 Blank	Original
6-i	Original
6-ii Blank	Original
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6.2-1 thru 6.2-13	Original
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6.2-17	Original
6.2-18	Original
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6.3-9	Original
6.3-10 Blank	Original
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6.5-1 thru 6.5-3	Original
6.5-4 Blank	Original
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7-ii Blank	Original
7.1-1 thru 7.1-4	Original
7.2-1	Original
7.2-2	Original
7.3-1 thru 7.3-5	Original
7.3-6 Blank	Original
7.4-1 thru 7.4-3	Original
7.4-4 Blank	Original
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7.5-2 Blank	Original
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8-ii Blank	Original
8.1-1	Original
8.1-2 Blank	Original
8.1-3	Original
8.1-4 Blank	Original
8.1-5	Original
8.1-6 Blank	Original
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8.2-4 Blank	Original
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8.2-10 Blank	Original
8.2-11	Original
8.2-12 Blank	Original
8.3-1	Original
8.3-2	Original
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8.4-2 Blank	Original
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8.5-2	Original
9-i	Original
9-ii Blank	Original
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9.2-1 thru 9.2-3	Original
9.2-4 Blank	Original
9.3-1 thru 9.3-5	Original
9.3-6 Blank	Original
10-i	Original
10-ii Blank	Original
11-i	Original
11-ii Blank	Original
II	Original
12-i	Original
12-ii Blank	Original
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13-i	Original
13-ii Blank	Original
13.1-1 thru 13.1-3	Original
13.1-4 Blank	Original
13.1-5	Original
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13.2-1	Original
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14-i	Original
14-ii Blank	Original
14.1-1 thru 14.1-3	Original
14.1-4 Blank	Original
14.2-1 thru 14.2-6	Original
14.3-1 thru 14.3-8	Original
14.4-1 thru 14.4-5	Original
14.4-6 Blank	Original
14.5-1 thru 14.5-4	Original
14.6-1	Original
14.6-2	Original
14.7-1 thru 14.7-7	Original
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14.8-1 thru 14.8-5	Original
14.8-6 Blank	Original
14.9-1 thru 14.9-5	Original
14.9-6 Blank	Original
14.10-1	Original
14.10-2	Original
15-i	Original
15-ii Blank	Original
15.1-1	Original
15.1-2	Original
15.2-1 thru 15.2-3	Original
15.2-4 Blank	Original
15.3-1	Original
15.3-2	Original
15.4-1 thru 15.4-7	Original
15.4-8 Blank	Original
15.4-9 thru 15.4-28	Original
15.5-1 thru 15.5-3	Original
15.5-4 Blank	Original
15.5-5	Original
15.5-6 Blank	Original
15.5-7 thru 15.5-13	Original
15.5-14 Blank	Original
15.5-15	Original
15.5-16	Original
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PART I

FUNCTIONAL DESCRIPTION

CHAPTER 1

INTRODUCTION

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SECTION 1.1

PURPOSE OF DOCUMENT

The intent of this document is to provide a system description of the Astrionics System for the Saturn IB and V Launch Vehicles. It is not intended to go too deeply into any given subject but rather to give an overall picture of the Astrionics System from functional and operational viewpoints. General mission requirements and system capabilities are briefly discussed in Chapter 1, Introduction, to provide a total view of the Astrionics System. The subsequent chapters of Part I present a functional description of the various subsystems and the involved hardware. The operational phases of the Astrionics System, including pre-launch checkout, are discussed in Chapter 11 and indicate how the system will be used during a typical Saturn V Apollo mission. Astrionics hardware which performs several different functions (e. g., Launch Vehicle Digital Computer and Data Adapter) is described in Part II.

The Astrionics System description includes all of the electrical and electronic equipment on board the vehicle. It also includes the launch site electronic support equipment. However, this particular description does not cover the individual stage relay circuitry which controls certain stage functions. It does describe the signal flow through the system to the point of energizing this special circuitry so that an overall understanding of system operation is presented. Likewise, stage propellant utilization systems and internal engine sequencing systems are not covered; since, for the purpose of this description, they are considered a part of the propulsion system.

Since Astrionics Systems of Saturn IB and Saturn V are very similar, this document is devoted primarily to Saturn V. The areas in which the Saturn IB Astrionics System deviates from the Saturn V Astrionics System are listed in Section 1.4. Where applicable, these deviations are specified in the text of that particular chapter.

SECTION 1.2

SATURN LAUNCH VEHICLES

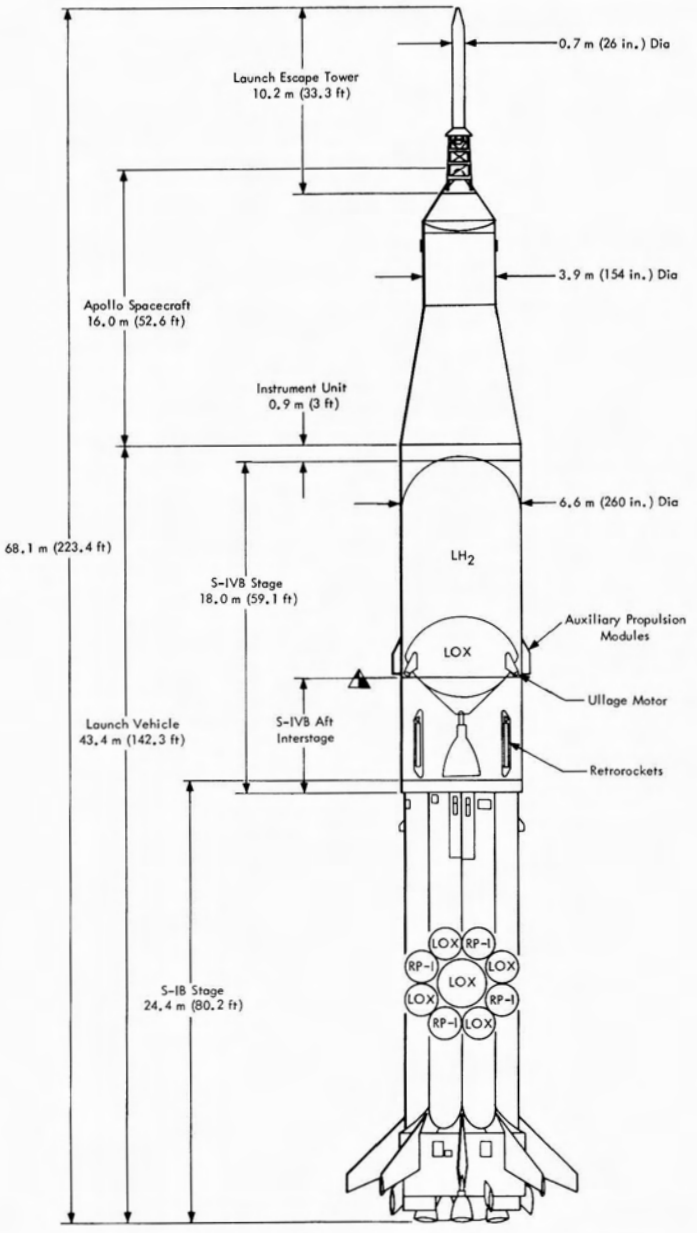
Figures 1.2-1 and 1.2-2 illustrate the Saturn IB Vehicle and Saturn V Vehicle, respectively, and include some characteristic vehicle data. Both vehicles have the same upper stage (the S-IVB Stage) which is propelled by a restartable engine to provide injection into escape trajectory from a parking orbit. The Instrument Unit is mounted on top of the S-IVB Stage and is very similar for Saturn IB and Saturn V.

The primary mission of Saturn IB is to serve as a launch vehicle for the Apollo Spacecraft earth orbital flight tests. These earth orbital flights will simulate certain phases of the lunar landing mission and will provide flight tests for the spacecraft and the S-IVB/IU Stage. Saturn V is the launch vehicle for the actual Apollo lunar landing missions. The typical profile of a lunar landing mission is described in Section 1.3.

The primary mission of the Saturn Vehicles is the successful accomplishment of the Apollo mission. In addition, the Saturn Vehicles are capable of performing other types of missions which can be generally classified as the insertion of heavy payloads into earth orbits and escape trajectories. This may include:

- Transfer between earth orbits
- Rendezvous in earth orbit
- Direct ascent and injection into escape trajectory
- Injection into escape trajectory following extended earth-orbit phases
- Extended missions beyond injection

Saturn Vehicles are numbered consecutively, beginning with 201 for the first Saturn IB Flight Vehicle and 501 for the first Saturn V Flight Vehicle. The first few vehicles of each series are considered as research and development vehicles.



SATURN IB

- Overall Length . . . . . : 68.1m (223.4 ft)

S-IB

- Dry Weight . . . . . : 39,861 kg (87,800 lbs)
- Main Propulsion Engine. : Rocketdyne H-1 (8)
  - Total Nominal Thrust . . : 7,116,000 N (1,600,000 lbs) (sea level)
  - Propellants . . . . . : LOX and RP-1
  - Engine Cant Angle . . . : Inboard (4) 3°
Outboard (4) 6°
  - Gimbal Pattern . . . . . : ± 8° Square Pattern (outboard engines only) (4)
- Retromotors . . . . . : Thiokol TE-29-1B (4) (1)
  - Propellant . . . . . : Solid
  - Arrangement . . . . . : Equally spaced circumferentially on aft interstage.

S-IVB

- Dry Weight . . . . . : 10,805 kg (23,800 lbs)
- Main Propulsion Engine. : Rocketdyne J-2 (1)
  - Total Nominal Thrust . . : 912,250 N (205,000 lbs) (vacuum)
  - Propellants . . . . . : LOX and LH_2
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : ± 7° Square Pattern
- Attitude Control Engines: TAPCO (6)
  - Nominal Thrust (Each) . : 666 N (150 lbs) (vacuum)
  - Propellants . . . . . : Hypergolic (MMH & N_2O_4)
  - Arrangement . . . . . : Two auxiliary propulsion modules containing 3 engines each, located at positions I and III on aft skirt.
- Ullage Motors/Engines . : Thiokol TX-280 (3)
  - Propellant . . . . . : Solid
  - Arrangement . . . . . : Equally spaced circumferentially on aft skirt.

INSTRUMENT UNIT

- Dry Weight . . . . . : 1,884 kg (4,150 lbs)

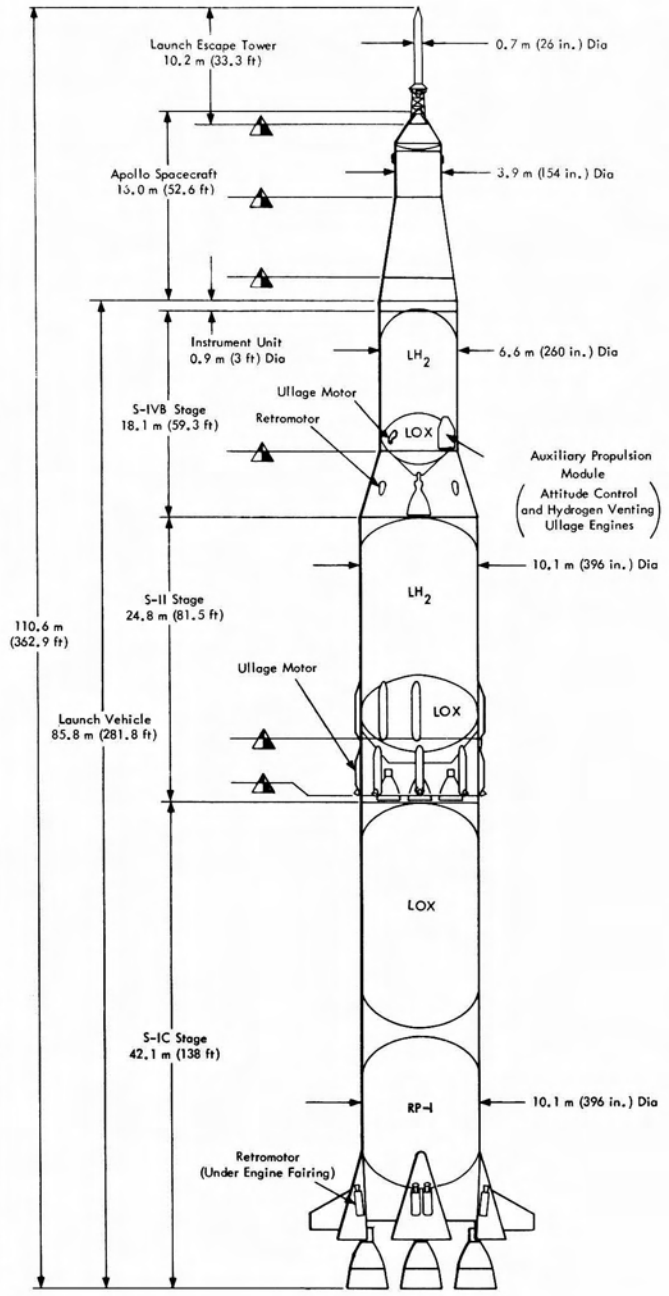
Note:

(1) Retromotors are used for S-IB retrograde acceleration.

▲ Flight Separation

IBM B128

Figure 1.2-1 Saturn IB Launch Vehicle Characteristic Data



SATURN V

- Overall Length . . . . . : 110.6m (362.9 ft)

S-IC

- Dry Weight . . . . . : 136,200 Kg (300,000 lbs)
- Main Propulsion Engines : Rocketdyne F-1 (5)
  - Total Nominal Thrust . . : 33,864,500 N (7,610,000 lbs)
  - Propellants . . . . . : LOX and RP-1
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : ± 5° 9' Square Pattern (Outboard Engines) (4)
- Retromotors . . . . . : 8
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Two in each F-1 engine fairing

S-II

- Dry Weight . . . . . : 37,183 kg (81,900 lbs)
- Mainstage Propellant Capacity . . . . . : 440,380 kg (970,000 lbs)
- Main Propulsion Engines : Rocketdyne J-2 (5)
  - Total Nominal Thrust . . : 4,561,250 N (1,025,000 lbs)
  - Propellants . . . . . : LOX and LH_2
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : ± 7° Square Pattern (Outboard Engines) (4)
- Ullage Motors/Engines . : RS-U-501 (8)
  - Nominal Thrust (Each) . : 101,900 N (22,900 lbs) (vacuum)
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Equally spaced around S-IC/S-II Interstage, in line with S-IC fins and positions I, II, III, & IV.

S-IVB

- Dry Weight . . . . . : 12,440 kg (27,400 lbs)
- Mainstage Propellant Capacity . . . . . : 104,420 kg (230,000 lbs)
- Main Propulsion Engine : Rocketdyne J-2 (1)
  - Total Nominal Thrust . : 912,250 N (205,000 lbs)
  - Propellants . . . . . : LOX and LH_2
  - Engine Cant Angle . . . : None
  - Gimbal Pattern . . . . . : ± 7° Square Pattern
- Attitude Control Engines : TAPCO (6)
  - Nominal Thrust (Each) . : 670 N (150 lbs) (vacuum)
  - Propellants . . . . . : Hypergolic (MMH & N_2O_4)
  - Arrangement . . . . . : Two auxiliary propulsion modules containing 3 engines each, located at positions I and III on aft skirt.
- Ullage Motors/Engines . : Thiokol TX-280 (2)
  - Nominal Thrust (Each) . : 15,560 N (3,500 lbs) (vacuum)
  - Propellant . . . . . : Solid
  - Arrangement . . . . . : Equally spaced circumferentially on aft skirt.
- Hydrogen Venting Ullage Engines . . . . . : Gemini OAMS (2)
  - Nominal Thrust (Each) . : 320 N (72 lbs) (vacuum)
  - Propellants . . . . . : Hypergolic (MMH & N_2O_4)
  - Arrangement . . . . . : One in each of two auxiliary propulsion modules located at positions I and III on aft skirt.
- Retromotors . . . . . : TE-29-1B (4) (1)
  - Propellants . . . . . : Solid
  - Arrangement . . . . . : Positions I, II, III, and IV S-II/S-IVB Interstage.

INSTRUMENT UNIT

- Dry Weight . . . . . : 1,884 kg (4,150 lbs)

Note:

(1) Retromotors are used for S-II retrograde acceleration

▲ Flight Separation

IBM B129

Figure 1.2-2 Saturn V Launch Vehicle Characteristic Data

SECTION 1.3

SATURN V/APOLLO MISSION PROFILE

The mission of the Apollo Project is to land 2 Astronauts on the moon and return the total crew of 3 Astronauts safely to earth.

The overall Apollo Space Vehicle, composed of the Saturn V Launch Vehicle and the Apollo Spacecraft, is shown in Figure 1. 2-2. The Saturn V consists of three propulsion stages and the Instrument Unit. The IU contains the navigation, guidance and control, communication, and power supply equipment common to the main propulsion stages.

The following is a brief description of the Saturn V Launch Vehicle mission only. The profile of the mission is illustrated in Figure 1. 3-1. The S-IC Stage boosts the vehicle through the atmospheric flight phase. Cutoff of the engines is initiated close to fuel depletion and occurs at an altitude of approximately 62 kilometers (34 nautical miles). After separation from the first stage, second stage (S-II) boost follows immediately; engine cutoff is executed as in the first stage. Both stages drop to earth in a ballistic flight path. After separation of the S-II Stage, the S-IVB Stage engine is ignited. The engine is cutoff when the vehicle has achieved the necessary orbital velocity. The vehicle, consisting now of the S-IVB/IU Stage and the Apollo Spacecraft, orbits the earth at an altitude of approximately 200 kilometers (108 nautical miles) for a maximum of 3 orbits. An orbital launch window exists once in each orbit. When the selected orbital launch window occurs, the S-IVB engine is ignited a second time to provide the thrust for injection into the translunar trajectory. The engine is cutoff when the required escape velocity is achieved. In the coast period following injection, the transposition maneuver is performed. In this maneuver, the Service and Command Modules of the spacecraft move away from the Saturn S-IVB/IU Stage, turn around, and dock with the Lunar Excursion Module still attached to the S-IVB/IU Stage to achieve the proper spacecraft configuration for the lunar landing operation. The S-IVB/IU Stage is then separated from the Apollo Spacecraft. The launch vehicle mission ends with the separation from the spacecraft at approximately one hour after injection (maximum time of 2 hours after injection). The spacecraft continues its coast flight toward the moon.

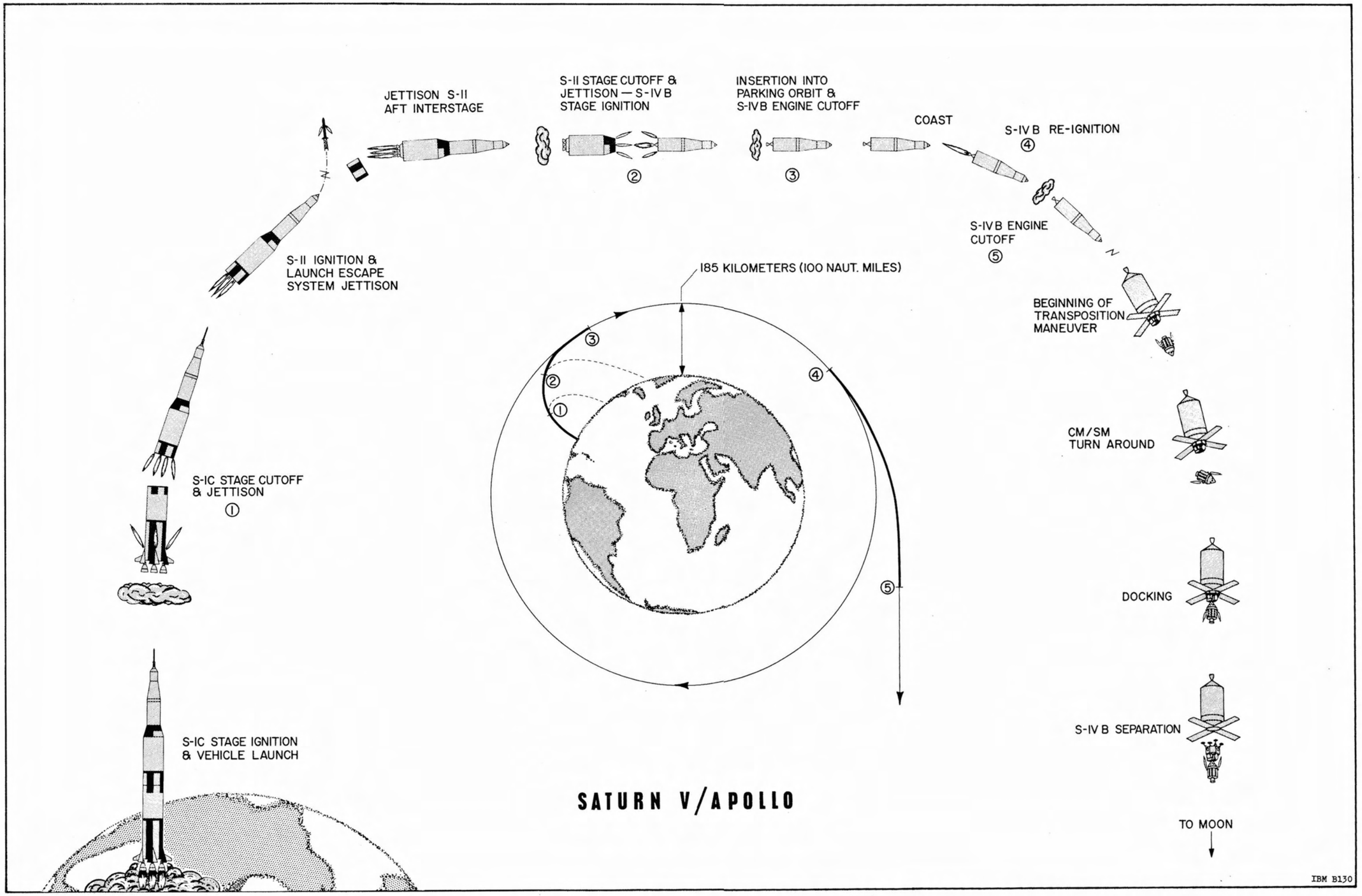


Figure 1.3-1 Saturn V/Apollo Mission Profile

SECTION 1.4

ASTRIONICS SYSTEM

The overall Astrionics Systems of the Saturn IB and V Launch Vehicles are shown in the simplified block diagrams, Figures 1.4-1 and 1.4-2, respectively. The major portion of the Astrionics equipment is located in the IU, which is mounted on top of the S-IVB Stage. During flight, the Astrionics System performs, or is involved in, the following main functions:

- Navigation, guidance, and control of the vehicle
- Measurement of vehicle parameters
- Data transmission between vehicle and ground stations (up and down)
- Tracking of the launch vehicle
- Checkout and monitoring of vehicle functions in orbit
- Detection of emergency situations
- Generation of electrical power for system operation

The operational lifetime of the S-IVB/IU Astrionics System is 4-1/2 hours for Saturn IB and 7 hours for Saturn V. The operational lifetime is limited only by the capacity of the power supply (batteries) and the water supply of the environmental control system which is sufficient to complete the presently defined launch vehicle missions. With increased power and water supply capacity, the operational lifetime of the Astrionics System can be extended for longer duration missions if required.

NAVIGATION, GUIDANCE, AND CONTROL

The Saturn Astrionics System provides navigation, guidance, and control of the vehicle from launch until separation of the S-IVB/IU from the spacecraft. The equipment involved in these functions are the ST-124-M Inertial Platform Assembly, the Launch Vehicle Digital Computer and Launch Vehicle Data Adapter, the Flight Control Computer, the Rate Gyros, and finally the propulsion engine actuators and the auxiliary propulsion system. The Saturn inertial navigation and guidance system can be updated by data transmission from ground stations through the IU command system. The Inertial Platform Assembly carries three integrating accelerometers which measure the thrust acceleration in a space-fixed reference frame. In addition, the platform gimbal angles indicate the attitude of the vehicle in the platform reference frame. The LVDA serves as the input/output device for the LVDC and also performs the necessary data processing.

The LVDC performs computations for navigation, guidance, and control functions. The position and velocity of the vehicle is obtained by combining accelerometer measurements with computed gravitational acceleration. This information is the input to the guidance computations which determine the required thrust vector orientation and engine cutoff time according to the guidance scheme stored in the memory of the LVDC.

Attitude control during powered flight is accomplished through swivelling of propulsion engines by means of hydraulic actuators to obtain the proper thrust vector orientation. The actuator commands are generated in the Flight Control Computer. The Flight Control Computer combines attitude error signals from the LVDA and angular rate signals from Rate Gyros to provide stable attitude control of the vehicle. The attitude error signal is generated in the LVDC by comparing the required thrust vector orientation (from guidance computations) with the actual vehicle attitude (obtained from platform gimbal angles).

During coast flight periods, attitude control is achieved by the auxiliary propulsion system. This system consists of 6 nozzles which are arranged in 2 modules and mounted on the aft end of the S-IVB Stage. The auxiliary propulsion system is also controlled by the Flight Control Computer located in the IU.

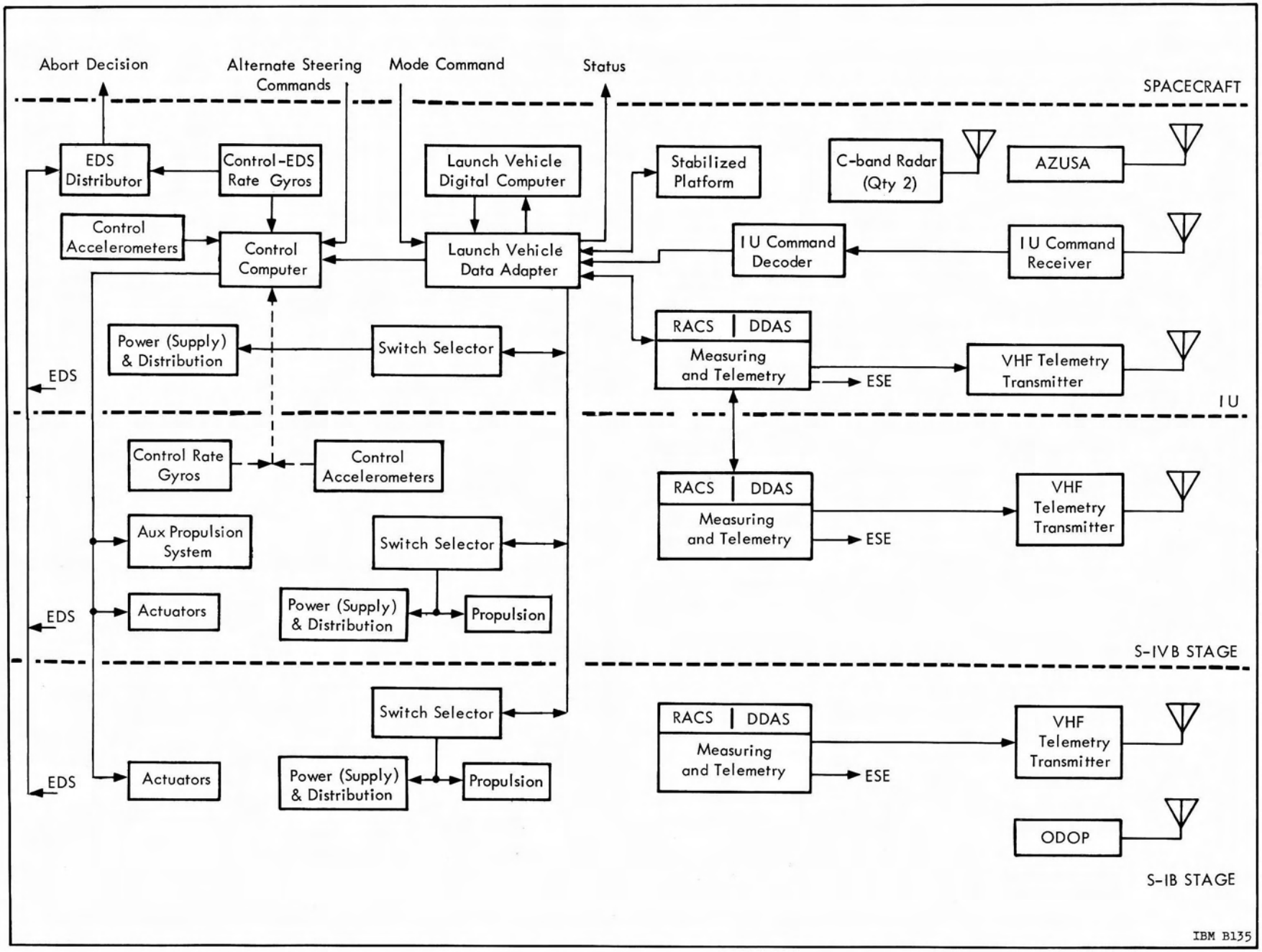


Figure 1.4-1 Saturn IB Astrionics System (Operational Vehicle)

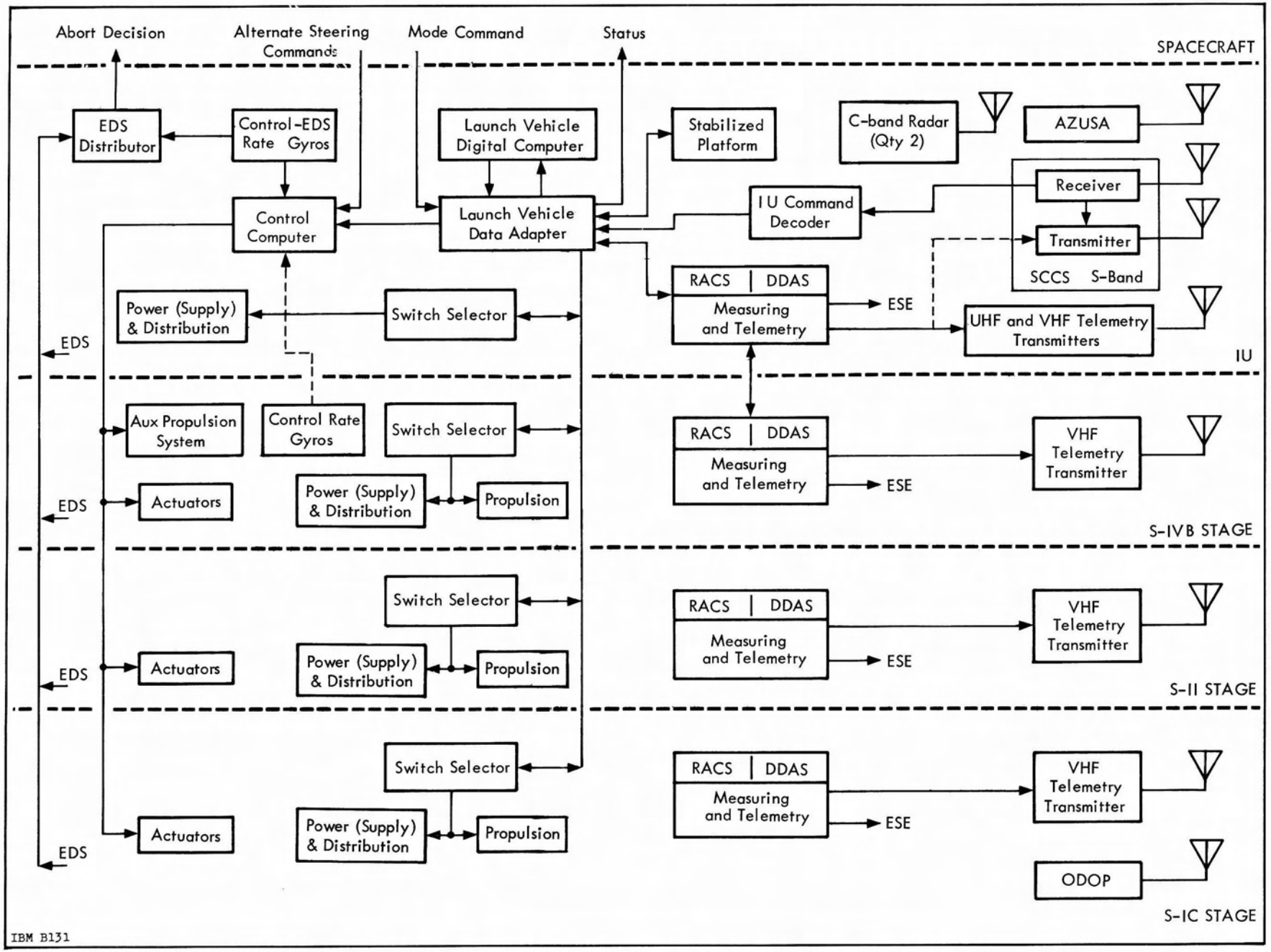


Figure 1.4-2 Saturn V Astrionics System (Operational Vehicle)

Flight sequence control (e.g., vehicle staging, engine ignition and cutoff) is performed by the LVDC. The flight program, stored in the LVDC memory, generates the necessary flight sequence commands which are transmitted through the LVDA and Switch Selector to the proper circuit in the particular vehicle stage.

MEASUREMENTS AND DATA TRANSMISSION

Each vehicle stage is equipped with a complete measuring and telemetry system, including RF transmitter and antennas. For efficient utilization of available bandwidth and to obtain the required accuracy, three different modulation techniques are used in each stage telemetry system. These three are: frequency modulation/frequency modulation, pulse code modulation/frequency modulation, and single sideband/frequency modulation (employed in research and development only).

In Saturn IB vehicles, telemetry data is radiated from the vehicle to ground stations in the VHF band (225-260 MHz). The PCM/FM system of the S-IVB Stage and the IU are interconnected to provide a redundant transmission path and to make S-IVB measurements available to the LVDA. All flight control data is transmitted through the PCM/FM system.

In Saturn V Vehicles, the PCM/FM telemetry data of the S-IVB and IU is transmitted in VHF band (225-260 MHz) and in the UHF band (2200-2300 MHz). The UHF-band transmission is provided primarily for transmission over the longer ranges after the vehicle has left the parking orbit. In addition, the PCM/FM data can be transmitted through the communication and command system transponder. This arrangement provides high reliability through redundancy in transmission path.

The telemetry system of each stage has a separate output via coaxial cable to the electronic support equipment, which is used with the digital data acquisition system for vehicle checkout before launch.

The Instrument Unit command system permits data transmission from ground stations to the IU for insertion into the LVDC.

TRACKING

The Saturn Vehicles carry several tracking transponders. The ODOP Transponder is located in the first stage of Saturn IB and V Launch Vehicles. The Instrument Unit is equipped with two C-band Radar Transponders, an AZUSA Transponder, and the CCS Transponder (S-band tracking).

EMERGENCY DETECTION SYSTEM

The emergency detection system collects special measurements from each stage of the launch vehicle. Based on these measurements, critical states of the vehicle which may require mission abort are detected, and the information is sent to the spacecraft for display and/or initiation of automatic abort.

SPACECRAFT INTERFACE

Several lines cross the IU/spacecraft interface for exchange of signals. Alternate steering commands from the spacecraft navigation and guidance system may be used to control the launch vehicle during S-II and S-IVB powered flight phases. This type of operation is considered as backup in case of a failure of the IU navigation and guidance system. During coast flight, the Astronaut may control the attitude of the vehicle through manually generated commands. In any case, a mode command must be sent first from the spacecraft to the LVDA to perform the necessary switching before the IU Flight Control Computer can accept the steering signals from the spacecraft. To indicate the state of the launch vehicle, certain measurements are sent to the spacecraft and displayed to the Astronaut.

Before launch, automatic checkout of the vehicle system is controlled by the launch computer complex and the electronic support equipment. This system also includes the digital data acquisition system.

Table 1.4-1 indicates the differences in the Saturn IB and Saturn V Astrionics Systems.

Table 1.4-1 Differences Between Saturn IB and Saturn V Astrionics Systems

(To be supplied at a later date)

SECTION 1.5

RELIABILITY CONSIDERATIONS

(To be supplied at a later date)

CHAPTER 2

NAVIGATION AND GUIDANCE

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SECTION 2.1

THE NAVIGATION, GUIDANCE, AND CONTROL SYSTEM

The problem of directing a ballistic missile or space vehicle, to accomplish a given mission, is customarily discussed in terms of three separate functions: navigation, guidance, and control. The boundaries between these 3 areas are to some extent arbitrary and conventional. The 3 terms, navigation, guidance, and control, will be used in this text according to the following definitions:

- Navigation is the determination of position and velocity of the vehicle from measurements made onboard the vehicle.
- Guidance is the computation of maneuvers necessary to achieve the desired end conditions of a trajectory (e.g., an insertion into orbit).
- Control is the execution of the maneuver (determined from the guidance scheme) by controlling the proper hardware.

A block diagram of the overall Saturn V navigation, guidance, and control system is shown in Figure 2.1-1. (This figure is also true for the Saturn IB Vehicle if the S-II Stage Switch Selector and engine actuator blocks are omitted.) The 3-gimbal stabilized platform (ST124-M) provides a space-fixed coordinate reference frame for attitude control and for navigation (acceleration) measurements. Three integrating accelerometers, mounted on the gyro-stabilized inner gimbal of the platform, measure the 3 components of velocity resulting from vehicle propulsion. The accelerometer measurements are sent through the LVDA to the LVDC. In the computer, the accelerometer measurements are combined with the computed gravitational acceleration to obtain velocity and position of the vehicle.

The LVDA is the input/output device for the LVDC. It performs the necessary processing of signals, from different sources, to make these signals acceptable to the computer.

According to the guidance scheme (programmed) into the computer), the maneuver required to achieve the desired end conditions is determined by the LVDC. The instantaneous position and velocity of the vehicle are used as inputs. The result is the required thrust direction (guidance command) and the time of engine cutoff.

Guidance information stored in the LVDC (e.g., position, velocity) can be updated through the IU command system by data transmission from ground stations. The IU command system provides the general capability of changing or inserting information in the LVDC.

Control of the launch vehicle can be divided into attitude control and discrete control functions. For attitude control, the instantaneous attitude of the vehicle is compared with the desired vehicle attitude (computed according to the guidance scheme). This comparison is performed in the LVDC. Attitude correction signals are derived from the difference between the existing attitude angles (gimbal angles) and the desired attitude angles. In the Control Computer these attitude correction signals are combined with signals from control sensors to generate the control command for the engine actuators. The required thrust direction is obtained by swivelling the engines in the propelling stage and thus changing the thrust direction of the vehicle. Since the S-IVB Stage has only 1 engine, an auxiliary propulsion system is used for roll control during powered flight. The auxiliary propulsion system provides complete attitude control during coast flight of the S-IV B/IU Stage.

Commands for flight sequence control are generated in the LVDC according to a stored program. These commands are transferred through the LVDA to the Switch Selector of the corresponding vehicle stage. Examples of flight sequence control are engine ignition, cutoff, and stage separation. The Switch Selector in the addressed stage activates the necessary circuit to perform the commanded function.

Attitude and sequence control of the launch vehicle is described in Chapters 3 and 4, respectively. The stabilized platform, LVDA and LVDC, which are involved in navigation, guidance, and control operations, are described in Chapters 14 and 15.

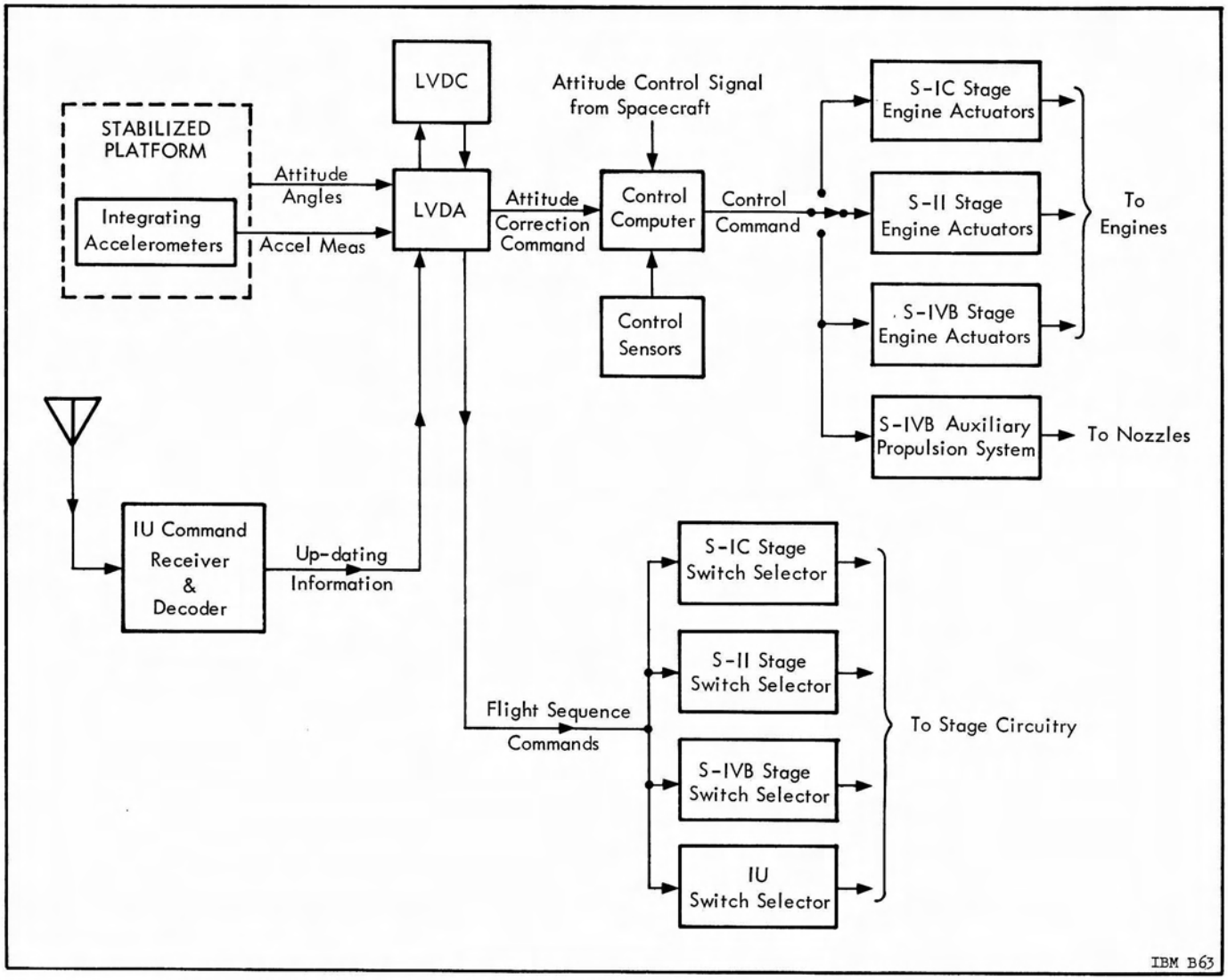


Figure 2.1-1 Block Diagram of Saturn V Navigation, Guidance, and Control System

SECTION 2.2

NAVIGATION

The function of navigation includes the determination of position, velocity, and thrust acceleration of the vehicle from accelerometer measurements. These quantities are required input data for guidance computations.

The velocity of the vehicle is determined by integration of acceleration. Three integrating accelerometers are mounted on the stabilized inner gimbal of the platform. The mutually orthogonal sensitive axes of the 3 accelerometers define the measuring or accelerometer coordinate system ($x_I y_I z_I$). The platform is aligned before launch so that the y_I axis is parallel to the vertical at the launch site and pointing upward, the x_I axis points in the direction of the flight azimuth (A_Z), and the z_I axis completes the right-handed coordinate system. The origin of the $x_I y_I z_I$ coordinate system is at the stabilized platform. For navigation computations, the $x_S y_S z_S$ coordinate system is used. It has its origin at the center of the earth. The $x_I y_I z_I$ system and the $x_S y_S z_S$ system are parallel. Before launch, both systems are earth-fixed (rotate with the earth), but at the moment of platform release (5 seconds before launch), both systems become space-direction fixed (see Figure 2.2-1). The total acceleration $\ddot{r}$ ($\ddot{x}\,\ddot{y}\,\ddot{z}$) of the vehicle in the $x_S y_S z_S$ system is given by:

$$\ddot{r} = \frac{F}{M} + g\,(r) \qquad (2.2\text{-}1)$$

and the velocity is

$$\dot{r} = \int \ddot{r}\, dt = \int \frac{F}{M}\, dt + \int g\,(r)\, dt + \dot{r}_o \qquad (2.2\text{-}2)$$

where F/M is the thrust acceleration, $g\,(r)$ is the gravitational acceleration, and $\dot{r}_o$ is the initial velocity of the vehicle at launch (caused by earth rotation).

During flight, the integrating accelerometers do not respond to gravitational acceleration so their outputs are the velocity components ($\dot{x}_I \dot{y}_I \dot{z}_I$) resulting only from thrust acceleration. To obtain the total velocity of the vehicle, the velocity components ($\dot{x}_g \dot{y}_g \dot{z}_g$) caused by gravity must be added to the accelerometer readings. The gravitational acceleration ($g\,r$), which is acting on the vehicle, is a function of vehicle position and is computed in the gravitation loop. The thrust acceleration (F/M) is computed from the differentiated accelerometer output according to the equation

$$\frac{F}{M} = \sqrt{\left(\frac{d\dot{x}_I}{dt}\right)^2 + \left(\frac{d\dot{y}_I}{dt}\right)^2 + \left(\frac{d\dot{z}_I}{dt}\right)^2} \qquad (2.2\text{-}3)$$

A flow diagram of the navigation computations is shown in Figure 2.2-2. Accelerometer readings, initial velocity, and velocity (vg)(caused by gravitation) are added to obtain the vehicle velocity ($\dot{r}$) in the space-fixed coordinate system ($x_S y_S z_S$). The velocity ($\dot{r}$) is integrated and the initial position is added to yield the vehicle position (r). This position data is used to compute gravitational acceleration and velocity which is then added to the accelerometer readings.

The gravitational acceleration acting on the vehicle is derived from the gravitational potential function of the earth. The expression for the gravitational potential (Ω) of the earth (used for Saturn navigation) is based on the Fisher ellipsoid and is given by:

$$\Omega = \frac{GM_E}{r}\left[1 + J\frac{R_E^2}{3r^2}(1 - 3\sin^2\lambda) + \frac{HR_E^2}{5r^3}(3 - 5\sin^2\lambda)\sin\lambda + \frac{DR_E^4}{35r^4}(3 - 30\sin^2\lambda + 35\sin^4\lambda)\right] \quad (2.2\text{-}4)$$

where

G = universal gravitational constant

M_E = mass of the earth

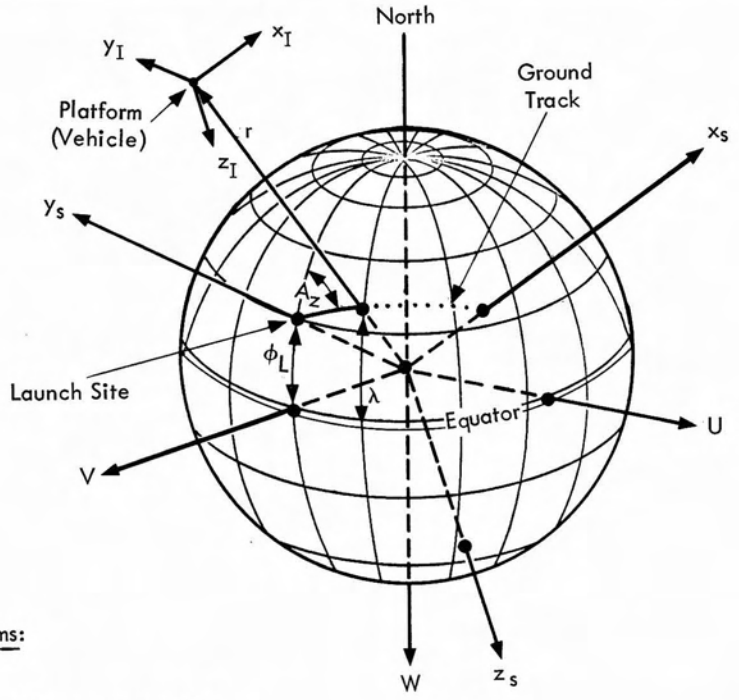
R_E = equatorial radius of the earth

$r = |\bar{r}|$ = distance from earth's center to the vehicle

λ = angle between $\bar{r}$ and the equatorial plane

J, D, H = constants

In order to combine the components of gravitational acceleration with the measured components of thrust acceleration, the gravitational potential is first expressed in a rectangular coordinate system (u v w) which is then "rotated" to be parallel with the accelerometer coordinate system ($x_I y_I z_I$) and the $x_S y_S z_S$ coordinate system.



Coordinate Systems:

UVW: Earth-fixed rectangular system used for gravity computations. Origin at the center of the earth; W axis collinear with the earth's spin axis and pointing south; V axis in the equatorial plane intersecting the equator at the longitude of the launch site; U axis completes right-handed orthogonal system.

$x_S y_S z_S$: Space-fixed rectangular coordinate system for navigation computations. Origin at the earth's center; the Y axis is parallel to the vertical at the launch site at the instant of take-off; the X-Y plane contains the flight plane; the Z axis completes the right-handed system.

Coordinate Systems:

$x_I y_I z_I$: Accelerometer coordinate system, parallel to the $x_S y_S z_S$ system, origin at the vehicle platform.

ϕ_L: Geodetic latitude of the launch site.

A_z: Launch azimuth, measured in clockwise direction from north.

r: Radius vector from the earth's center to the vehicle.

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Figure 2.2-1 Navigation Coordinate Systems

The potential function (2.2-2) is expressed in polar coordinates and may be written in a rectangular earth-fixed coordinate system (u v w) with the origin at the center of the earth and oriented as shown in Figure 2.2-1 by using the relationship:

$$r = \sqrt{u^2 + v^2 + w^2} \qquad (2.2\text{-}5)$$

and $w = -r \sin\lambda$

The components of gravitational acceleration ($u_g v_g w_g$) along the u v w coordinate axis are given by the partial derivatives of (u v w)

$$\ddot{u}_g = \frac{\partial \Omega}{\partial u} = uQ$$

$$\ddot{v}_g = \frac{\partial \Omega}{\partial v} = vQ$$

$$\ddot{w}_g = \frac{\partial \Omega}{\partial w} = wQ + P$$

The expressions for Q and P are given in Table 2.2-1.

The components of gravitational acceleration ($\ddot{u}_g \ddot{v}_g \ddot{w}_g$) must be transformed now into the accelerometer coordinate system ($x_I y_I z_I$)(or $x_S y_S z_S$ system).

The relationship between the u v w system and the $x_S y_S z_S$ system may be expressed in matrix form:

$$\begin{bmatrix} x_S \\ y_S \\ z_S \end{bmatrix} = [A] \begin{bmatrix} u \\ v \\ w \end{bmatrix} \qquad (2.2\text{-}7)$$

or $$\begin{bmatrix} u \\ v \\ w \end{bmatrix} = [A]^T \begin{bmatrix} x_S \\ y_S \\ z_S \end{bmatrix}$$

the rotational transformation matrix $[A]$ is

$$[A] = \begin{bmatrix} \sin A_Z & -\sin\phi_L \cos A_Z & -\cos\phi_L \cos A_Z \\ 0 & \cos\phi_L & -\sin\phi_L \\ \cos A_Z & \sin\phi_L \sin A_Z & \sin A_Z \cos\phi_L \end{bmatrix} \qquad (2.2.8)$$

where ϕ_L is the geodetic latitude of the launch site and A_Z is the launch azimuth measured clockwise from north. The matrix $[A]$ corresponds to two successive rotations of the u v w system: first about the u axis by an angle ϕ_L and second, about the new v axis (now parallel to the y_S axis) by an angle of $(90° - A_Z)$. (See Figure 2.2-1.)

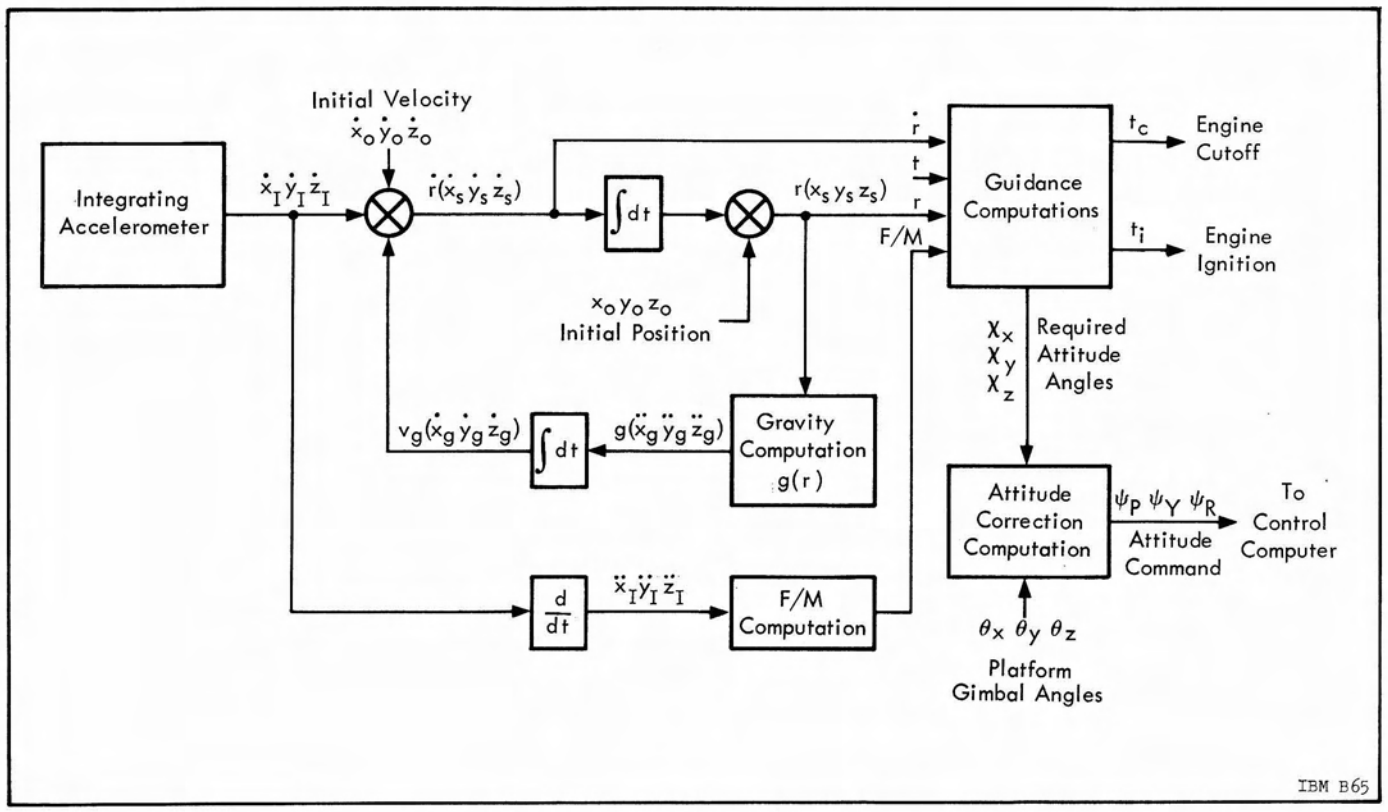

Figure 2.2-2 Navigation Flow Diagram

The gravitational acceleration components in the $x_S y_S z_S$ coordinate system are:

$$\ddot{x}_g = x_S Q - P \cos \phi_L \cos A_Z$$
$$\ddot{y}_g = y_S Q - P \sin \phi_L$$
$$\ddot{z}_g = z_S Q + P \cos \phi_L \sin A_Z \qquad (2.2\text{-}9)$$

The quantities $\sin \phi_L$, $\cos \phi_L$, $\dot{x}_o \dot{y}_o \dot{z}_o$, $x_o y_o z_o$ are constants for a given launch site and are stored in the LVDC. The initial conditions $x_o y_o z_o$ represent the position of the launch site in the $x_S y_S z_S$ coordinate system while $\dot{x}_o \dot{y}_o \dot{z}_o$ is the velocity of the launch site (equals initial vehicle velocity) caused by the rotation of the earth. For certain missions, the launch azimuth A_Z varies with time. In this case, the quantity $\cos A_Z$ stored in the LVDC is continuously updated.

The quantities and equations required for navigational computations are listed in Table 2.2-1.

Navigation is performed continuously throughout the mission. During coast flight periods (in orbit and after translunar injection), no accelerometer readings are obtained. Position and velocity are obtained from gravity computations alone; i.e., by solving the equations of motion.

Actually, a small thrust is applied during coast flight which is the result of the venting of the S-IVB hydrogen tank. Whether the acceleration caused by venting can be measured, considered in computations, or neglected, is under investigation.

Table 2.2-1 Navigation Equations

Velocity:

$$\dot{x}_S = \dot{x}_I + \int \ddot{x}_g \, dt + \dot{x}_o$$
$$\dot{y}_S = \dot{y}_I + \int \ddot{y}_g \, dt + \dot{y}_o$$
$$\dot{z}_S = \dot{z}_I + \int \ddot{z}_g \, dt + \dot{z}_o$$

Position (Displacement)

$$x_S = \int \dot{x}_S \, dt + x_o$$
$$y_S = \int \dot{y}_S \, dt + y_o$$
$$z_S = \int \dot{z}_S \, dt + z_o$$

Thrust Acceleration:

$$\frac{F}{M} = \sqrt{\left(\frac{d\dot{x}_I}{dt}\right)^2 + \left(\frac{d\dot{y}_I}{dt}\right)^2 + \left(\frac{d\dot{z}_I}{dt}\right)^2}$$

$x_o y_o z_o$ and $\dot{x}_o \dot{y}_o \dot{z}_o$ are initial conditions at lift-off

$\dot{x}_I \dot{y}_I \dot{z}_I$: Accelerometer output

Gravitational Acceleration:

$$\ddot{x}_g = x_S Q - P \cos \phi_L \cos A_Z$$
$$\ddot{y}_g = y_S Q - P \sin \phi_L$$
$$\ddot{z}_g = z_S Q + P \cos \phi_L \sin A_Z$$

ϕ_L : Latitude of launch site

A_Z : Launch Azimuth

$$Q = -\frac{GM_E}{r^3}\left[1 + J\left(\frac{R_E}{r}\right)^2\left(1 - \frac{5w^2}{r^2}\right) + H\left(\frac{R_E}{r}\right)^3\left(\frac{w}{r}\right)\left(3 - \frac{7w^2}{r^2}\right) + \frac{D}{7}\left(\frac{R_E}{4}\right)^4\left(3 - 42\frac{w^2}{r^2} + 63\frac{w^4}{r^4}\right)\right]$$

$$P = \frac{GM_E}{r^2}\left(\frac{R_E}{r}\right)^2\left[2J\left(\frac{w}{r}\right) + \frac{H}{5}\left(\frac{R_E}{r}\right)\left(15\frac{w^3}{r^3} - 3\right) + \frac{D}{7}\left(\frac{R_E}{r}\right)^2\left(\frac{w}{r}\right)\left(12 - 28\frac{w^2}{r^2}\right)\right]$$

SECTION 2.3

GUIDANCE

2.3.1 GENERAL CONSIDERATIONS

Guidance of the vehicle in powered flight is accomplished by computing the necessary flight maneuvers to meet the end conditions (e.g., at orbit insertion) determined by mission requirements under given constraints for the trajectory. Computations of flight maneuvers are performed according to the guidance scheme which is represented by a set of guidance equations programmed into the LVDC. Input data to the guidance computations are the state variables of the vehicle position, velocity, acceleration (i.e., the navigation measurements). The result of the guidance computations is the required thrust direction (guidance command) and the time of engine cutoff and re-ignition for the S-IVB Stage. The thrust direction is expressed as three Euler angles $\chi_z\ \chi_x\ \chi_y$ defining the thrust vector orientation in the space-fixed coordinate system $x_S y_S z_S$.

The guidance commands are functions of the state variables and time. They may be expressed in the general form:

$$\chi = f_1\left(\bar{r}\ \dot{\bar{r}}\ \frac{F}{M}\ t\right) = f_1\left(x\,y\,z\ \dot{x}\,\dot{y}\,\dot{z}\ \frac{F}{M}\ t\right) \qquad (2.3\text{-}1)$$

and

$$t_c = f_2\left(\bar{r}\ \dot{\bar{r}}\ \frac{F}{M}\ t\right) \qquad (2.3\text{-}2)$$

where t_c is the time of engine cutoff or re-ignition. The required thrust direction, computed from the guidance scheme, is sent to the attitude control system which controls the vehicle attitude until the command thrust direction is achieved.

PATH ADAPTIVE GUIDANCE

Overall system performance requires that the guidance scheme permits minimum propellant consumption for flight maneuvers and avoids excessive structural loads caused by such maneuvers. The guidance system must correct numerous flight perturbations, such as atmospheric perturbations from wind, unsymmetrical air flow because of vehicle dissymmetry, flight path deviations caused by nonstandard vehicle and engine characteristics and performance (this might even include engine-out cases), control inaccuracies, and emergency situations.

In addition, the required end conditions of the powered flight phase, at insertion into earth orbit and at injection into translunar trajectory, must be met with a high degree of accuracy to avoid additional propellant consuming maneuvers.

To meet this requirement, path adaptive guidance has been developed for Saturn Vehicles. The path adaptive guidance scheme does not constrain the vehicle to a standard trajectory, as with many ballistic missiles. Based on the instantaneous state of the vehicle, the path adaptive guidance scheme computes a new minimum propellant flight path to achieve the mission-determined end conditions. These computations are repeated at intervals of approximately 1 second. Thus, perturbations occurring during flight will be corrected in an optimum way.

Several path adaptive guidance schemes have been developed for Saturn Vehicles. The polynomial guidance scheme and the iterative guidance mode have been successfully used in Saturn I flights. The iterative guidance mode will be used with Saturn IB and V and is described in Paragraph 2.3.2.

During first stage flight (S-IB or S-IC Stage propulsion), the vehicle transverses the dense portion of the atmosphere where high aerodynamic pressure occurs. To avoid excessive structural loads caused by guidance maneuvers, no guidance constraints are applied during this flight phase. An open loop guidance in the form of a time tilt program is used. Path adaptive guidance begins with the ignition of the second stage (S-II Stage for Saturn V and S-IVB Stage for Saturn IB).

TRAJECTORY CONSTRAINTS AND LAUNCH WINDOW

A large number of constraints apply to the trajectory of a launch vehicle. These constraints result from mission rules; environmental conditions such as the atmosphere and location of launch point; operational requirements such as safety restrictions of launch azimuth and tracking requirements; and hardware limitations such as structural load limits and available propulsion means. The dominating and most severe requirement applying to the choice of trajectories is optimal propellant utilization.

A combination of the various constraints generates a limited time period for launch; i. e., a launch window to meet mission requirements. There are 2 types of launch windows for the launch vehicle in the Saturn V/Apollo mission: the ground launch window for ascent into parking orbit and the orbital launch window for translunar injection.

The launch azimuth at the ground and the orientation (inclination and descending node) of the parking orbit are varying with time. A brief explanation of the reasons for time varient launch azimuth, inclination, and descending node seems advisable at this point. At any instant of time a plane can be defined which contains the launch site, the center of the earth, and the moon at the desired time of arrival. In order to maintain this plane it is necessary to vary the launch azimuth on the ground continuously, since the launch site is moving with the rotating earth and the moon is moving. When range safety constraints are introduced, the launch azimuth will be limited to a certain band of values. For launches from Cape Kennedy, the band is approximately 45 to 110 degrees measured east of north and will be encountered twice each day. Within this band, a range of azimuths of 26 degrees will guarantee at least a 2-1/2 hour launch window and normally this variation will be applied to the portion of the band where launch azimuth varies linearly with the time of launch. Of the two daily launch periods, one will generally lead to a shorter coasting arc in orbit than the other. Since the geographic position of the launch site is fixed, it follows that one of the launch periods leads to time of coast in parking orbit such that ignition in orbit occurs within a range close to the launch site—sometimes referred to as the "Atlantic opportunity". The second launch period calls for coasting arcs of greater length—commonly referred to as "Pacific opportunities".

Since launch vehicle payload capability is degraded by powered plane changes, it is assumed that in the nominal case there will be no such maneuvers. If it is desired to go into an orbit with an inclination to the earth's equator (greater than the latitude of the launch site), then it is possible to launch directly into the properly selected launch azimuth. There are other constraints which might be present which affect the launch window problem; e. g., launch during daylight, proper lighting of the launch site, and lighting of the return landing sites. These, however, do not affect the basic geometrical considerations.

2.3.2 ITERATIVE GUIDANCE MODE

The iterative guidance mode was developed to meet the mission flexibility requirement of large space vehicles with minimum propellant consumption. The scheme is based on optimizing techniques using calculus of variations to determine a minimum propellant flight path which satisfies the mission requirements. Experience with hundreds of minimum propellant trajectories for various orbital injection missions has demonstrated that the optimum thrust direction, relative to the local vertical, is very nearly a linear function of time during vacuum flight. Moreover, the size of the angle between the optimum thrust direction and the local horizon is never very large. These observations show a remarkable agreement with the mathematical results obtained from the calculus of variations when a flat earth model having a constant gravitational field is used, and position and velocity constraints are imposed at cutoff. A closed solution can be obtained with this mathematical model and yields an explicit equation for the optimum thrust direction. This equation has the form:

$$\chi_p = \arctan (A + Bt) \qquad (2.3\text{-}3)$$

where χ_p is the optimum thrust direction for minimum propellant consumption and t is the time. Constants A and B are determined by the specified cutoff velocity and position, the initial values of the state variables, the vehicle thrust acceleration, and the engine specific impulse. The comparison of this equation with the results of trajectory studies suggests the use of the approximation:

$$\chi_p = A + Bt \qquad (2.3\text{-}4)$$

A rectangular guidance coordinate system (ξ, η, ζ) (Figure 2. 3-1) is established with the origin

at the center of the earth and with the η axis lying along the vertical which intersects the calculated cutoff position of the vehicle. Simplified equations of motions are derived to approximate the motion over an oblate earth with a realistic gravitational field. These equations of motion are solved during flight to determine the instantaneous range angle to cutoff, the time-to-go to cutoff, and the gravitational effects occurring over the remaining flight time. This information is used to compute values for A and B continuously during flight. In practice, only the value of A need be calculated when computation rates on the order of one or more per second are used (except during the last few seconds before cutoff when both A and B are computed and held constant over the remaining flight time). This is necessary because the equation gives an indeterminate command angle at the cutoff point.

The iterative guidance scheme, which is a quasi-explicit scheme, will be activated after jettison of the launch escape system in the S-II Stage

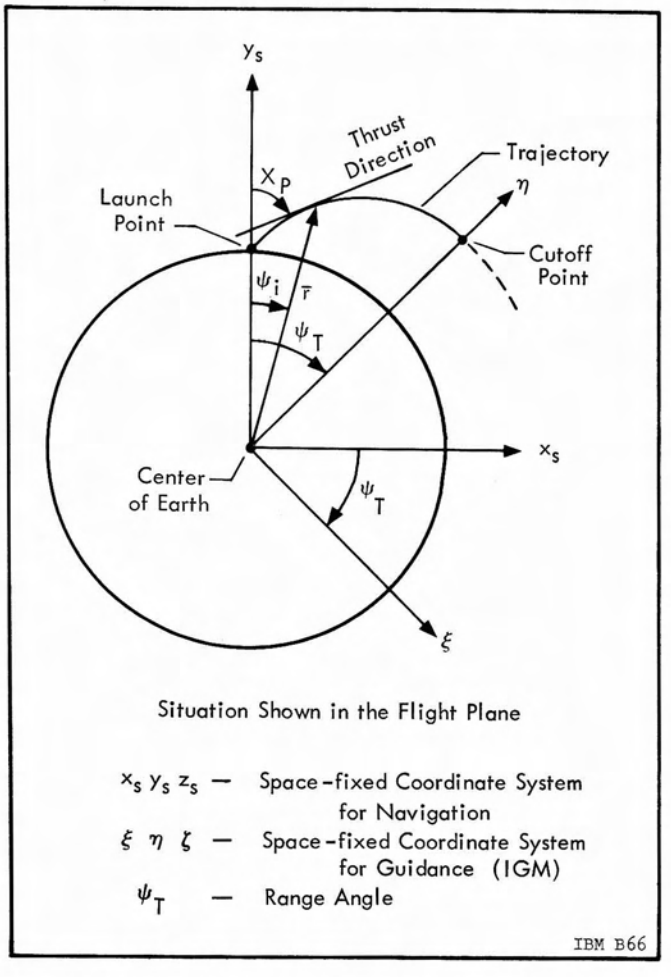

Figure 2.3-1 Coordinate System Used for Iterative Guidance Mode (IGM)

burn period and will continue in operation to insertion into parking orbit by the S-IVB Stage and subsequently to lunar transit injection with the second burn to the S-IVB Stage.

The iterative guidance mode equations for ascent into parking orbit and for powered flight out of orbit are shown in Figures 2.3-2 and 2.3-3, respectively. The guidance scheme generates commands for the pitch and yaw angle of the thrust direction and the cutoff velocity.

The inputs required are divided into 2 categories: (1) vehicle dependent inputs and (2) mission dependent inputs. Figure 2.3-2 shows these inputs required for the ascent-to-orbit phase and the guidance equations—the solution of which generates the steering commands in pitch and yaw. Figure 2.3-3 shows the additional input for flight-out-of-orbit and the additional computation. Although it is seen that the required inputs for the 2 phases differ somewhat, emphasis should be placed on the fact that the guidance equations are identical for both phases; i.e., through built-in logic on the LVDC, the multistage equations necessary for ascent to parking orbit are reduced to single stage equations for flight-out-of-orbit by means of nulling the proper parameters. This task can be accomplished entirely onboard during the time in parking orbit.

Figure 2.3-3 shows that there are 10 inputs dependent on the physical characteristics of the vehicle and 33 inputs dependent on the mission. It should be noted that the inclination of the parking orbit cutoff plane, the decending node, and the launch azimuth are functions of time of launch. During the last few minutes prior to lift-off, these quantities will be computed in the launch ground computer and the results will be put into the LVDA. At the same time, the Stabilized Platform will be turned in the direction of the desired launch azimuth. Figure 2.3-4 shows how the quantities, dependent on time of launch, vary for a typical launch day. Very simple representations of these curves, as a function of time of launch, can be obtained.

When the inputs are considered for the out-of-orbit case, it is convenient that the vehicle characteristics of the S-IVB Stage are already in the LVDC from its first burn into parking orbit. It has been stated previously that the multistage equations are reduced to the single stage by properly storing zeros into the pertinent parameters while the vehicle is in parking orbit. Since this feature is an outgrowth of programmed logic, it is questionable whether these parameters

should be considered bona-fide inputs. As a result, only estimated cutoff time for the second burn of the S-IVB is shown in Figure 2. 3-3 as an input. There are 27 inputs dependent on the mission. Four quantities are time dependent and can be represented by polynominals as shown in Figure 2. 3-3: the aim vector, aim vector magnitude, nominal eccentricity of the outgoing ellipse, and cutoff energy. If the 2-body problem is considered such that Keplerian mechanics holds, the aim vector might be defined as close to the earth-moon line (a line which is between the center of the earth and the center of the moon). Its direction is, of course, time variant since the earth and moon are moving relative to each other. The actual aim vectors are taken from fully optimized trajectories which attain a specified periselenum, flight time, and a specified inclination to the lunar equatorial plane. In the nominal case, the flight plane is chosen such that no powered plane changes are required. If parking orbit perturbations occur, experience has shown that rotating the cutoff plane about the aim vector results in significant payload gains. The cutoff plane is defined by the aim vector and perigee vector as shown in Figure 2. 3-3. Energy input constrains flight time and therefore determines the semi-major axis of the outgoing ellipse. The magnitude of the aim vector determines the true anomaly of the aim vector. In short, with the elliptical parameters M, semi-major axis a, and eccentricity e, the shape of the outgoing ellipse is defined. The perigee vector $\underline{S}$ determines the orientation of the ellipse, and the perigee vector and aim vector determine the plane. Since the iterative guidance equations predict range-to-cutoff updated at discrete intervals, the true anomaly of the cutoff point can be computed and hence the cutoff parameters η_T, V_T, and θ_T which feed into the iterative scheme. It must be emphasized that these quantities change under perturbations such that the S-IVB cuts off possibly at a different point on the ellipse for a thrust perturbation for example, in order to maintain the desired conditions at the moon. The ignition criterion shown here is that ignition will occur when the orbiting vehicle is a fixed angle from the aim vector. The evaluation will begin upon injection into orbit and tests for the number of changes of sign will be made until the correct number is attained. If for some reason (e.g., there is not enough time to perform all checkout procedures before the time to ignite out of the first orbit) it is necessary to go out of the second orbit, the same type of representations of aim vector, energy, and eccentricity can be read into the onboard computer and it is even conceivable that the same coefficients may be used. Open questions still exist as to whether to update the energy such that the moon is reached at a fixed time of arrival—for example, alter the energy such that the resulting time of flight is reduced by the additional time in parking orbit—or to execute a plane change and fly the same amount of time as in the case of going out of the first orbit.

Examination of the loop shown in Figure 2.3-5 between vehicle tracking and telemetry of the LVDC and the stabilized platform, along with transmission of data in real time to the IMCC, the various possibilities of updating information to the computer, of overriding commands such as the ignition equation, and of performing an alternate mission can be seen. In the case of abort (e.g., failure somewhere in the S-II to the nominal mission), no change in input is required. The solution of time-to-go and other parameters in the iterative scheme settle out quite rapidly (after 2 or 3 cycles). This statement also holds for changes in desired terminal conditions which might be built into the computer. Neither the accuracy nor the near optimality of the scheme is degraded.

Figure 2. 3-6 shows a typical relative time sequence of events: when the vehicle data is supplied, when the mission is defined, when the launch day is given, and when the inputs are loaded into the launch computer to be transmitted to the LVDC. It would be assumed that one representation of the time-varying quantities would be made available over an entire month which contained a potential launch date. If 1 month before scheduled launch, a launch date in a different month is selected, approximately 1 week would be required to obtain new representations of launch azimuth, inclination, descending node, aim vector, eccentricity, and energy.

In summary, the effort has been directed towards generality of guidance equations with a minimum amount of input — both for the nominal mission and for abort and alternate missions. Since a minimum amount of "tampering" with the main program in the LVDC is necessary, efficiency is at a high level, and checkout is greatly simplified. A great deal of consideration was given to the question: Is it better to have one set of guidance equations with the extraneous computation of the quantities which are nulled for a special case, or to have separate equations for the ascent-into-orbit and the flight-out-of-orbit? Close coordination with personnel who would actually be involved with the flight program on the LVDC resolved the answer. Extraneous computation, with the minimum amount of change to the flight program, is more desirable. The time required for programming a computer from one flight to the next is reduced by this method. In fact, theoretically it is

INPUTS FOR ASCENT

Vehicle Dependent Inputs (9)

- T_1 = estimated first stage burning time
- T_2 = estimated second stage burning time
- T_c = coast time between second and third stages
- $V_{ex_1} = g_o I_{sp_1}$
- $V_{ex_2} = g_o I_{sp_2}$
- $V_{ex_3} = g_o I_{sp_3}$
- τ_2 = nominal $m_2/\dot{m}_2$
- τ_3 = nominal $m_3/\dot{m}_3$
- T^1 = estimated third stage burning time to parking orbit

Mission Dependent Inputs (7)

- η_T = radius at cutoff
- V_T = velocity at cutoff
- θ_T = path angle at cutoff
- K_6 = mission constant
- i = inclination of cutoff plane
- Θ = descending node of cutoff plane
- A_Z = launch azimuth

MATRIX TO TRANSFORM FROM PLATFORM COORDINATES TO GUIDANCE COORDINATES

$$[A] = \begin{bmatrix} \sin A_Z & 0 & \cos A_Z \\ 0 & 1 & 0 \\ -\cos A_Z & 0 & \sin A_Z \end{bmatrix}$$

$$[B] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi_o & \sin\phi_o \\ 0 & -\sin\phi_o & \cos\phi_o \end{bmatrix}$$

$$[C] = \begin{bmatrix} \cos\Theta & -\sin\Theta & 0 \\ \sin\Theta & \cos\Theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$[D] = \begin{bmatrix} \cos i & 0 & \sin i \\ 0 & 1 & 0 \\ -\sin i & 0 & \cos i \end{bmatrix}$$

$$[G] = [D]\ [C]\ [B]\ [A]$$

TERMINAL RANGE ANGLE CALCULATION IN ORBIT PLANE

$$L_2 = \ln[\tau_2/(\tau_2 - T_2)]$$
$$J_2 = V_{ex_2}(\tau_2 L_2 - T_2)$$
$$S_2 = J_2 - T_2 V_{ex_2} L_2$$
$$Q_2 = \tfrac{1}{2} V_{ex_2} T_2^2 + \tau_2 S_2$$
$$\tau_1 = V_{ex_1}/(F/M)$$
$$L_1 = \ln[\tau_1/(\tau_1 - T_1)]$$
$$J_1 = V_{ex_1}(\tau_1 L_1 - T_1)$$
$$S_1 = J_1 - T_1 V_{ex_1} L_1$$
$$Q_1 = \tfrac{1}{2} V_{ex_1} T_1^2 + \tau_1 S_1$$
$$L^* = V_{ex_1} L_1 + V_{ex_2} L_2$$
$$\delta_1 = -S_1 - J_2 + L^*(T_2 + T_c)$$
$$T_{1C} = T_1 + T_2 + T_C$$
$$L' = \ln[\tau_3/(\tau_3 - T')]$$
$$J' = V_{ex_3}(\tau_3 L' - T')$$
$$T^* = T' + T_{1C}$$
$$A' = L^* + V_{ex_3} L'$$
$$\delta_2 = VT^* - J' + A'T' - K_6(\tau_3 - T')(A' + V - V_T)L'$$
$$\begin{bmatrix} x_{FP} \\ y_{FP} \\ z_{FP} \end{bmatrix} = [G] \begin{bmatrix} x \\ y \\ z \end{bmatrix}$$
$$\phi_T = \arctan(x_{FP}/y_{FP}) + \frac{1}{\eta_T}(\delta_1 + \delta_2)$$

$\dot{\eta}_T = V_T \sin\theta_T$ velocity along η axis

$\dot{\xi}_T = V_T \cos\theta_T$ velocity along ξ axis

POSITION, VELOCITY, F/m & μ FROM NAVIGATION

x, y, z, ẋ, ẏ, ż, F/m, μ

COORDINATE ROTATIONS

$$\ddot{\eta}_{gT} = -\mu/\eta_T^2$$
$$[\phi_T] = \begin{bmatrix} \cos\phi_T & -\sin\phi_T & 0 \\ \sin\phi_T & \cos\phi_T & 0 \\ 0 & 0 & 1 \end{bmatrix}$$
$$[K] = [\phi_T][G]$$
$$\begin{bmatrix} \xi \\ \eta \\ \zeta \end{bmatrix} = [K] \begin{bmatrix} x \\ y \\ z \end{bmatrix}, \quad \begin{bmatrix} \dot{\xi} \\ \dot{\eta} \\ \dot{\zeta} \end{bmatrix} = [K] \begin{bmatrix} \dot{x} \\ \dot{y} \\ \dot{z} \end{bmatrix}$$
$$\begin{bmatrix} \ddot{\xi}_g \\ \ddot{\eta}_g \\ \ddot{\zeta}_g \end{bmatrix} = \frac{1}{2}\left[\begin{bmatrix} 0 \\ \ddot{\eta}_{gT} \\ 0 \end{bmatrix} + [K] \begin{bmatrix} g_1 \\ g_2 \\ g_3 \end{bmatrix} \right]$$

TIME TO CUTOFF CALCULATION

$$\Delta\dot{\xi}^* = \dot{\xi}_T - \dot{\xi} - \ddot{\xi}_g T^*$$
$$\Delta\dot{\eta}^* = \dot{\eta}_T - \dot{\eta} - \ddot{\eta}_g T^*$$
$$\Delta\dot{\zeta}^* = -\dot{\zeta} - \ddot{\zeta}_g T^*$$
$$G = \frac{1}{2}\left[\frac{(\Delta\dot{\xi}^*)^2 + (\Delta\dot{\eta}^*)^2 + (\Delta\dot{\zeta}^*)^2}{A'} - A' \right]$$
$$\Delta T = G(\tau_3 - T')/V_{ex_3}$$
$$T_3 = T' + \Delta T$$
$$T^* = T^* + \Delta T$$

PITCH AND YAW ANGLE CALCULATIONS

$$M = \cos\tilde{\chi}_y + K_3 \sin\tilde{\chi}_y$$
$$N = K_4 \sin\tilde{\chi}_y$$
$$A_p = MA_y - NB_y$$
$$P_1 = -\tfrac{1}{2} T_1^2 V_{ex_1} + \tau_1 J_1$$
$$P_2 = -\tfrac{1}{2} T_2^2 V_{ex_2} + J_2(\tau_2 + 2T_1)$$
$$P_3 = -\tfrac{1}{2} T_3^2 V_{ex_3} + J_3(\tau_3 + 2T_{1C})$$
$$B_p = MB_y - N(T_1^2 V_{ex_2} L_2 + T_{1C}^2 V_{ex_3} L_3 + P_1 + P_2 + P_3)$$
$$E_p = \eta - \eta_T + \dot{\eta} T^* + \tfrac{1}{2}\ddot{\eta}_g T^{*2} - (MC' - ND')\sin\tilde{\chi}_p$$
$$C_p = (MC' - ND')\cos\tilde{\chi}_p$$
$$Q' = \tfrac{1}{2} T_3^2 V_{ex_3} + \tau_3 S_3$$
$$U_1 = \tfrac{1}{6} T_1^3 V_{ex_1} + \tau_1 Q_1$$
$$U_2 = \tfrac{1}{6} T_2^3 V_{ex_2} + Q_2(\tau_2 + 2T_1)$$
$$U_3 = \tfrac{1}{6} T_3^3 V_{ex_3} + Q'(\tau_3 + 2T_{1C})$$
$$D_p = \{MD' - N[U_1 + U_2 + U_3 + T_1^2 S_2 + T_{1C}^2 S_3 - (T_3 + T_C)(P_1 + P_2 + T_1^2 V_{ex_2} L_2) - P_1 T_2]\}\cos\tilde{\chi}_p$$
$$K_1 = B_p E_p/(A_p D_p - B_p C_p)$$
$$\chi_p' = \tilde{\chi}_p - K_1$$

$$\Delta\dot{\xi} = \Delta\dot{\xi}^* - \ddot{\xi}_g \Delta T$$
$$\Delta\dot{\eta} = \Delta\dot{\eta}^* - \ddot{\eta}_g \Delta T$$
$$\Delta\dot{\zeta} = \Delta\dot{\zeta}^* - \ddot{\zeta}_g \Delta T$$
$$\tilde{\chi}_y = \arctan[\Delta\dot{\zeta}/(\Delta\dot{\xi}^2 + \Delta\dot{\eta}^2)^{1/2}]$$
$$\tilde{\chi}_p = \arctan(\Delta\dot{\eta}/\Delta\dot{\xi})$$
$$V_{ex_3} L_3 = V_{ex_3} L' + G$$
$$A_y = L^* + V_{ex_3} L_3$$
$$J_3 = J' + T_3 G$$
$$C' = J_3 - A_y T_3 - \delta_1$$
$$C_y = C' \cos\tilde{\chi}_y$$
$$E_y = \zeta + \dot{\zeta} T^* + \tfrac{1}{2}\ddot{\zeta}_g T^{*2} - C' \sin\tilde{\chi}_y$$
$$\delta_3 = J_1 + J_2 + T_1 V_{ex_2} L_2$$
$$B_y = J_3 + T_{1C} V_{ex_3} L_3 + \delta_3$$
$$\delta_4 = Q_1 + Q_2 - T_2 J_1 + T_1 S_2$$
$$\delta_5 = \delta_3(T_3 + T_C)$$
$$S_3 = J_3 - T_3 V_{ex_3} L_3$$
$$Q_3 = \tfrac{1}{2} T_3^2 V_{ex_3} + S_3(\tau_3 + T_{1C})$$
$$D' = \delta_4 - \delta_5 + Q_3$$
$$D_y = D' \cos\tilde{\chi}_y$$
$$K_3 = B_y E_y/(A_y D_y - B_y C_y)$$
$$\chi_y' = \tilde{\chi}_y - K_3$$

CUTOFF WHEN $V = V_T$

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Figure 2.3-2 Iterative Guidance Mode Equations, Flight to Orbit

INPUTS FOR OUT OF ORBIT

Vehicle Dependent Inputs (1)

T' = estimated burning time out of parking orbit

Mission Dependent Inputs (28)

$\underline{M}_i = M_{i0} + M_{i1}\,T + M_{i2}\,T^2 + M_{i3}\,T^3$
unit aim vector

$M = R_0 + R_1 T + R_2 T^2 + R_3 T^3$
aim vector magnitude

$e_N = e_0 + e_1 T + e_2 T^2 + e_3 T^3$
nominal eccentricity

$C_3 = C_0 + C_1 T + C_2 T^2 + C_3 T^3$
cutoff enery

r_N = nominal radius at time of ignition

K_6 = mission constant

COSA = cosine of angle before $\underline{M}$ to ignite

TIGA = cosine of angle before $\underline{M}$ to begin chill down

QUADRANT TEST

IGNITION INHIBITOR SWITCH

AFTER PARKING ORBIT INJECTION
COAST UNTIL

$$\text{COS A} = \frac{\underline{r}\cdot\underline{M}}{|\underline{r}|} + \text{TIGA}$$

IGNITION OCCURS IN TIG SECONDS

MATRIX TO TRANSFORM FROM PLATFORM COORDINATES TO GUIDANCE COORDINATES

$$[A] = \begin{bmatrix} \sin A_Z & 0 & \cos A_Z \\ 0 & 1 & 0 \\ -\cos A_Z & 0 & \sin A_Z \end{bmatrix}$$

$$[B] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\phi_o & \sin\phi_o \\ 0 & -\sin\phi_o & \cos\phi_o \end{bmatrix}$$

$$[C] = \begin{bmatrix} \cos\Theta & -\sin\Theta & 0 \\ \sin\Theta & \cos\Theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$[D] = \begin{bmatrix} \cos i & 0 & \sin i \\ 0 & 1 & 0 \\ -\sin i & 0 & \cos i \end{bmatrix}$$

$$[G] = [D]\ [C]\ [B]\ [A]$$

COMPUTE AT SECOND S-IVB IGNITION

$\underline{M}$ unit aim vector

M aim vector magnitude

e_N nominal eccentricity

C_3 cutoff energy

$e = \frac{r}{F_N}(e_N - 1) + 1$ — eccentricity of cutoff ellipse

$p = \frac{u}{C_3}(e^2 - 1)$ — semilatus rectum

$\cos\phi^* = \frac{1}{e}\left(\frac{p}{M} - 1\right)$ — true anomaly of aim vector

$K_5 = \sqrt{u/p}$ — constant

$\underline{N} = \underline{r} \times \underline{v}$ — normal to parking orbit plane

$DD = (\underline{N}\cdot\underline{M})^2 / |\underline{N}\times\underline{M}|^2 + 1$ — constant

$FF = \underline{N}\cdot\underline{M} / |\underline{N}\times\underline{M}|^2$ — constant

$\underline{S} = \left[DD\,\underline{M} - FF\,\underline{N} + \frac{\underline{N}\times\underline{M}}{|\underline{N}\times\underline{M}|}\left(\frac{1}{\cos^2\phi^*} - DD\right)^{\frac{1}{2}}\right]\cos\phi^*$ perigee vector

$\underline{S}_\perp = \frac{\underline{M} - \underline{S}\cos\phi^*}{\sqrt{1 - \cos^2\phi^*}}$ — vector perpendicular to perigee vector

$\underline{C}_1 = \underline{S}\times\underline{S}_\perp$ — normal to cutoff plane

$\underline{\Omega} = \cos A_Z \cos\phi_o\,\underline{i} + \sin\phi_o\,\underline{j} - \sin A_Z \cos\phi_o\,\underline{k}$ earth spin vector

$\cos i = \underline{\Omega}\cdot\underline{C}_1$ inclination of cutoff plane

$\underline{r}_L = -\cos A_Z \sin\beta_o\,\underline{i} + \cos\beta_o\,\underline{j} + \sin A_Z \sin\beta_o\,\underline{k}$ vector to launch site

$\underline{DN} = \underline{C}_1 \times \underline{\Omega}$ constant vector

$\Theta = \arctan\left(\frac{\cos i \sin\psi_o - \underline{C}_1\cdot\underline{r}_L}{\underline{DN}\cdot\underline{r}_L}\right)$ descending node

$\alpha = \arctan\left(\frac{\underline{DN}\cdot\underline{S}_\perp}{\underline{DN}\cdot\underline{S}}\right)$ angle from $\underline{S}$ to descending node

TERMINAL RANGE ANGLE CALCULATION IN ORBIT PLANE

$L_2 = \ln[\tau_2/(\tau_2 - T_2)]$

$J_2 = V_{ex_2}(\tau_2 L_2 - T_2)$

$S_2 = J_2 - T_2 V_{ex_2} L_2$

$Q_2 = \frac{1}{2} V_{ex_2} T_2^2 + \tau_2 S_2$

$\tau_1 = V_{ex_1}/(F/M)$

$L_1 = \ln[\tau_1/(\tau_1 - T_1)]$

$J_1 = V_{ex_1}(\tau_1 L_1 - T_1)$

$S_1 = J_1 - T_1 V_{ex_1} L_1$

$Q_1 = \frac{1}{2} V_{ex_1} T_1^2 + \tau_1 S_1$

$L^* = V_{ex_1} L_1 + V_{ex_2} L_2$

$\delta_1 = -S_1 - J_2 + L^*(T_2 + T_C)$

$T_{IC} = T_1 + T_2 + T_C$

$L' = \ln[\tau_3/(\tau_3 - T')]$

$J' = V_{ex_3}(\tau_3 L' - T')$

$T^* = T' + T_{IC}$

$A' = L^* + V_{ex_3} L'$

$\delta_2 = VT^* - J' + A'T' - K_6(\tau_3 - T')(A' + V - V_T)L'$

$\begin{bmatrix} x_{FP} \\ y_{FP} \\ z_{FP} \end{bmatrix} = [G]\begin{bmatrix} x \\ y \\ z \end{bmatrix}$

$\phi_T = \arctan(x_{FP}/y_{FP}) + \frac{1}{\eta_T}(\delta_1 + \delta_2)$

$\Delta\Phi = \phi_T + \alpha$ — true anomaly

$\theta_T = \arctan\left[\frac{e\sin\Delta\Phi}{1 + e\cos\Delta\Phi}\right]$ — path angle

$\eta_T = p/(1 + e\cos\Delta\Phi)$ — radius

$V_T = K_5(1 + e^2 + 2e\cos\Delta\Phi)^{\frac{1}{2}}$ — velocity

$\dot{\eta}_T = V_T \sin\theta_T$ — velocity along η axis

$\dot{\xi}_T = V_T \cos\theta_T$ — velocity along ξ axis

POSITION, VELOCITY, F/m & μ FROM NAVIGATION

x, y, z, ẋ, ẏ, ż, F/m, μ

COORDINATE ROTATIONS

$\ddot{\eta}_{gT} = -\mu/\eta_T^2$

$[\phi_T] = \begin{bmatrix} \cos\phi_T & -\sin\phi_T & 0 \\ \sin\phi_T & \cos\phi_T & 0 \\ 0 & 0 & 1 \end{bmatrix}$

$[K] = [\phi_T][G]$

$\begin{bmatrix} \xi \\ \eta \\ \zeta \end{bmatrix} = [K]\begin{bmatrix} x \\ y \\ z \end{bmatrix}, \quad \begin{bmatrix} \dot{\xi} \\ \dot{\eta} \\ \dot{\zeta} \end{bmatrix} = [K]\begin{bmatrix} \dot{x} \\ \dot{y} \\ \dot{z} \end{bmatrix}$

$\begin{bmatrix} \ddot{\xi}_g \\ \ddot{\eta}_g \\ \ddot{\zeta}_g \end{bmatrix} = \frac{1}{2}\left[\begin{bmatrix} 0 \\ \ddot{\eta}_{gT} \\ 0 \end{bmatrix} + [K]\begin{bmatrix} g_1 \\ g_2 \\ g_3 \end{bmatrix}\right]$

TIME TO CUTOFF CALCULATION

$\Delta\xi^* = \xi_T - \xi - \dot{\xi}_g T^*$

$\Delta\dot{\eta}^* = \dot{\eta}_T - \dot{\eta} - \ddot{\eta}_g T^*$

$\Delta\dot{\zeta}^* = -\dot{\zeta} - \dot{\zeta}_g T^*$

$G = \frac{1}{2}\left[\frac{(\Delta\xi^*)^2 + (\Delta\dot{\eta}^*)^2 + (\Delta\dot{\zeta}^*)^2}{A'} - A'\right]$

$\Delta T = G(\tau_3 - T')/V_{ex_3}$

$T_3 = T' + \Delta T$

$T^* = T^* + \Delta T$

PITCH AND YAW ANGLE CALCULATIONS

$M = \cos\tilde{\chi}_y + K_3 \sin\tilde{\chi}_y$

$N = K_4 \sin\tilde{\chi}_y$

$A_P = MA_y - NB_y$

$P_1 = -\frac{1}{2} T_1^2 V_{ex_1} + \tau_1 J_1$

$P_2 = -\frac{1}{2} T_2^2 V_{ex_2} + J_2(\tau_2 + 2T_1)$

$P_3 = -\frac{1}{2} T_3^2 V_{ex_3} + J_3(\tau_3 + 2T_{IC})$

$B_P = MB_y - N(T_1^2 V_{ex_2} L_2 + T_{IC}^2 V_{ex_3} L_3 + P_1 + P_2 + P_3)$

$E_P = \eta - \eta_T + \dot{\eta}T^* + \frac{1}{2}\ddot{\eta}_g T^{*2} - (MC' - ND')\sin\tilde{\chi}_P$

$C_P = (MC' - ND')\cos\tilde{\chi}_P$

$Q' = \frac{1}{2} T_3^2 V_{ex_3} + \tau_3 S_3$

$U_1 = \frac{1}{6} T_1^3 V_{ex_1} + \tau_1 Q_1$

$U_2 = \frac{1}{6} T_2^3 V_{ex_2} + Q_2(\tau_2 + 2T_1)$

$U_3 = \frac{1}{6} T_3^3 V_{ex_3} + Q'(\tau_3 + 2T_{IC})$

$D_P = \{MD' - N[U_1 + U_2 + U_3 + T_1^2 S_2 + T_{IC}^2 S_3 - (T_3 + T_C)(P_1 + P_2 + T_1^2 V_{ex_2} L_2) - P_1 T_2]\}\cos\tilde{\chi}_P$

$K_1 = B_P E_P/(A_P D_P - B_P C_P)$

$\chi_P' = \tilde{\chi}_P - K_1$

$\Delta\xi = \Delta\xi^* - \dot{\xi}_g \Delta T$

$\Delta\dot{\eta} = \Delta\dot{\eta}^* - \ddot{\eta}_g \Delta T$

$\Delta\dot{\zeta} = \Delta\dot{\zeta}^* - \dot{\zeta}_g \Delta T$

$\tilde{\chi}_y = \arctan\left[\Delta\zeta/(\Delta\xi^2 + \Delta\dot{\eta}^2)^{1/2}\right]$

$\tilde{\chi}_P = \arctan(\Delta\dot{\eta}/\Delta\dot{\xi})$

$V_{ex_3} L_3 = V_{ex_3} L' + G$

$A_y = L^* + V_{ex_3} L_3$

$J_3 = J' + T_3 G$

$C' = J_3 - A_y T_3 - \delta_1$

$C_y = C' \cos\tilde{\chi}_y$

$E_y = \xi + \dot{\zeta}T^* + \frac{1}{2}\ddot{\zeta}_g T^{*2} - C' \sin\tilde{\chi}_y$

$\delta_3 = J_1 + J_2 + T_1 V_{ex_2} L_2$

$B_y = J_3 + T_{IC} V_{ex_3} L_3 + \delta_3$

$\delta_4 = Q_1 + Q_2 - T_2 J_1 + T_1 S_2$

$\delta_5 = \delta_3(T_3 + T_C)$

$S_3 = J_3 - T_3 V_{ex_3} L_3$

$Q_3 = \frac{1}{2} T_3^2 V_{ex_3} + S_3(\tau_3 + T_{IC})$

$D' = \delta_4 - \delta_5 + Q_3$

$D_y = D' \cos\tilde{\chi}_y$

$K_3 = B_y E_y/(A_y D_y - B_y C_y)$

$\chi_y' = \tilde{\chi}_y - K_3$

CUTOFF WHEN

$$V^2 - \frac{2\mu}{r} = C_3$$

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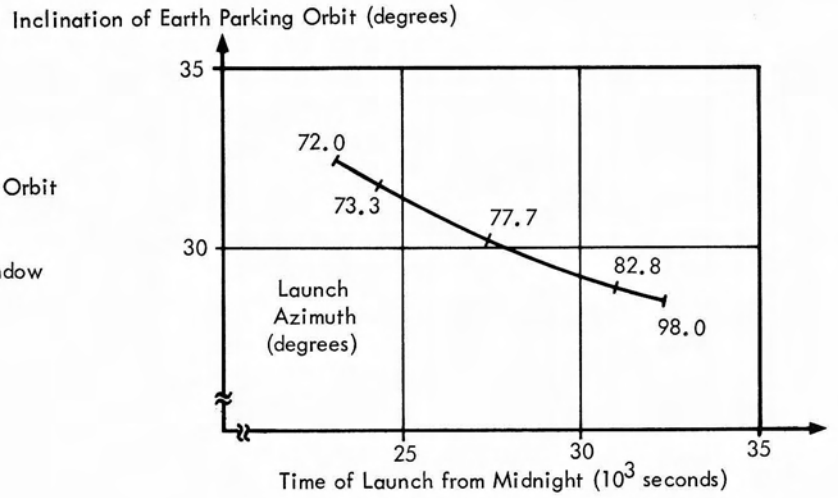
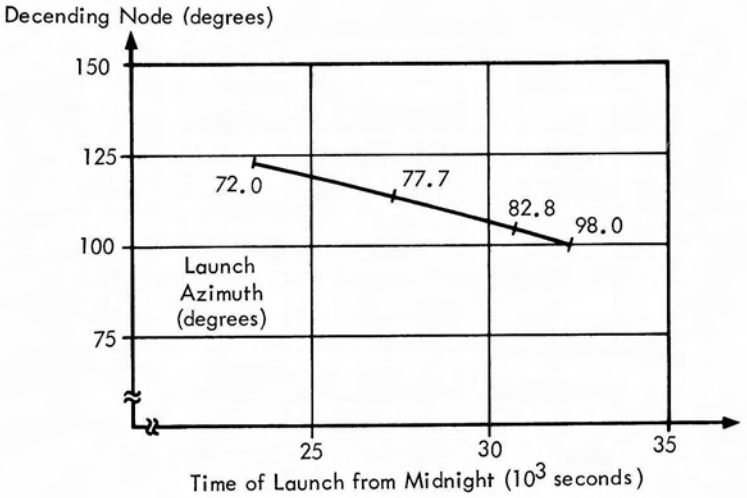
Figure 2.3-3 Iterative Guidance Mode Equations, Flight out of Orbit

Inclination of Earth Parking Orbit
Versus
Time of Launch
for a Typical Launch Window



Time of Launch Versus Descending Node
for a Typical Launch Window



Time of Launch Versus Launch Azimuth
for a Typical Launch Window

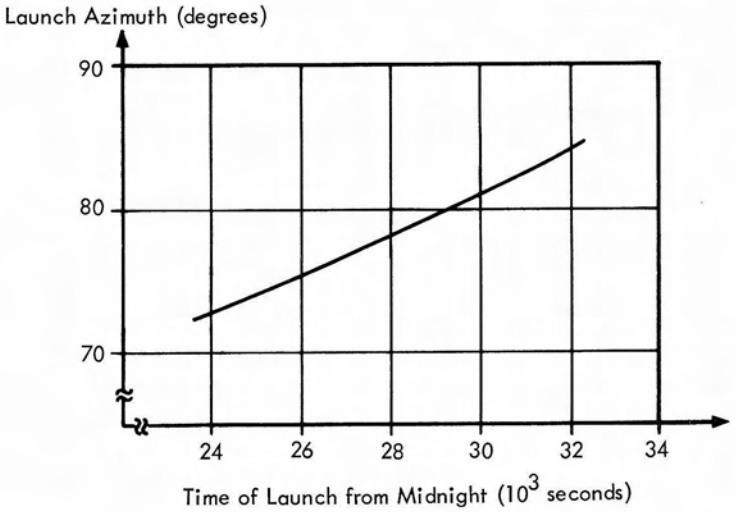


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Figure 2.3-4 Launch Window Parameters

possible to program the computer, change the vehicle configuration, change the mission, and never perform another checkout of the LVDC. Practically, of course, a high confidence level is necessary for crew safety and for accomplishing the desired mission — so checkouts are performed again but of a much more limited nature than if a completely new computer program were required.

The guidance mode, qualitatively described here, is not necessarily a final recommendation; its implementation is merely one way to accomplish the task of successfully performing the Apollo mission and many other orbital and, indeed, interplanetary missions. The details of the cutoff surface must be analyzed carefully with respect to interface and subsequent consistency with the spacecraft guidance mode.

The iterative guidance equations require more LVDC capacity than most of the other guidance schemes optimized for minimum propellant consumption, but considerable flexibility is gained. The same set of guidance command equations is applicable to almost all orbital missions and can be formulated for use with any number of high thrust stages. The small number of presettings that must be calculated for a flight represents physical quantities such as vehicle exhaust velocity, nominal cutoff time, and desired cutoff position and velocity. This is an important characteristic of the scheme since these presettings may be determined without resorting to time-consuming statistical methods. The accuracy and propellant economy with the scheme are excellent. The fuel required to attain the desired cutoff conditions (at orbit insertion) is within 5 kilograms (11.1 pounds) of that required using exact minimum propellant equations obtained with the calculus of variations. This economy is obtained even under severe perturbations such as an engine failure in the first stage of a 2 stag multi-engine vehicle.

2.3.3 GUIDANCE FUNCTIONS IN FLIGHT

The following is a brief summarizing description of guidance functions during the various phases of the Saturn Launch Vehicle Mission in the Apollo Program.

Before launch, the platform is erected with the y_I axis vertical and the x_I axis pointing in the direction of the launch azimuth. Since the launch azimuth is varying with time, the platform is torqued to maintain this orientation. Just prior to lift-off, the

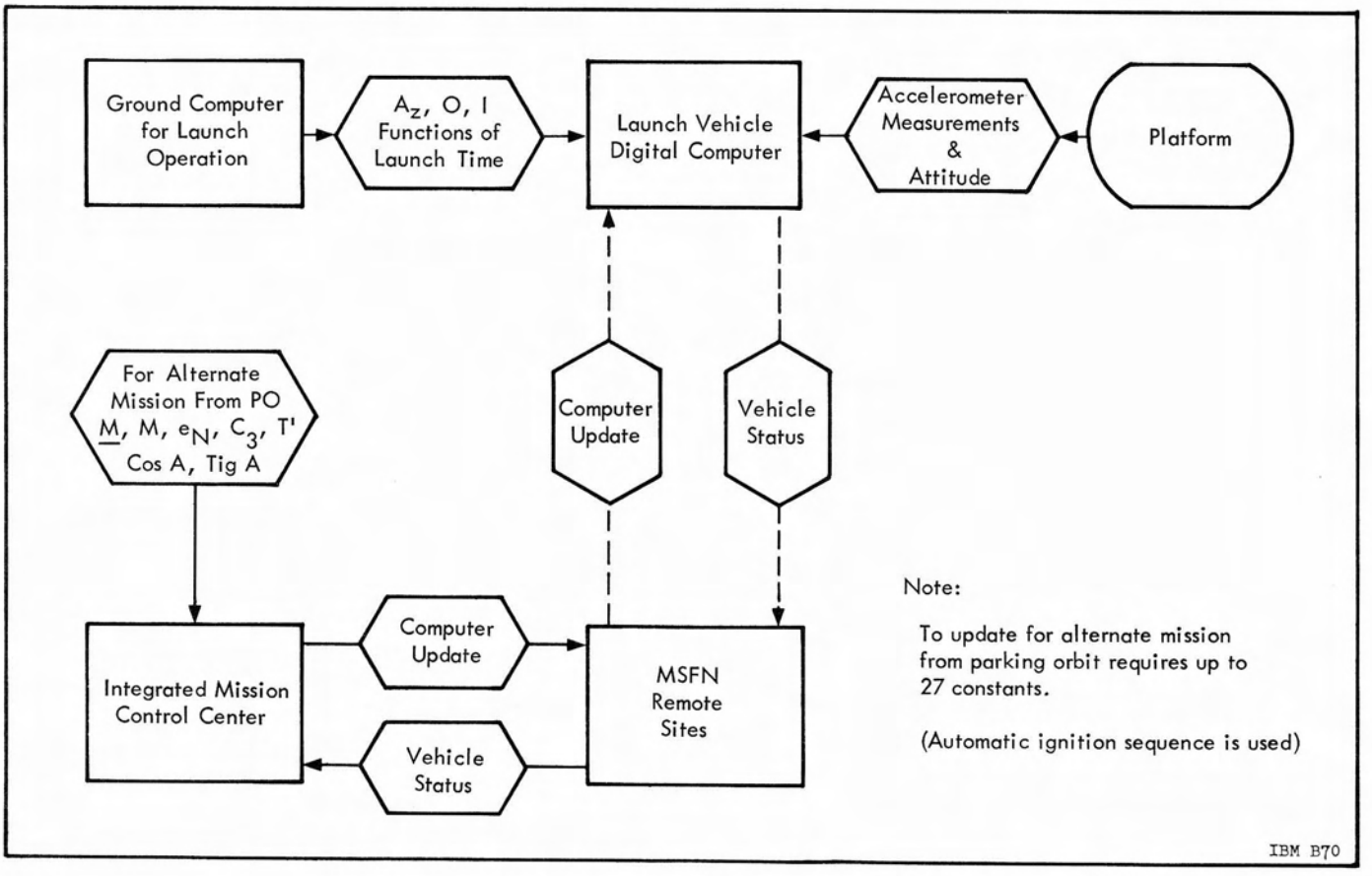


Figure 2.3-5 Linkage Between Vehicle and Ground

platform is released and becomes space-fixed oriented. The x_I axis now determines the flight azimuth.

FIRST STAGE FLIGHT

The vehicle lifts off vertically from the launch pad and maintains its lift-off orientation long enough to clear the ground equipment. It then performs a roll maneuver to align the vehicle with the flight azimuth direction. This maneuver gives the vehicle control axes the correct alignment to the flight plane thus simplifying the computations in the attitude control loop. On the launch pad, the vehicle always has a roll orientation fixed to the launching site.

During first-stage propulsion, a time tilt program, stored in the LVDC, is applied simultaneously with the described roll maneuver. The pitch angle of the vehicle is commanded according to the tilt program which is a function of time only and is independent of navigation measurements. However, navigation measurements and computations are performed throughout the flight, beginning at the time the platform is released (i.e., 5 seconds before lift-off). Cutoff of the first stage engines occurs when the fuel level in the tanks reaches a predetermined level. Thereafter, the first stage is separated from the launch vehicle.

SECOND AND THIRD STAGE FLIGHT

After ignition of the S-II Stage, adaptive guidance (i.e., the iterative guidance mode) is used during all propelled flight phases of the mission. The iterative guidance mode which has been described in paragraph 2.3.2, computes the pitch and yaw angle of the required thrust direction to guide the vehicle on a minimum propellant trajectory into the predetermined parking orbit.

S-II Stage engine cutoff is initiated when the propellant in the S-II tank is consumed to a predetermined level. Following separation of the S-II Stage, the S-IVB Stage engine is ignited.

By this time the vehicle has reached approximately the orbital altitude and the S-IVB propulsion provides the necessary velocity for the circular parking orbit. When the predetermined velocity has been obtained, the guidance computations command engine cutoff.

Acceleration, velocity, and aerodynamic pressure for a typical Saturn V powered flight trajectory into earth orbit are shown in Figure 2.3-7. The step in the F/M curve around 420 seconds is caused by a change of the propellant mixture ratio to increase the

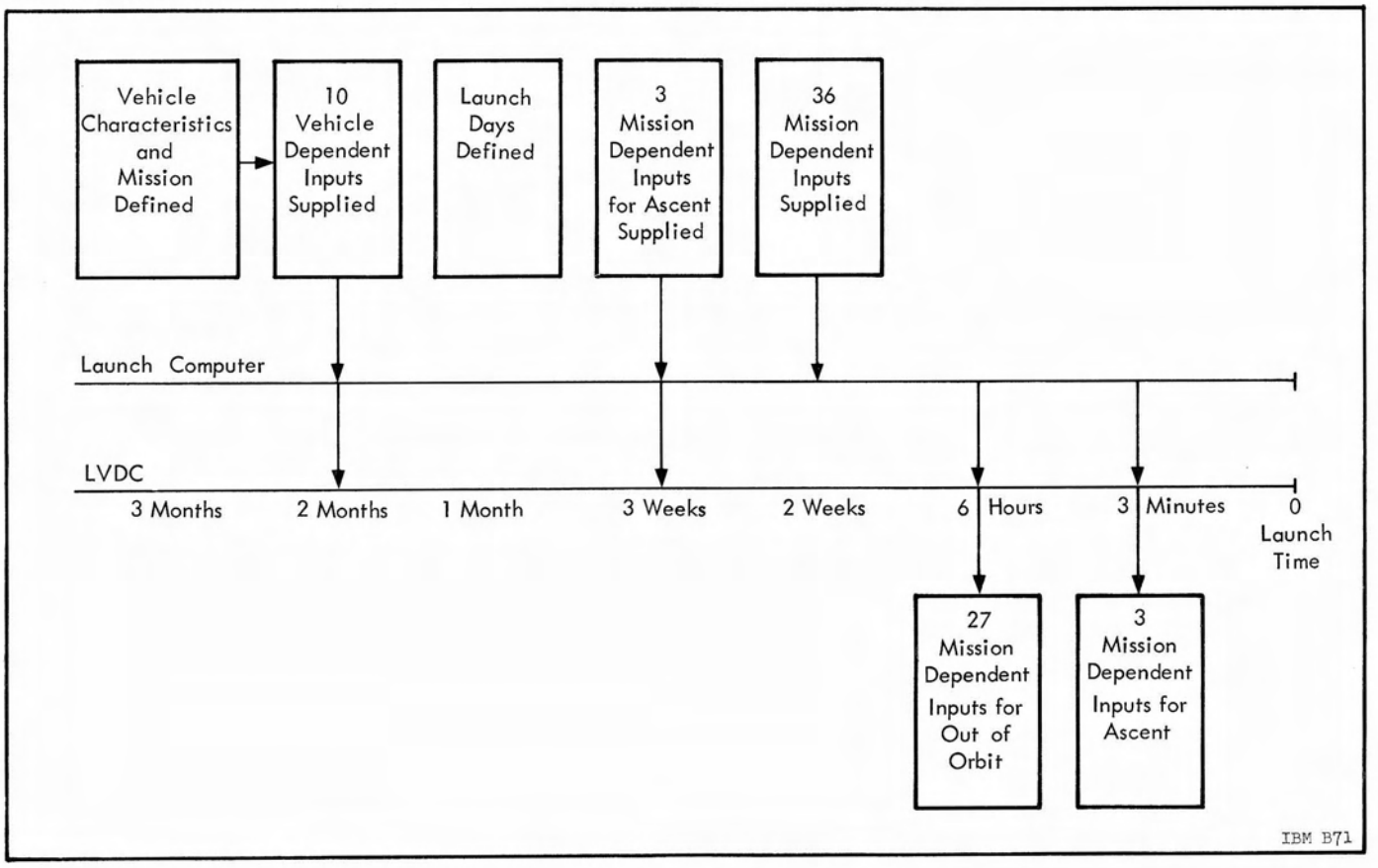


Figure 2.3-6 Guidance System Input Sequence

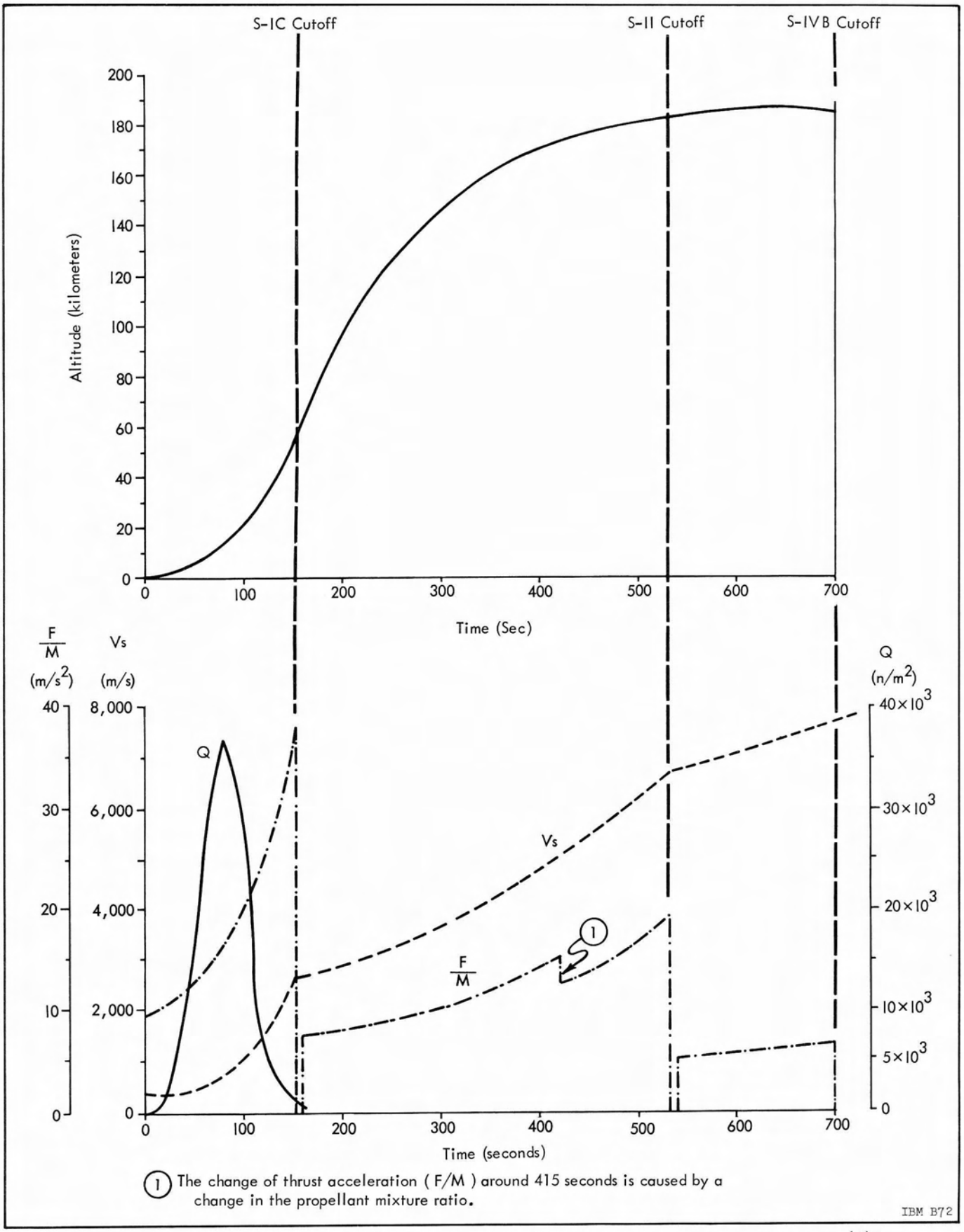


Figure 2.3-7 Altitude, Acceleration (F/M), Velocity (V_S), and Aerodynamic Pressure (Q) for a Typical Saturn Trajectory

specific impulse which, however, reduces the thrust and therefore cannot be applied earlier.

ORBITAL FLIGHT

During orbital coast flight, the navigation program continually computes the vehicle position and velocity from the equations of motion based on insertion conditions. Attitude of the vehicle roll axis in orbit is maintained at 90 degrees with respect to the local vertical. The local vertical is determined from navigational computations. The time of re-ignition of the S-IVB engine and the required thrust orientation for powered flight-out-of-orbit are computed during each orbit.

In orbit, navigation and guidance information in the LVDC can be updated by data transmission from ground stations through the IU radio command system.

TRANSLUNAR INJECTION

When the computed time of re-ignition occurs, the S-IVB engine is ignited. The same guidance equations are used again for the translunar injection. The S-IVB propulsion is cutoff when the proper energy (V^2) for translunar injection is achieved.

In the following flight phase, up to and through the transposition maneuver, navigation computations continue.

CHAPTER 3

ATTITUDE CONTROL

TABLE OF CONTENTS

SECTION 3.1

ATTITUDE CONTROL DURING POWERED FLIGHT

3.1.1 GENERAL CONSIDERATIONS

The attitude control requirement of the Saturn Launch Vehicle can be divided into attitude control during powered flight and attitude control during coast flight. Attitude control and stabilization during powered flight are accomplished by swivelling of the propulsion engines to control thrust vector direction. During coast flight (in orbit and after translunar injection), attitude control is provided by the auxiliary propulsion system of the S-IVB Stage. This auxiliary propulsion system is used also during powered flight of the S-IVB Stage for roll control which cannot be achieved with the single engine of the S-IVB Stage.

Control of the launch vehicle during ascent into earth orbit can be divided into 2 phases. During first-stage powered flight, the vehicle traverses the dense portion of the atmosphere. Large side forces (resulting from aerodynamic flow and wind) can act on the vehicle. Maneuvers during this flight phase are limited because of structural constraints. Structural loads from aerodynamic forces are kept within a tolerable range by controlling the vehicle to achieve a minimum angle of attack. Aerodynamic pressure reaches a maximum at approximately 12 kilometers (7.4 miles) altitude 77 seconds after lift-off. For a typical Saturn V trajectory, see Figure 2.3-7.

From the viewpoint of vehicle control, maneuvers during vacuum flight are limited only to the extent that structural bending and propellant sloshing are not dangerously excited through the nature of the control command.

The objective of the attitude control system during propulsion of the vehicle is to appropriately orient the thrust vector, relative to the vehicle, such that the required attitude commands are performed in a satisfactorily damped mode of rotation.

The vehicle cannot be considered rigid but must be treated as distributed masses connected by an elastic structure. Forces acting on these masses, resulting from atmospheric perturbations or active control of the vehicle, excite the complex spring-mass system and cause body bending. Since the structure possesses low damping, oscillatory bending modes of considerable amplitude can be produced, to which control sensors may be subjected at their particular location. Thus, incorrect information about the total vehicle behavoir may cause self-excitation of the bending modes and instability of the vehicle control system.

The vehicle is aerodynamically unstable — which means that the center of pressure is located forward of the center of gravity. As an example, Figure 3.1-1 is a plot of the center of pressure and the center of gravity for the first phase of the Saturn V flight and shows that the vehicle is unstable except for a short period of time around the 60th flight second.

Much of the vehicle characteristic data varies widely with time and the individual stages. In addition, some can be predetermined only to a certain degree, and tolerances must be imposed. Thus a wide operating range of the control system must be provided.

A typical frequency spectrum for the Saturn V Vehicle during powered flight can be seen in Figure 3.1-2. The frequency bands, rather than single frequencies, are the result of changing vehicle-state conditions because of propellant consumption as a function of flight time. The frequency band marked "engine-reaction-zero" represents the sinusoidal response where the inertial effects of the engine induce forces at the engine gimbal point equal and opposite to the side forces obtained by swivelling the thrust vector. The net effect is that the vehicle bending mode response to the engine deflection is zero at this frequency. This is sometimes known as the "tail-wags-dog" frequency.

The basic control scheme is an attitude/attitude-rate scheme. Accelerometer control may be added to produce drift minimum or load minimum. Using body-

mounted accelerometers, the control law for the thrust vector deflection angle(β)is:

$$\beta = a_0 \Delta\phi + a_1\dot{\phi} + g_2\ddot{\gamma} \qquad (3.1\text{-}1)$$

Where a_0 and a_1 are gain factors, $\Delta\phi = \psi$ and $\dot{\phi}$ are attitude error angle and attitude angular rate respectively, $\ddot{\gamma}$ is the lateral acceleration measured by the accelerometers with its sensitive axis perpendicular to the vehicle longitudinal axis, and g_2 is the corresponding gain factor. The attitude error angle ($\Delta\phi$) is obtained from the stabilized platform, the attitude rate ($\dot{\phi}$) from rate gyros, and the lateral acceleration ($\ddot{\gamma}$) from control accelerometers.

The lateral acceleration control is used during first-stage propulsion only to reduce structural loads from aerodynamic forces and to provide drift-minimum control.

The acceleration measured by the body-mounted Control Accelerometers differs from that measured by the guidance accelerometers. The guidance accelerometers are mounted on the stable platform and measure accelerations with respect to an inertial space coordinate system.

The choice of the control sensor (rate gyros and accelerometers) locations is very important for attitude stabilization of the vehicle. Stabilization of large launch vehicles, with respect to bending and torsion modes, is usually obtained by shaping networks in each of the three control sensor channels.

Elastic body stability may be attained either by phase stabilization or by attenuation of the bending frequencies. Each method has its advantages. Phase stabilization, especially of the lower bending modes, makes it possible to maintain adequate bandwidth at

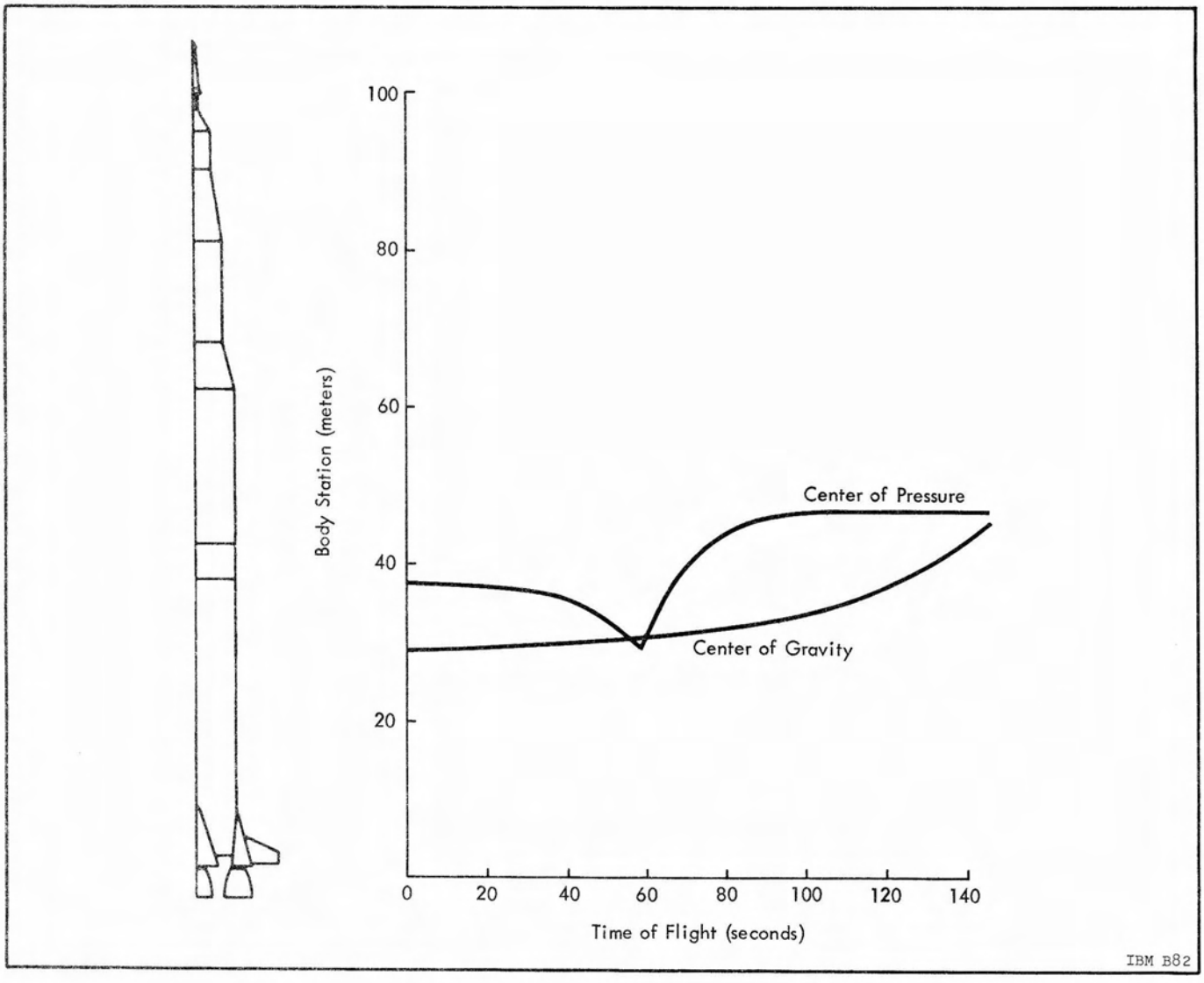


Figure 3.1-1 Variations of CP and CG During Flight

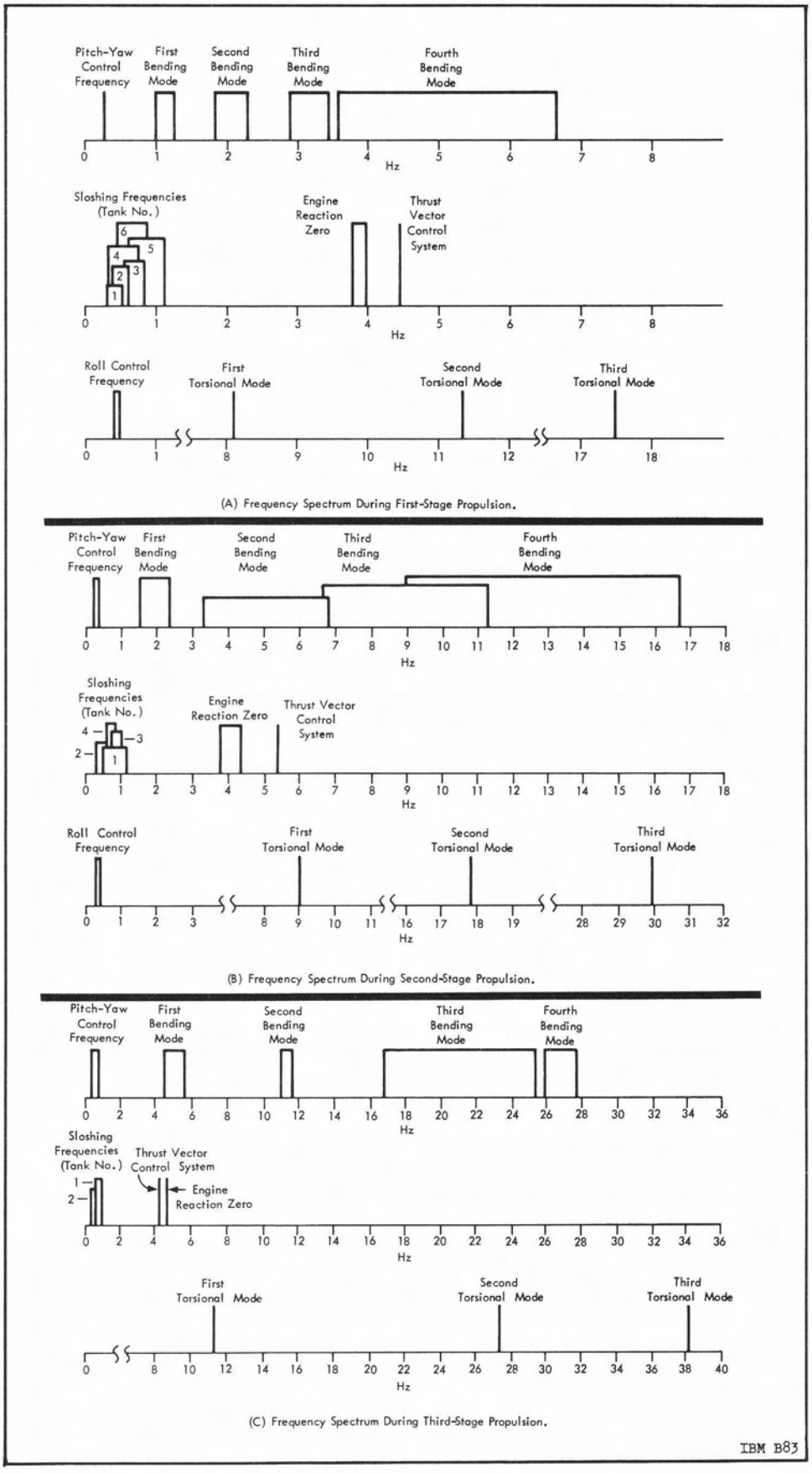


Figure 3.1-2 Typical Saturn V Frequency Spectrum

the control frequency. Also, a phase-stabilized bending mode will damp out faster after excitation than a mode that depends upon attenuation for stabilization. In contrast, stabilization by attenuation is preferable for the higher bending modes since these mode shapes are generally more difficult to define and because it is possible to compensate bending mode shapes and frequencies satisfactorily by attenuation. Thus for practical reasons, phase stabilization is applied to the lower frequencies and gain stabilization (stabilization by attenuation) to the higher frequency spectrum. In the case of large launch vehicles like Saturn V, some bending modes are so close to the control loop frequency that they are best phase stabilized. Thus, for Saturn V during first-stage operation, the first and second bending modes will be phase stabilized and higher modes will be attenuated. During the second-stage powered flight, only the first bending modes will be phase stabilized and higher modes will be attenuated. During the third-stage powered flight, the bending mode frequencies are higher than those for the other stages; therefore, all the bending modes of this stage will be stabilized by attenuation. All torsional modes are at a relatively high frequency and will be attenuated for all stages.

To provide the desired phase, it is necessary that the rate gyro be properly located on the vehicle. Figure 3.1-3 exhibits the Saturn configuration and the first two bending mode shapes.

The attitude gyro stabilized platform is located in the Instrument Unit. Since the control loop gain at the bending mode frequencies is much less through the attitude loop than through the rate loop, the location of the attitude gyro is not as sensitive and is usually determined by other considerations — primarily the need to have one centrally located unit for all stages.

The location of the body-mounted accelerometer (used only in the first-stage propulsion phase) is determined by 2 factors. First, rigid-body stability analyses limit the distance the sensor can be located in longitudinal direction from the vehicle center of gravity. Second, the phase sensed by the accelerometer when located to the rear of the vehicle center of gravity subtracts from the rigid-body lead margin.

The simplified block diagram shown in Figure 3.1-4 illustrates the basic partial control loops, one for each control sensor. $F(\Delta\phi)$, $F(\dot{\phi})$, and $F(\ddot{\gamma})$ are the shaping networks necessary to stabilize the vehicle and a_0, a_1, and g_2 are the total control gains illustrated earlier.

3.1.2 ATTITUDE CONTROL SYSTEM FOR POWERED FLIGHT

The attitude control system of the Saturn V Launch Vehicle provides attitude control and stabilization from launch until separation of the S-IVB/IU Stage from the Apollo Spacecraft. For the second-burn phase of the S-IVB Stage, the Apollo navigation guidance and control system is available as a backup system and sends input signals to the Saturn Flight Control Computer. This backup capability for the S-II and S-IVB first-powered flight is under consideration.

Attitude control of the launch vehicle during powered flight is accomplished by swivelling of the main propulsion engines and thereby changing the orientation of the thrust vector. The S-IB Stage has eight engines. The four outer engines can be swivelled in pitch and yaw by two hydraulic actuators at each engine (see Figure 3.1-5).

The S-IC and S-II Stages have five engines each. The four outer engines can be swivelled in pitch and yaw by two hydraulic actuators at each engine. The S-IVB Stage is propelled by a single engine which can be swivelled in pitch and yaw. In

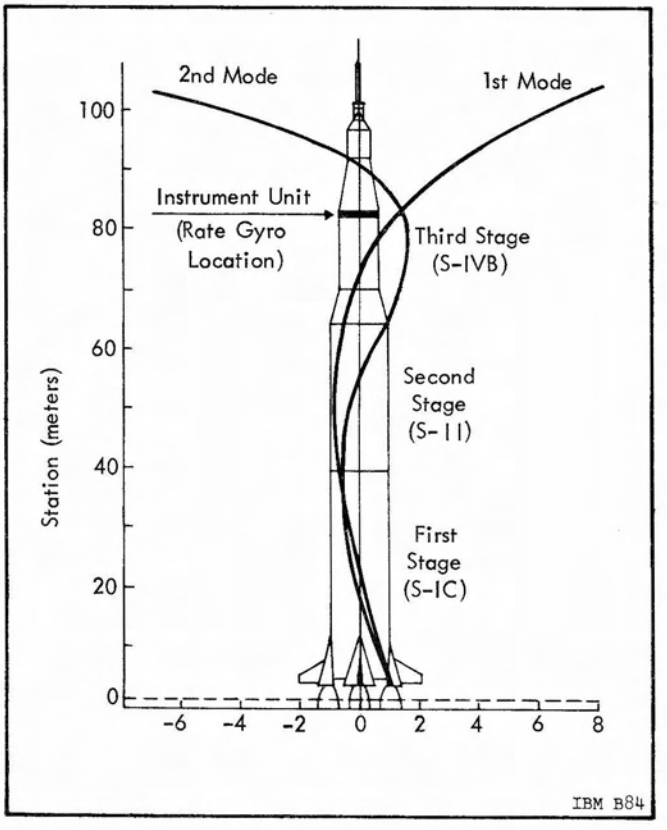


Figure 3.1-3 Shape of the First and Second Bending Modes (Saturn V)

addition, the S-IVB Stage is equipped with an auxiliary propulsion system consisting of 6 nozzles (2 sets of 3 nozzles) mounted on the outside of the aft end of the S-IVB Stage. Four of the six nozzles are required for roll control of the S-IVB Stage which cannot be achieved with a single main propulsion engine. Figure 3.1-6 shows the layout of engine actuators and nozzles for the stages of the Saturn V Vehicle. The polarity tables given in this figure indicate which actuators or nozzles are required to perform a pitch, yaw, or roll maneuver. All four controllable main propulsion engines of a stage are swivelled simultaneously to generate the desired attitude maneuver.

The main components of the Saturn attitude control system are shown in Figure 3.1-7. The platform gimbal angle readings ($\theta_X\ \theta_Y\ \theta_Z$) indicate the orientation of the vehicle in the platform coordinate system ($X_p\ Y_p\ Z_p$). The LVDC computes the required thrust vector orientation, (i.e., the desired gimbal angles ($X_X\ X_Y\ X_Z$) according to the guidance scheme and generates the difference $\Delta\theta = \theta - X$). From the attitude angle differences ($\Delta\theta_X\ \Delta\theta_Y\ \Delta\theta_Z$), attitude error signals ($\psi_p\ \psi_y\ \psi_r$) (with respect to the body fixed pitch, yaw, and roll axes) are generated and sent to the Flight Control Computer.

In addition to the attitude error signals ($\psi_p\ \psi_y\ \psi_r$), the Flight Control Computer receives signals from control sensors — attitude rate signals ($\phi_p\ \phi_y\ \phi_r$) (with respect to the vehicle's pitch, yaw, and roll axes) and lateral acceleration signals ($\ddot{\gamma}_p, \ddot{\gamma}_y$) (along the pitch and yaw axes). All control signals fed into the Flight Control Computer are analog signals. The Flight Control Computer processes and combines these signals according to the control law (Equation 3.1-1) to generate the control signals for the engine actuators and attitude control nozzles.

The number and exact location of the control sensors (rate gyros and control accelerometers) depend on the vehicle configuration and the results of further studies of vehicle dynamics.

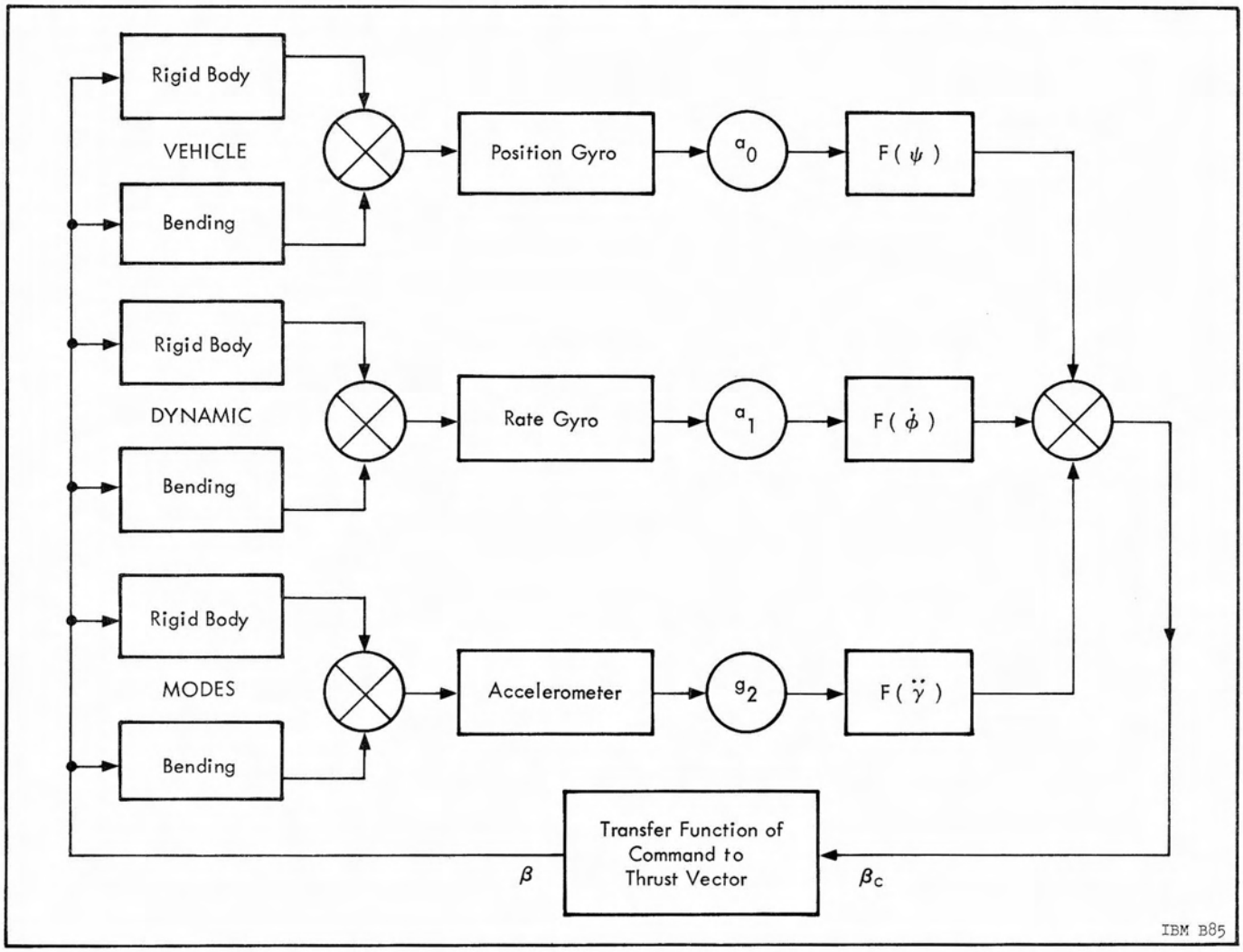
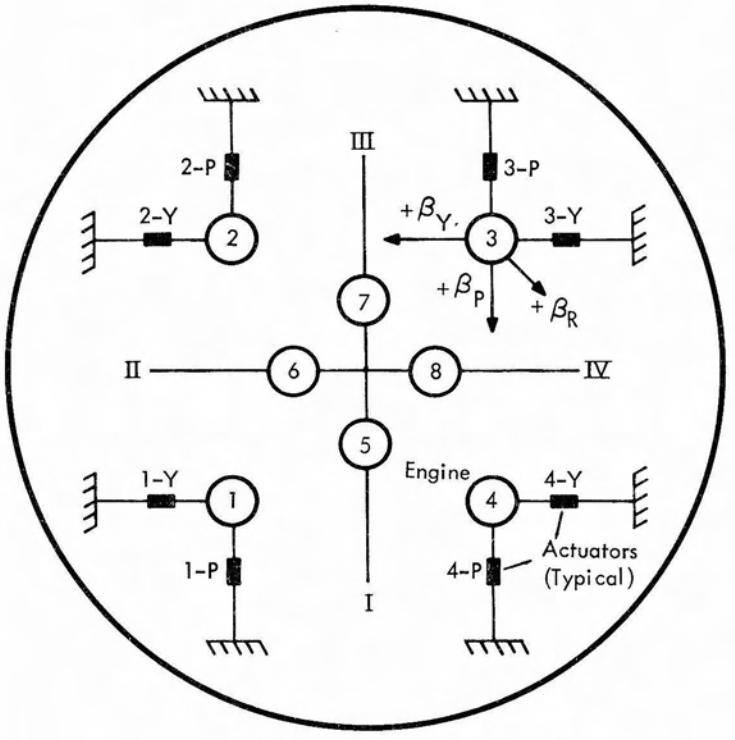
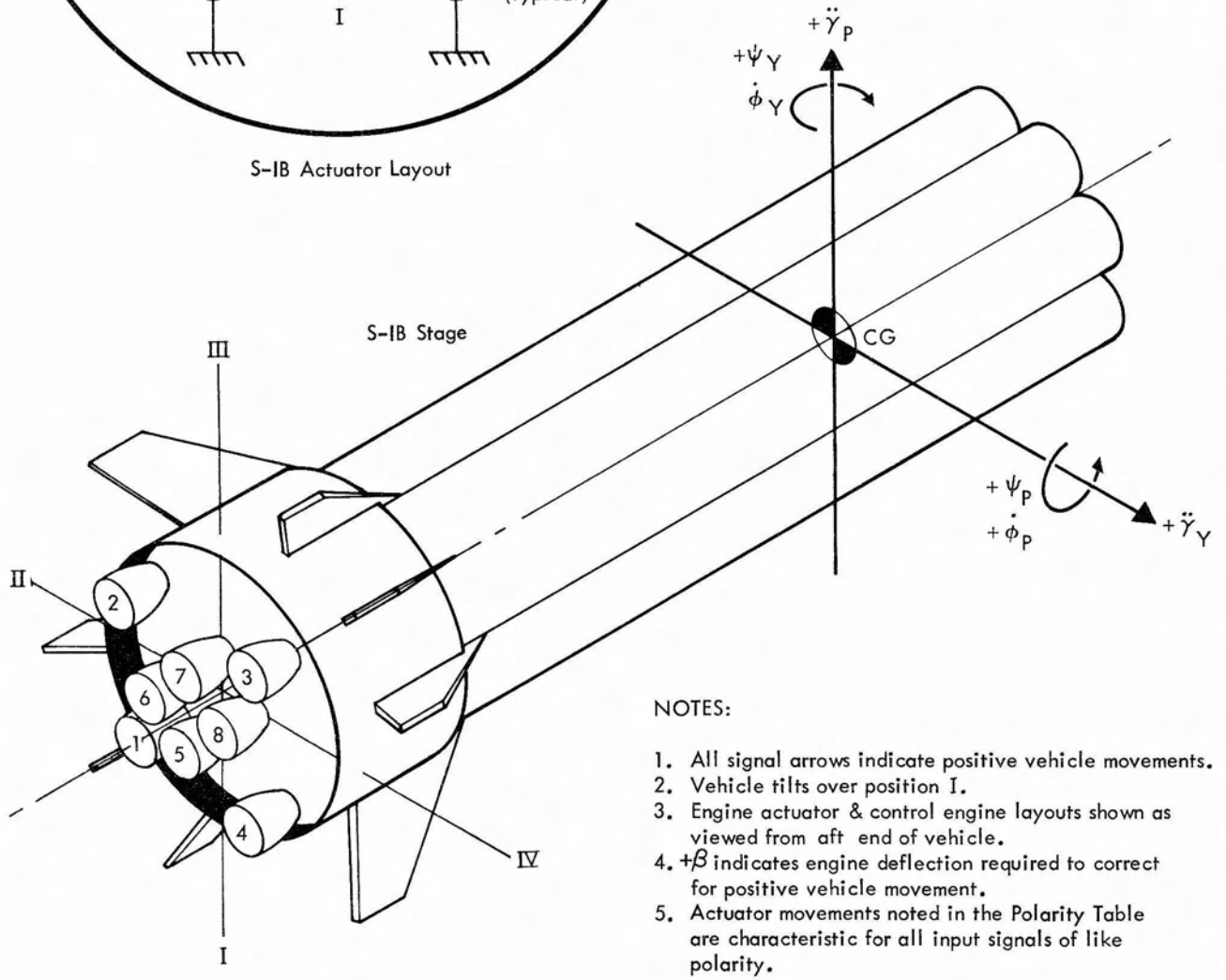


Figure 3.1-4 Control Loop Block Diagram



S-IB Actuator Layout

S-IB Control Signal Polarity Table			
Actuator No.	Signal & Actuator Movement		
	$+\psi_R$	$+\psi_Y$	$+\psi_P$
1-Y	RET	RET	
1-P	EXT		RET
2-Y	EXT	RET	
2-P	RET		EXT
3-Y	RET	EXT	
3-P	EXT		EXT
4-Y	EXT	EXT	
4-P	RET		RET



NOTES:

1. All signal arrows indicate positive vehicle movements.
2. Vehicle tilts over position I.
3. Engine actuator & control engine layouts shown as viewed from aft end of vehicle.
4. $+\beta$ indicates engine deflection required to correct for positive vehicle movement.
5. Actuator movements noted in the Polarity Table are characteristic for all input signals of like polarity.

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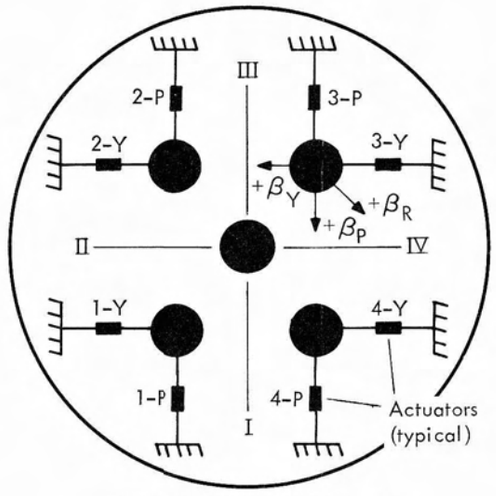
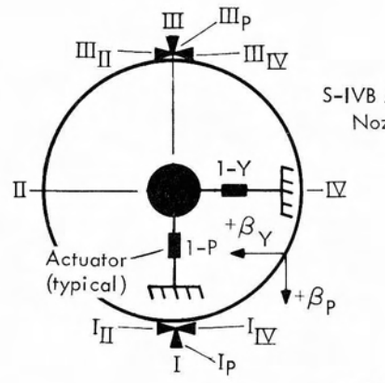
Figure 3.1-5 S-IB Engine and Actuator Configuration

NOTES:

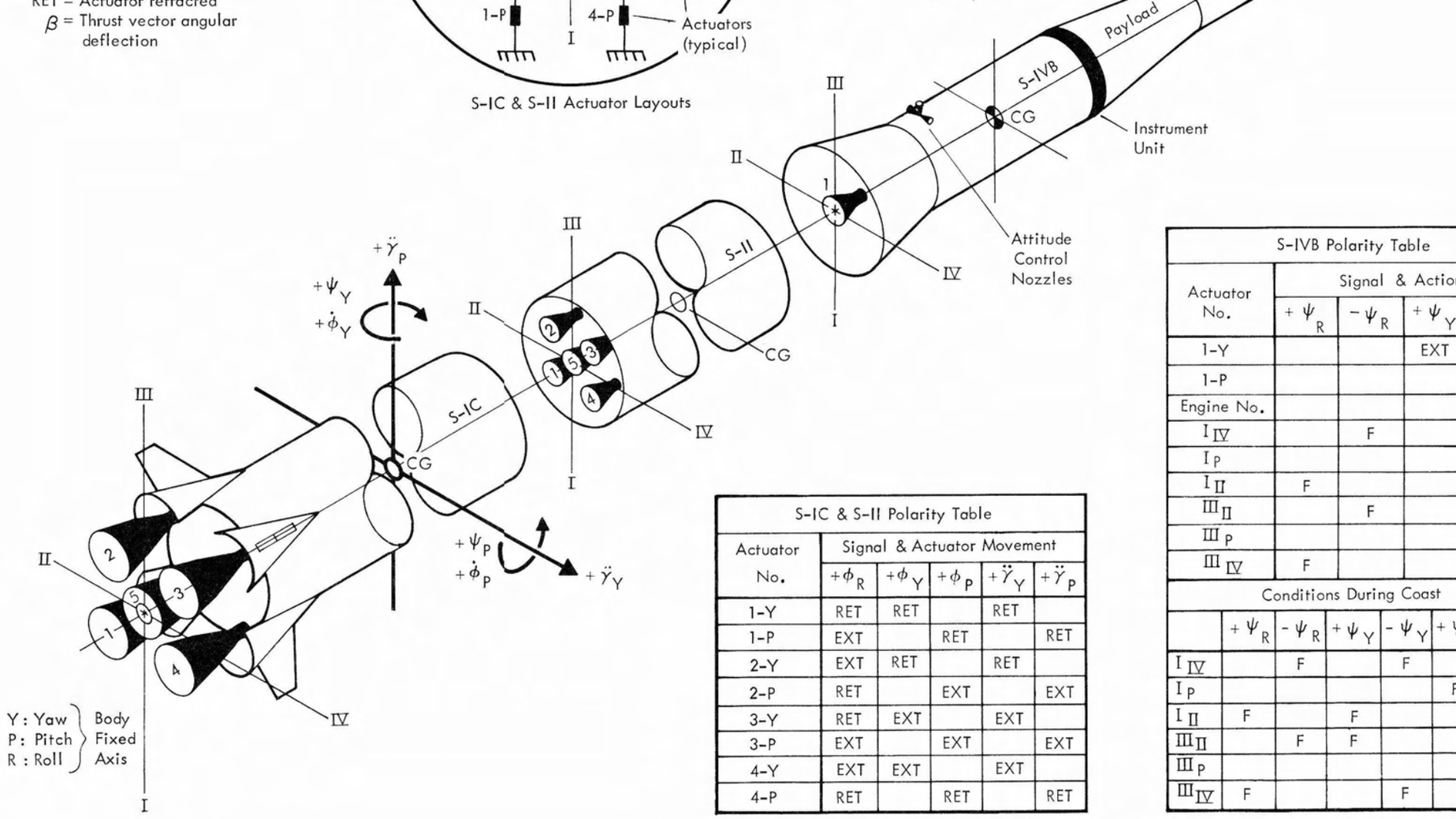
1. All signal arrows indicate positive vehicle movements.
2. Vehicle tilts over position I.
3. Engine actuator layouts shown as viewed from aft end of vehicle.
4. Directions and polarities shown are typical for all stages.
5. $+\beta$ indicates engine deflection required to correct for positive vehicle movement.
6. CG = Center of gravity
   F = Nozzles on
   EXT = Actuator extended
   RET = Actuator retracted
   β = Thrust vector angular deflection



S-IC & S-II Actuator Layouts



S-IVB Actuator and Nozzle Layout



S-IC & S-II Polarity Table					
Actuator No.	Signal & Actuator Movement				
	$+\phi_R$	$+\phi_Y$	$+\phi_P$	$+\ddot{\gamma}_Y$	$+\ddot{\gamma}_P$
1-Y	RET	RET		RET	
1-P	EXT		RET		RET
2-Y	EXT	RET		RET	
2-P	RET		EXT		EXT
3-Y	RET	EXT		EXT	
3-P	EXT		EXT		EXT
4-Y	EXT	EXT		EXT	
4-P	RET		RET		RET

S-IVB Polarity Table				
Actuator No.	Signal & Action			
	$+\psi_R$	$-\psi_R$	$+\psi_Y$	$+\psi_P$
1-Y			EXT	
1-P				RET
Engine No.				
I_{IV}		F		
I_P				
I_{II}	F			
III_{II}		F		
III_P				
III_{IV}	F			
Conditions During Coast				
	$+\psi_R$	$-\psi_R$	$+\psi_Y$	$-\psi_Y$	$+\psi_P$	$-\psi_P$
I_{IV}		F		F		
I_P					F	
I_{II}	F		F			
III_{II}		F	F			
III_P						F
III_{IV}	F			F		

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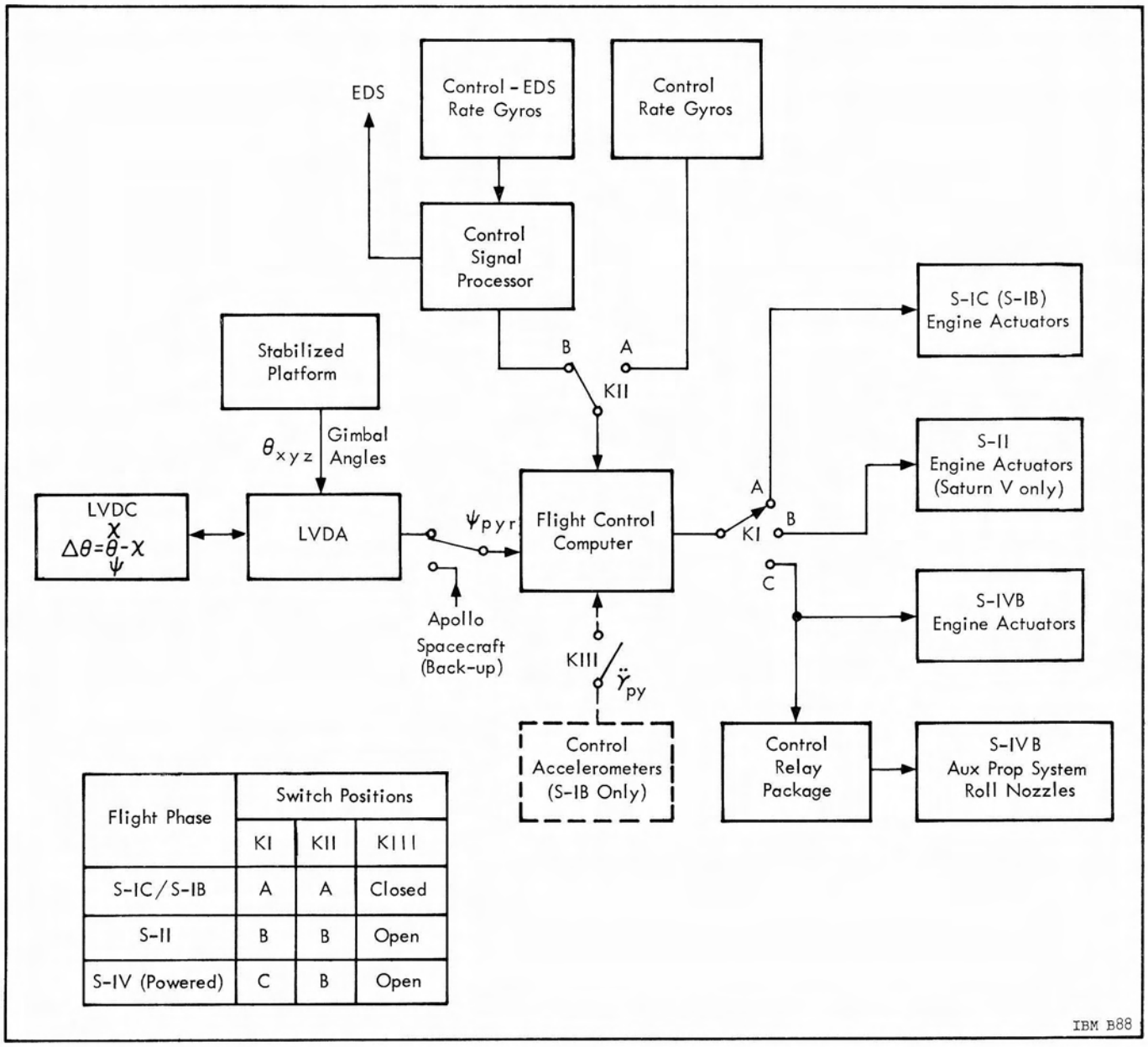
Figure 3.1-6 Saturn V Engines, Actuators, and Nozzle Arrangement

The Saturn IB Vehicle attitude control system will use signals from two Control Accelerometers (during first-stage powered flight only). There are two different schemes under consideration for the S-IB powered flight phase. In the first scheme, lateral acceleration information is supplied by Control Accelerometers located in the IU, and angular rate signals are provided by the Control-EDS Rate Gyros also located in the IU. In the second scheme, the Control Accelerometers and an additional Control Rate Gyro package would be located at the left end of the S-IVB Stage. After separation of the S-IB Stage, only the Control-EDS Rate Gyros in the IU will be used.

Control studies of the Saturn V Vehicle have indicated that no appreciable reduction in bending moments is obtained with body-fixed control accelerometers. Therefore, no control accelerometers will be used in Saturn V Vehicles. During the S-IC powered flight, either the Control-EDS Rate Gyros in the IU or a separate Control Rate Gyro package at the aft end of the S-IVB Stage will be used. After the first-stage separation, only the Control-EDS Rate Gyros in the IU will be used.

A processing and flow diagram for attitude control signals during powered flight is illustrated in Figure 3.1-8. The analog attitude angle difference



Flight Phase	Switch Positions		
	KI	KII	KIII
S-IC/S-IB	A	A	Closed
S-II	B	B	Open
S-IV (Powered)	C	B	Open

Figure 3.1-7 Saturn Control System Block Diagram (Powered Flight)

signals (θ_x θ_y θ_z) from the gimbal angle resolvers are converted in the LVDA to digital signals with a readout rate of 25 signals per second. The guidance command angles (χ_x χ_y χ_z) are computed once per second. Interpolation between computed and predicted χ angles (from the guidance scheme) also provides χ angle data 25 times per second by using the following equations:

$$D\chi = \frac{1}{25} (\chi_{j+1} - \chi_i) \quad \text{for} \quad \chi_x \; \chi_y \; \chi_z$$

and

$$\chi_i = \chi_{i-1} + D\chi \qquad \text{for } \chi_x \; \chi_y \; \chi_z$$

The attitude angle difference ($\Delta\theta$) between interpolated χ angles and gimbal angles (θ) is computed 25 times per second:

$$\Delta\theta_x = \chi_x - \theta_x$$

$$\Delta\theta_y = \chi_y - \theta_y$$

$$\Delta\theta_z = \chi_z - \theta_z$$

The χ angles are computed in the $X_S Y_S Z_S$ coordinate system, and the θ angles are measured in the plot form coordinate system (X_p Y_p Z_p). Both systems are space-fixed and parallel. The X_p Y_p Z_p system has its origin at the stabilized platform, while the X_S Y_S Z_S system has its origin at the earth's center.

The attitude angle differences ($\Delta\theta$) are then transformed into the body-fixed axis system to generate the attitude error signals (ψ_p ψ_y ψ_r). This transformation is performed using the simplified equations for the Euler angle rotations:

$$\psi_p = K_p (K_1 \Delta\theta_z + K_2 \Delta\theta_x)$$

$$\psi_y = K_y (K_5 \Delta\theta_x - K_4 \Delta\theta_2)$$

$$\psi_r = K_r (\Delta\theta_y + K_3 \Delta\theta_2)$$

where

$$K_1 = \cos\frac{(\chi_y + \theta_y)}{2} \cos\frac{(\chi_x + \theta_x)}{2}$$

$$K_2 = \sin\frac{(\chi_y + \theta_y)}{2}$$

$$K_3 = \sin\frac{(\chi_x + \theta_x)}{2}$$

$$K_4 = \sin\frac{(\chi_y + \theta_y)}{2} \cos\frac{(\chi_x + \theta_x)}{2}$$

$$K_5 = \cos\frac{(\chi_y + \theta_y)}{2}$$

For guidance of the vehicle, a guidance command (χ) rate of once per second is sufficient. Attitude control signals are generated 25 times per second to minimize vehicle stabilization problems and provide near continuous attitude control (the coefficients K_1 through K_5 are calculated only once per second).

The approximate transport delays from the time the gimbal angles are read until the attitude error is issued is 4.92 milliseconds in yaw, 3.28 milliseconds in pitch, and 3.198 milliseconds in roll. These times, combined with 0.492 millisecond required to return to the slow loop, give a total computation time in the fast loop of 11.89 milliseconds.

The gimbal angles are read from the fine resolvers (resolution of 0.00279 degree) 25 times per second. The backup resolvers, which replace the fine resolvers, if necessary, have a resolution of 0.0893 degree.

The attitude error signals (ψ) from the LVDC are converted to analog voltages by ladder decoders in the LVDA. The resolution of the ladders is 0.0575 degree with a maximum value of 15.3 degrees.

The analog attitude error signal is fed to the Flight Control Computer where it is combined with the angular rate signals and lateral acceleration signals. A functional description of the Flight Control Computer is given in Section 3.4.

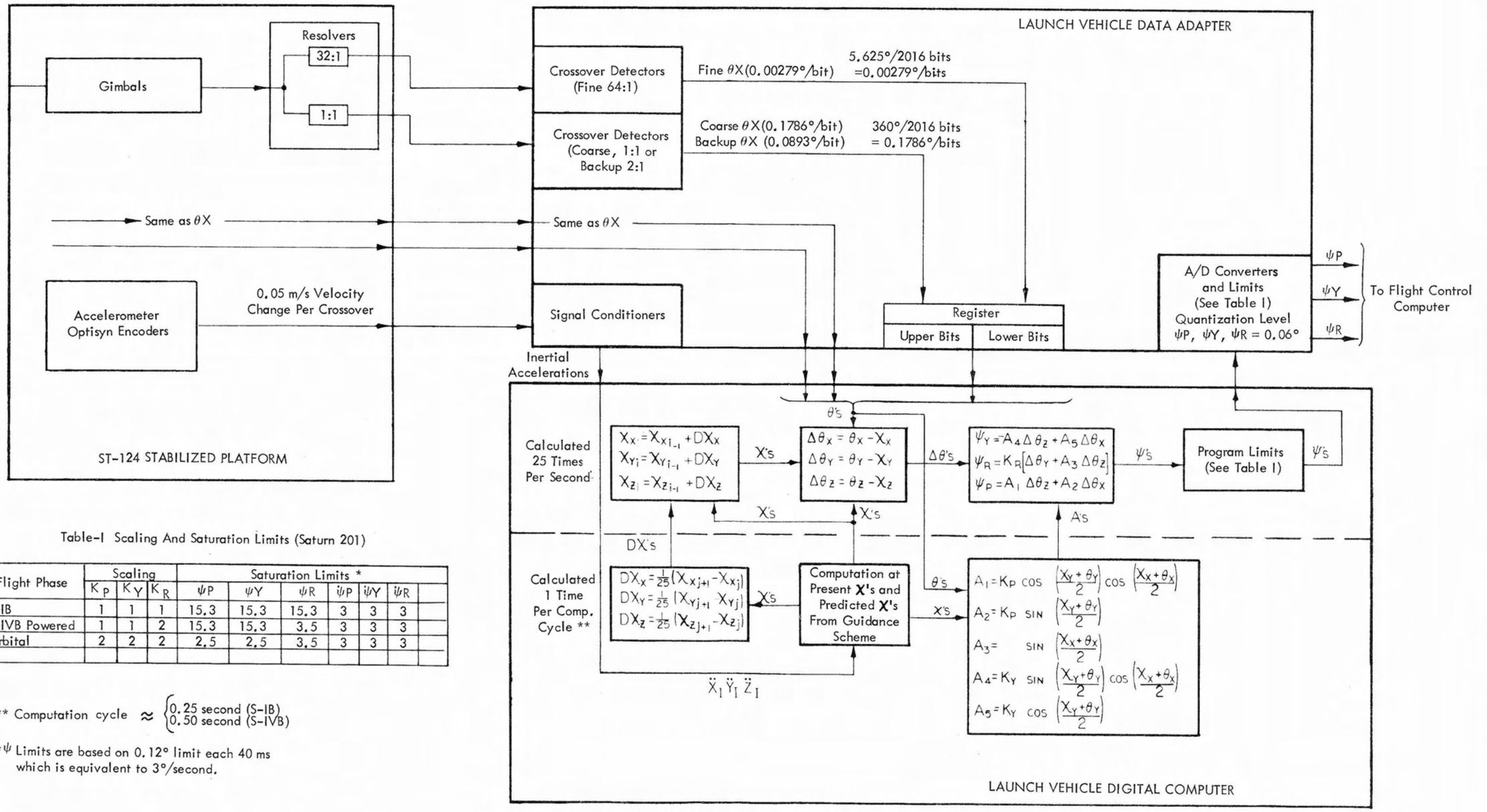


Table-I Scaling And Saturation Limits (Saturn 201)

Flight Phase	Scaling			Saturation Limits *						
	K_P	K_Y	K_R	ψP	ψY	ψR	$\dot{\psi}$P	$\dot{\psi}$Y	$\dot{\psi}$R	
S-IB	1	1	1	15.3	15.3	15.3	3	3	3	
S-IVB Powered	1	1	2	15.3	15.3	3.5	3	3	3	
Orbital	2	2	2	2.5	2.5	3.5	3	3	3	

** Computation cycle ≈ {0.25 second (S-IB) / 0.50 second (S-IVB)

*ψ Limits are based on 0.12° limit each 40 ms which is equivalent to 3°/second.

Figure 3.1-8 Attitude Signal Flow Diagram

SECTION 3.2

ATTITUDE CONTROL DURING COAST FLIGHT

During coast flight, attitude control of the vehicle is accomplished by means of the S-IVB Stage auxiliary propulsion system which contains six attitude control engines (thrust nozzles). When fired, the nozzles produce torques about the center of gravity of the vehicle. They are controlled in a pulse-type manner (full thrust or OFF) by the spatial amplifiers in in the Flight Control Computer. The attitude control engines are turned ON when the input signal to the spatial amplifier exceeds certain limits and turned OFF when the input signal falls below a set threshold. The control scheme generates thrust pulses of variable duration at changing intervals which are controlled by the pseudo rate modulators in the spatial amplifier. Over a certain range of the input signal, the output of the modulator is pulse-width and frequency modulated and is a function of the input signal magnitude. Above this range, the output (thrust) is continuously ON and below this range, it is OFF.

A phase diagram (Figure 3.2-1) shows the angle and angular rate relationship for a limit cycle operation. When the vehicle is rotating in a positive direction with positive angle (corresponding to point A on the diagram), it will reach point B when the combination of ψ and $\dot{\phi}$ exceeds the upper side of the attitude deadband — thus firing the rocket motor. The angular rate of $\dot{\phi}$ decreases and changes to a negative quantity, placing the vehicle at point C on the diagram where the signal, still positive, falls below the level required to keep the motor ON, and the torque disappears. From this point, the vehicle drifts at a constant angular velocity toward condition D where the negative deadband limit is exceeded.

The attitude control engines of the S-IVB Stage auxiliary propulsion system are used to control the vehicle attitude in roll during powered flight phases and in pitch, yaw, and roll during coast flight phases. These engines are located in 2 modules 180 degrees apart on the aft end of the S-IVB Stage. One module is located over position I and the other over position III as shown in Figure 3.1-6. Each module has three hypergolic attitude control engines. One engine of each module is used to control the vehicle's attitude in pitch while the other two are used in yaw and roll control.

The attitude engine control signal is composed of an attitude error signal (ψ) and a vehicle turning rate signal ($\dot{\phi}$). The body mounted Control-EDS Rate Gyros, located in the Instrument Unit, supply the desired vehicle turning rate information. Attitude error information (ψ) may come from 2 sources. When the Instrument Unit is controlling the vehicle attitude, error information is supplied by the LVDC through the LVDA as shown in Figure 3.2-2. When the Spacecraft is controlling the vehicle attitude error, information is obtained from the Spacecraft over Spacecraft/IU interface lines. It should be noted in Figure 3.2-2, that attitude error limits of ±2.5 degrees in pitch and yaw and ±3.5 degrees in roll are imposed on the attitude error signals. These error signals are used only by the auxiliary propulsion system. The limits are imposed by the LVDC for IU-generated attitude error signals and by the IU Flight Control Computer for Spacecraft-generated attitude error signals. The necessity for limiting the attitude error signals will be discussed later.

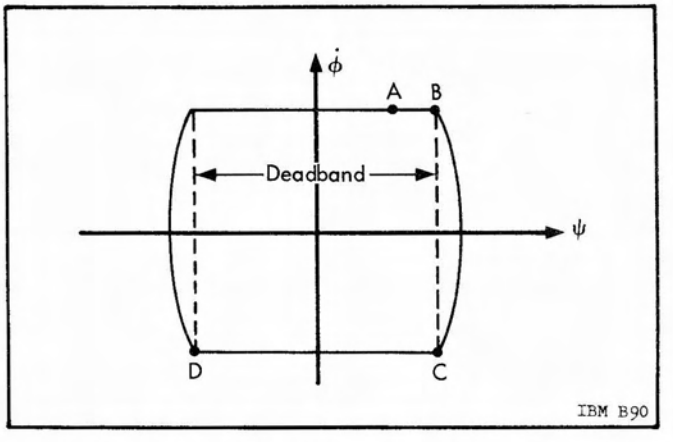


Figure 3.2-1 Limit Cycle Phase Diagram

Control of vehicle attitude about the pitch axis (Figure 3.1-6) will be considered first because it is not coupled with yaw and roll. Figure 3.2-3 is a simplified block diagram of the pitch channel. The commanded vehicle attitude angle χ_p is compared with the actual vehicle attitude (gimbal angle) θ_p and the attitude error signal (ψ) is formulated by the following relationship:

$$\psi = \theta_p - \chi_p \qquad (3.2\text{-}1)$$

The attitude error signal (ψ) is then combined with the vehicle rate signal (ϕ) through appropriate gain constants to form the combined system error signal $\epsilon(t)$:

$$\epsilon(t) = a_0 \psi(t) + a_1 \dot{\phi}(t) \qquad (3.2\text{-}2)$$

The inner block of the pseudo rate modulator in Figure 3.2-3 may be considered as an ON-OFF contactor, and regardless of the state of the system, the voltage to the ON-OFF contactor may be expressed as:

$$\epsilon_c(t) = \epsilon(t) + h(t) - V(t) \qquad (3.2\text{-}3)$$

Where $h(t)$ is the positive switching hysteresis and $V(t)$ is the voltage of the negative feedback lag network. For $|\epsilon_c| < |E_c|$, the contactor is OFF; for $|\epsilon_c| \geq |\epsilon_c|$, the contactor is ON. The polarity depends upon the polarity of ϵ_c. The system may be most easily understood by assuming that $\epsilon(t)$ is essentially constant or, at best, varies slowly with time during minim impulse limit cycle operation. At the time just prior to contactor actuation ($t = 0$), $\epsilon_c = \epsilon_c$ and Equation 3.2-3 becomes:

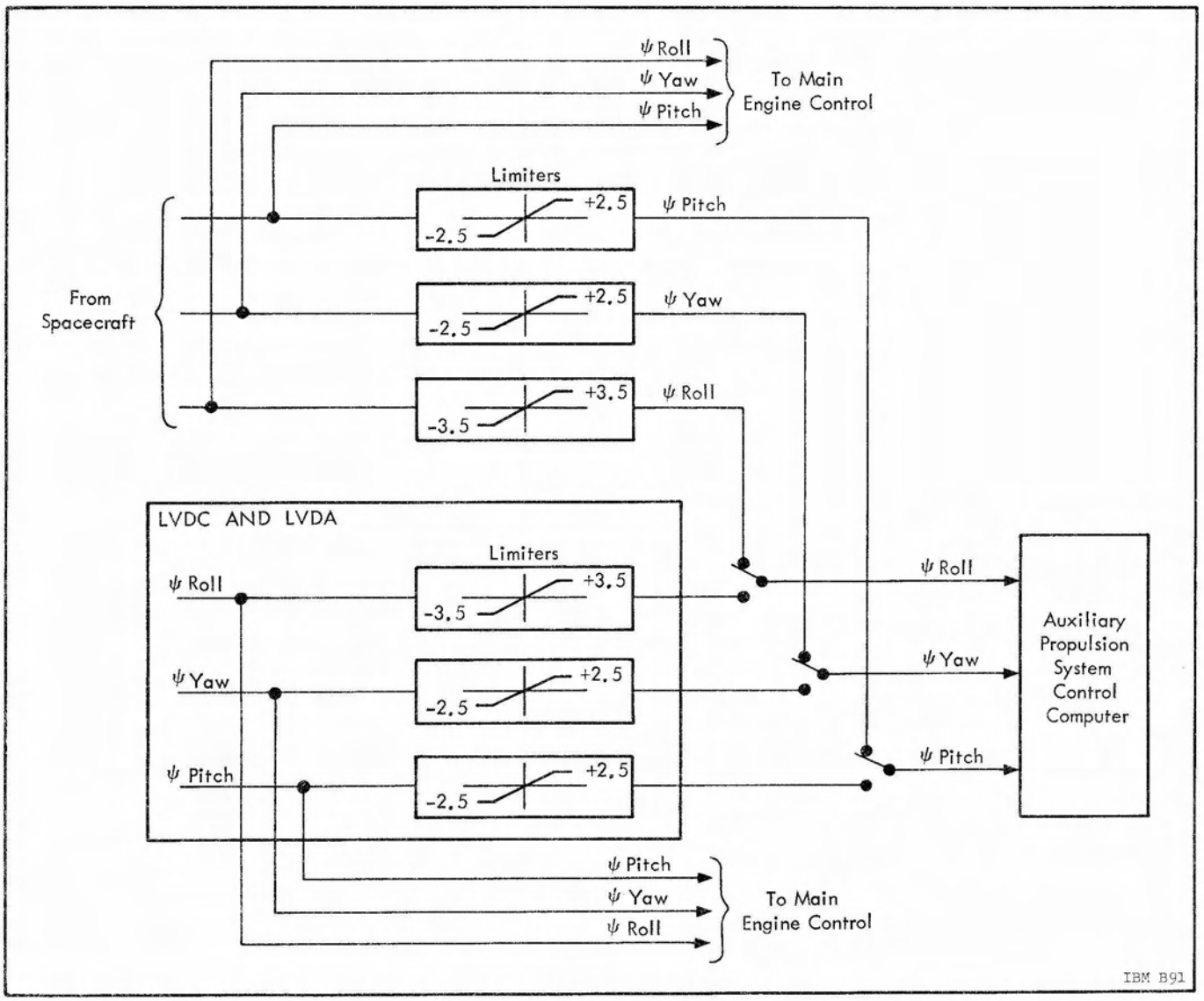


Figure 3.2-2 Attitude Error Signal Sources

$$\epsilon_c = \epsilon_o - V_o = E_c \qquad (3.2\text{-}4)$$

$$\text{or} \quad V_o = \epsilon_o - E_c \qquad (3.2\text{-}5)$$

V_o is the initial condition of V at t = 0. At the instant t = 0^+ (just after contactor actuation), V(t) and h may be expressed as

$$V(t) = K_f E_o - (K_f E_o - V_o)^{t/\tau_f} \qquad (3.2\text{-}6)$$

$$h = K_o E_o \qquad (3.2\text{-}7)$$

The contactor will remain energized until $t = t_1$ at which time $\epsilon_c(t) = E_c$. At the instant just prior to cutoff, substituting Equation 3.2-6 and 3.2-7 into Equation 3.2-3, we have:

$$\epsilon_c(t_1) = \epsilon_o + K_o E_o - \left[K_f E_o - (K_f E_o - V_o)^{-t_1/\tau_f}\right]$$

$$= E_c \qquad (3.2\text{-}8)$$

Using V_o as given by Equation 3.2-5, Equation 3.2-8 may be solved for t_1 to give:

$$t_1 = \tau_f \ln \left[\frac{K_f - \left(\frac{\epsilon_o - E_c}{E_o}\right)}{K_f - K_o - \left(\frac{\epsilon_o - E_c}{E_o}\right)} \right] \qquad (3.2\text{-}9)$$

Where:
$|\epsilon_o| \geq |E_c|$
ϵ_o = Constant

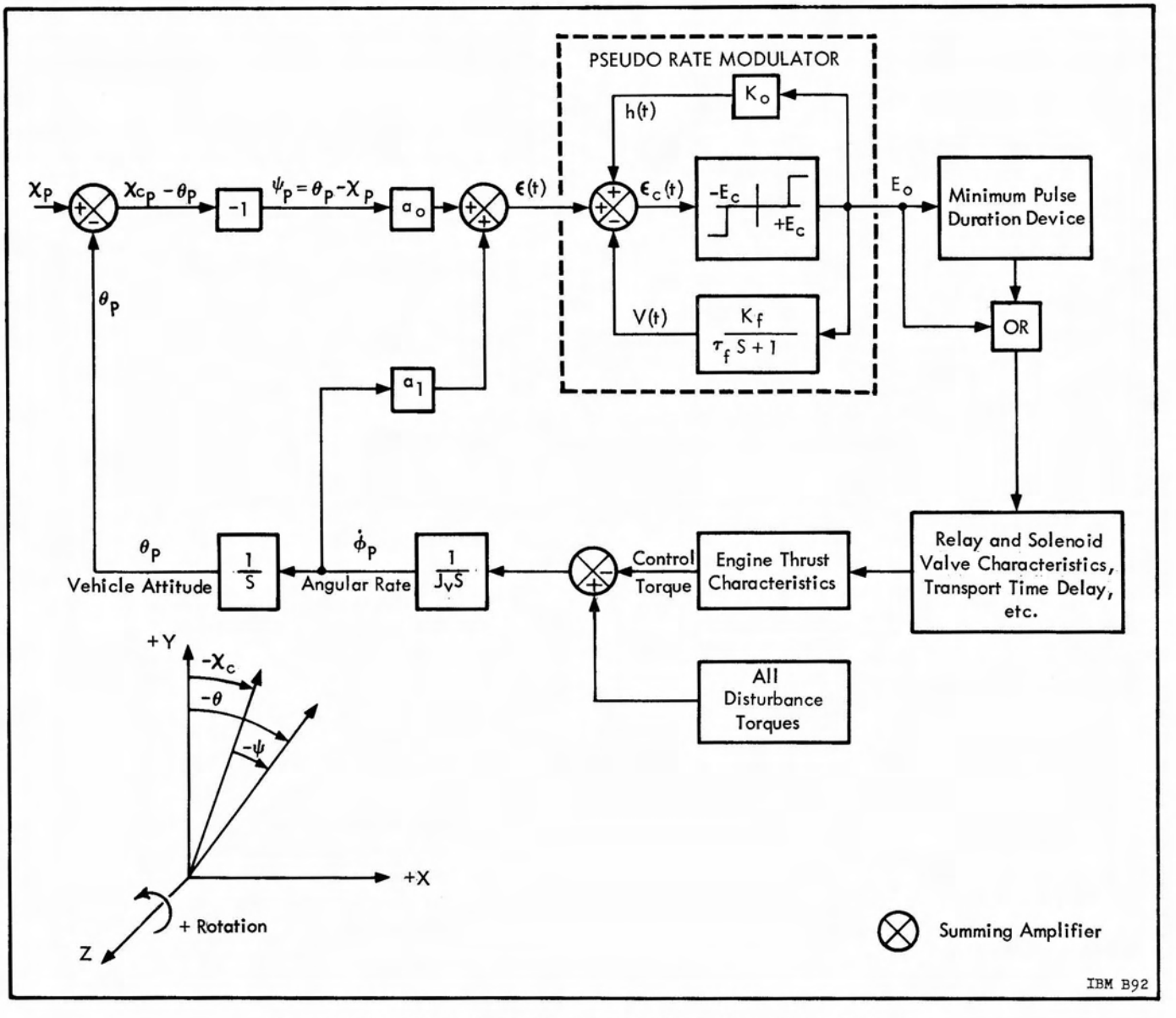


Figure 3.2-3 Pitch Channel of the Auxiliary Propulsion System

Equation 3.2-9 expresses (for steady - state operation) the contactor ON-time increment t_1. Equation 3.2-9 is solved for $\epsilon_o = E_c$ to give the expression for the minimum ON time ($t_1 = \Delta t$). This gives:

$$\Delta t = \tau_f \ln \left[\frac{K_f}{K_f - K_o} \right] \qquad (3.2\text{-}10)$$

The modulation range may also be determined from Equation 3.2-9 by noting that:

$$t_1 \rightarrow \infty \text{ as } \frac{\epsilon_o - E_c}{E_o} \rightarrow (K_f - K_o). \qquad (3.2\text{-}11)$$

Since Equation 3.2-11 shows the contactor to be continuously ON for this condition of input, the modulation range may be defined as:

$$0 \leq \frac{\epsilon_o - E_c}{E_o} \leq \left(K_f - K_o \right) \qquad (3.2\text{-}12)$$

In a development similar to that used for the ON-time increment t_1, the OFF-time increment t_2 may be obtained. The resulting relationship is:

$$t_2 = \tau_f \ln \left[\frac{\frac{\epsilon_o - E_c}{E_o} + K_o}{\frac{\epsilon_o - E_c}{E_o}} \right] \qquad (3.2\text{-}13)$$

In order to attain the desired pseudo rate modulation characteristics and to prevent reverse firing in the system, it is necessary to keep K_o/K_f small with respect to unity:

$$\left(K_f \right)_{max} \leq \frac{E_c}{E_o \left(1 + \frac{K_o}{K_f} \right)} \qquad (3.2\text{-}14)$$

The pseudo rate modulation system, over a certain range of input signals, is both pulse-width and pulse-rate modulated as a function of input signal level. Pseudo rate modulation has desirable characteristics of both modulation schemes. An additional characteristic of the feedback lag network (in the pseudo rate modulator) is that it adds a small amount of damping to the control system. This is a desirable and important consideration since the amount of damping is normally sufficient to maintain control system limit cycle operation in the event of a rate sensor failure.

Analog and digital computer studies have shown that near optimum fuel consumption, together with desired system accuracy characteristics, are obtained with the following system parameters:

Gain factor ..... $a_0 = 1$
Gain factor ..... $a_1 = 5$
Modulator limit ..... $E_c = 1^\circ$
Attitude error signal limits $\psi_{P_{Lim}}$ ..... = $\psi_{Y_{Lim}} = \pm 2.5^\circ$
Attitude error signal limits $\psi_{R_{Lim}}$ ..... $= \pm 3.5^\circ$
Minimum ON-time $\Delta t_{(min)}$ ..... = 0.065 second (corresponds to 7.5 # second minimum impulse per engine)
Modulation range ..... $\cong 0.6^\circ$

Phase-plane plots of the pitch, yaw, and roll deadbands (using the preceding parameters) are shown in Figures 3.2-4 and 3.2-5. By referring to Figures 3.2-2 and 3.2-5, it can be seen that the effect of limiting the attitude error signal is to limit the rate at which a large attitude error change can take place. The maximum output for the $\psi_{P_{Lim}}$ channel (independent of the ψ_P error) is ±2.5 degrees, and as soon as the vehicle rate builds up to ±0.3 degrees/second, the contactor "drops out" because

$$\epsilon_c = \pm 2.5^\circ \pm 5 \times .3^\circ \lesssim 1$$

The velocity increment ΔV (and thus the fuel) required for the system to settle out from a given disturbance would be excessive if it were not for

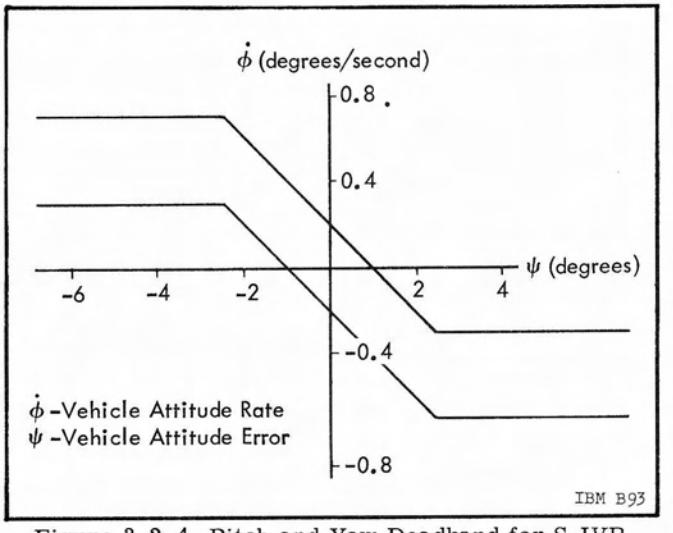


Figure 3.2-4 Pitch and Yaw Deadband for S-IVB Auxiliary Propulsion System

the velocity ledges shown in Figures 3.2-4 and 3.2-5. The settling-out time for a given disturbance is larger when using the imposed velocity ledges, but it is not critical.

Referring again to Figure 3.2-3, it is noted that the pseudo rate modulator output pulse E_0 is transmitted to a minimum pulse duration device and to an OR gate. As previously mentioned, the equation considered in developing and sizing the pseudo rate modulation system assumed an ϵ (t) that was essentially constant or varied slowly with time during minimum impulse limit cycle operation. This assumption was valid for pitch and yaw control but not roll. In the roll channel, the vehicle attitude rate response was sufficient in magnitude to cause the contactor to "drop out" earlier than desired. This, coupled with the fact that the engine specific impulse (I_{sp}) drops off rapidly for minimum pulses (less than approximately 60 milliseconds), made it necessary to insure that once the engines turn ON, they will stay ON for at least 65 milliseconds. The minimum pulse duration device guarantees this. The OR circuit passes the longer pulse whether it is from the minimum pulse duration device or directly out of the pseudo rate modulator.

The electrical pulse leaving the OR circuit energizes relay coils which transmit stage power to fuel and oxidizer solenoid valves of the commanded hypergolic engine.

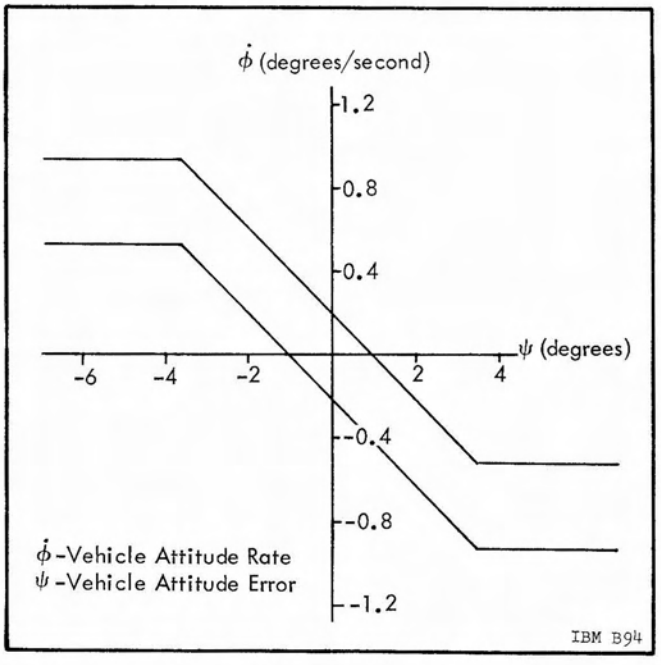


Figure 3.2-5 Roll Deadband for S-IVB Auxiliary Propulsion System

To this point, the discussion of the auxiliary propulsion system has been concerned with the pitch channel. The yaw and roll channels are similar in all details except that their combined error signals are mixed to ensure minimum fuel consumption. Figure 3.2-6 shows the pitch, yaw, and roll systems and in particular, the yaw-roll mixing scheme. As shown in the figures, the yaw-roll mixing scheme ensures that opposing engines will not fire simultaneously. The scheme also prevents one engine from adding to an error already existing in another channel.

The operation of the auxiliary propulsion system during coast phase is illustrated in Figure 3.2-7. The operation starts at point A, which represents a given attitude error (ψ) and attitude rate ($\dot{\phi}$) of the vehicle. The end state is the limit cycle within the deadband and about the commanded attitude angle.

The attitude error signals from the spacecraft may originate in the Apollo navigation, guidance, and control system or may be generated by the Astronaut through manual control. In any case, the limiters in the IU Flight Control Computer will limit the angular rate to 0.3 degree/second in pitch and yaw and 0.5 degree/second in roll. These limits prevent excessive propellant usage which would result from large angular rate commands while driving the vehicle to the desired attitude.

The Apollo Spacecraft attitude reference system can follow the instantaneous vehicle attitude. This is accomplished by driving the command display unit servo motor with an error signal which is formed by differencing the commanded and actual gimbal angles. When the Astronaut wishes to maintain a particular attitude orientation, he can use the computer to set the command display unit command resolver to the desired gimbal value. The difference between the commanded and actual gimbal angles results in an error signal which is resolved into vehicle coordinates and is given to the IU Flight Control Computer as an attitude error signal. The S-IVB attitude control system then operates in the limit-cycle mode about this command attitude. The introduction of an attitude deadband in the limit cycle scheme saves propellant which would otherwise be required to correct attitude errors smaller than the $\pm$ 1 degree deadband limits.

CONTROL RELAY PACKAGE

Each control relay package consists of 12 miniature, double-pole, double-throw relays. Two

such packages are used to control the S-IVB attitude control engine valve coils. These valve coils are an integral part of the engine and control the fuel and oxidizer poppet valves. The relays are driven in groups of eight from the three S-IVB attitude control spatial amplifiers in the Flight Control Computer. Figure 3.2-8 shows the arrangement of the relays, valve coils, and quad-redundant fuel and oxidizer poppet valves associated with 1 amplifier in the pitch or yaw axis.

As an example, if the attitude control requires nozzle I be turned ON, the spatial amplifier energizes coils K1 through K4, which closes the associated contacts (1, 1', etc). Valve coils 1, 1', etc., are energized and open fuel valves 1, 2, 3, and 4 and oxidizer valves 1' and 2', 3' and 4' in the quad valve network. This turns on nozzle I.

The control relay package was designed to take advantage of the redundant valve configuration by pro-

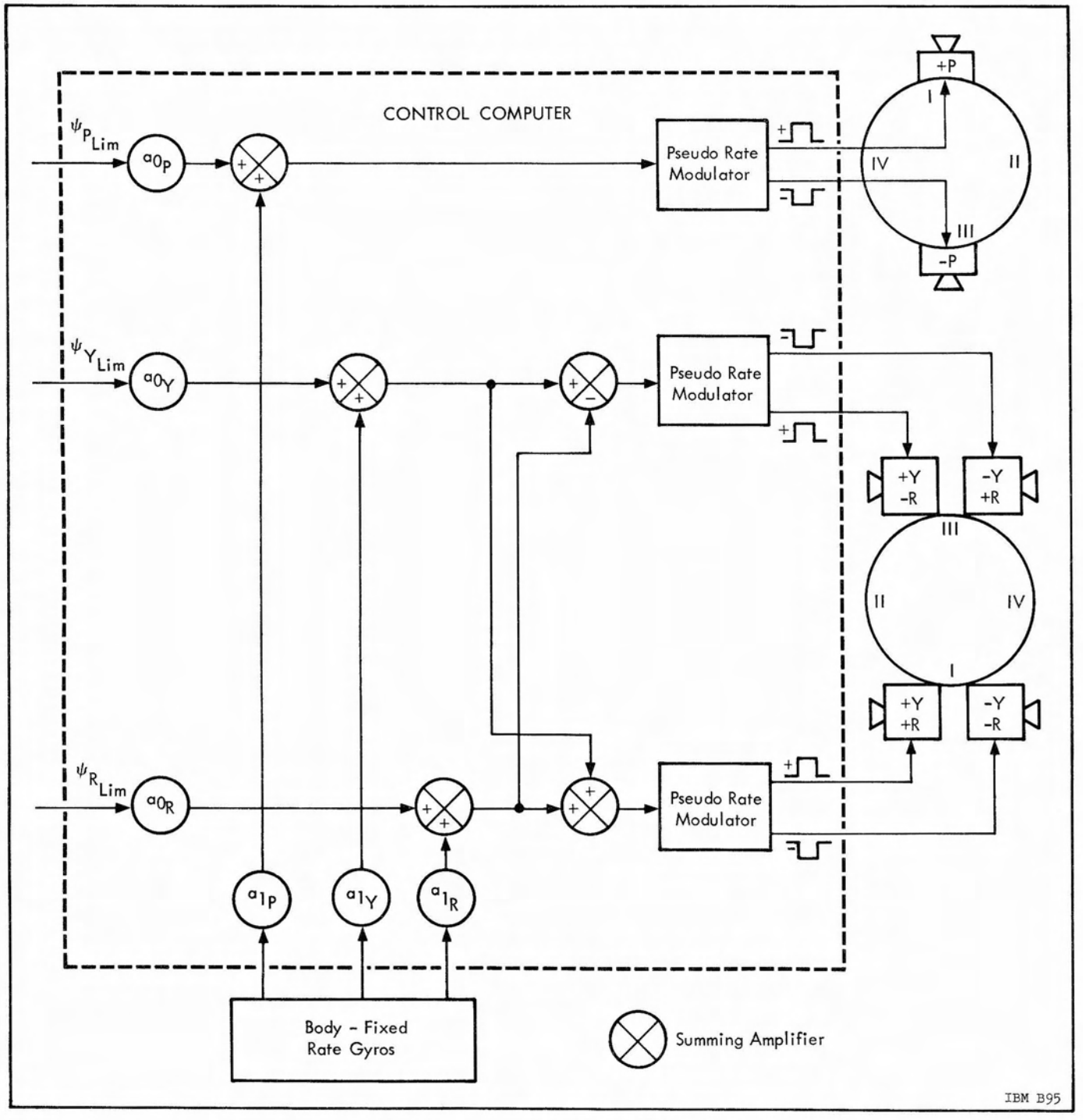


Figure 3.2-6 S-IVB Attitude Control System

viding failure isolation from the predominant modes of relay failure (open-circuited coils, failure-to-make contacts, and welded contacts). This relay redundancy can be shown by considering relay 1 as an example. When relay coil K1 is energized, it closes contacts 1 and 1' which causes fuel valve 1 and oxidizer valve 1' to be open. An open in coil K1 or a failure of contacts 1 and 1' to close results in no operation of fuel valve 1 and oxidizer valve 1'. However, this does not cause a failure of the attitude control system, since the quad-redundant valves provide an operative flow path through valves 2, 4 and 2', and 4'. If, on the other hand, either or both sets of contacts of relay 1 should weld, or otherwise become permanently closed, fuel valve 1 and oxidizer valve 1' would be open. However, control of fuel and oxidizer would be maintained by valves 3 and 3' respectively.

Reliability predictions have shown that 85 percent of relay coil failures are due to an open coil, and 93 percent of contact failures are due to failure to close. The design of the control relay package isolates the control system from these predominate failures, as well as welded contacts.

The control relay package was introduced into the design of the S-IVB attitude control system to improve the interstage cabling design between the IU Flight Control Computer and the S-IVB valve coils by reducing the current requirements from 12 amperes to 200 milliamperes. Therefore, the control relay package saves about 100 pounds of cabling and reduces the Flight Control Computer spatial amplifier's power requirements by switching the power to the valve coils in the S-IVB Stage.

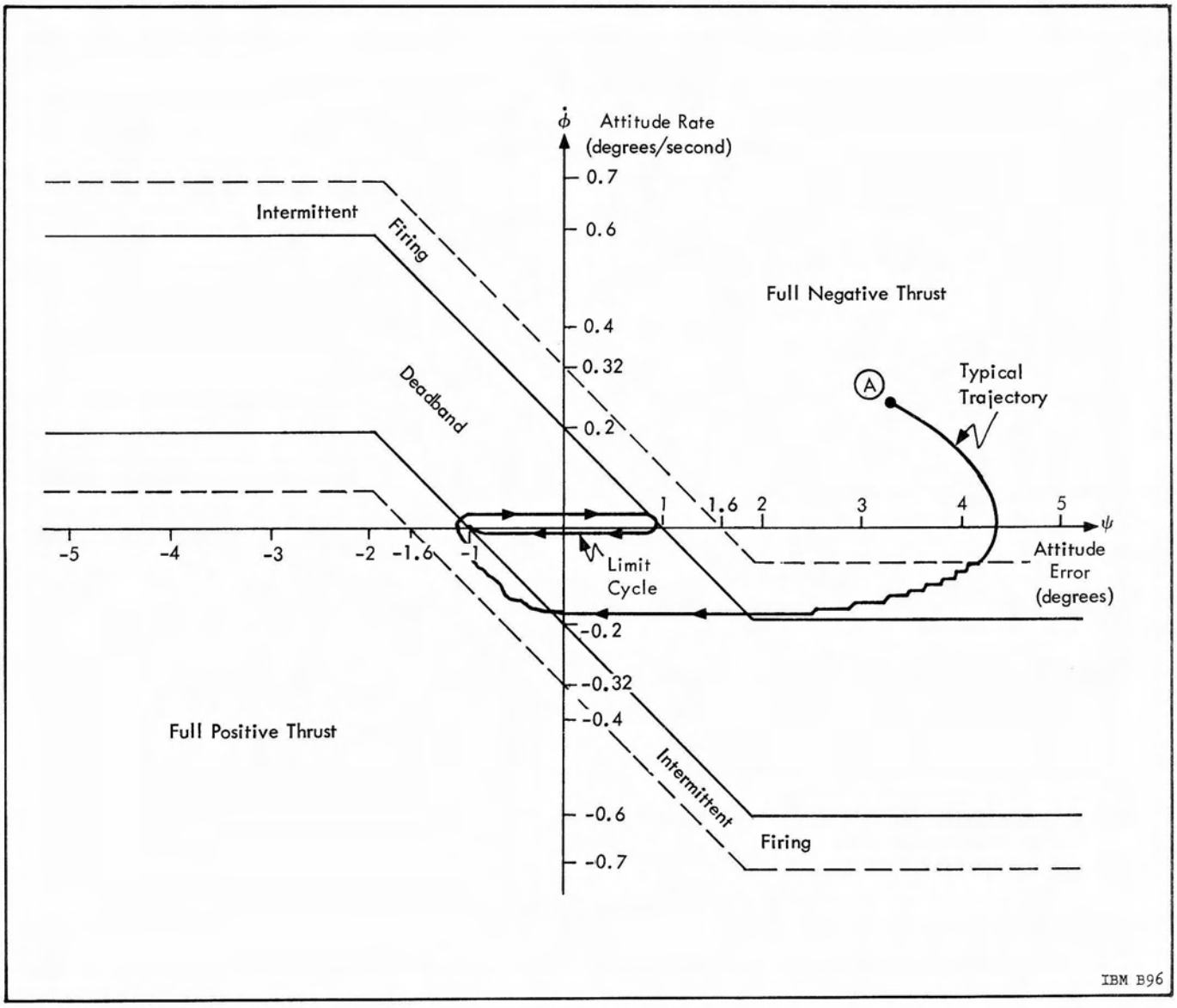


Figure 3.2-7 Deadbands of Attitude Control System

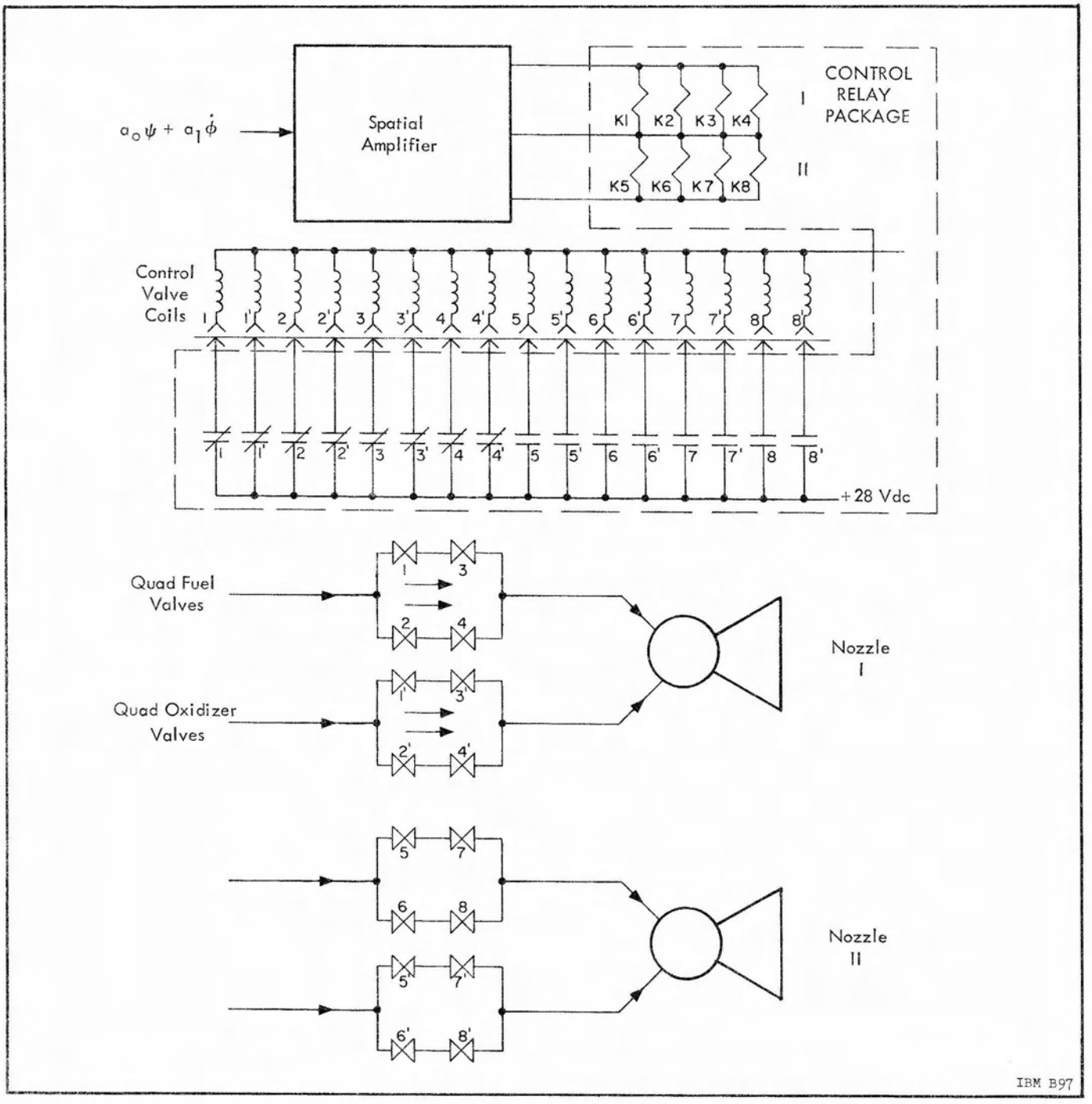


Figure 3.2-8 Relay Control Unit and Quad Redundant Valves

SECTION 3.3

CONTROL SENSORS

3.3.1 RATE GYROS

Single degree of freedom rate gyros are used on the Saturn Vehicles to sense the angular rate of movement of the vehicles about the roll, yaw, and pitch axes. The same type of rate gyros are employed in two separate packages, the Control-EDS Rate Gyro package and the Control Rate Gyro package. The Control-EDS Rate Gyro package is located in the IU on the Saturn IB and V Vehicles. It is used for attitude control and EDS operation. The location of the Control Rate Gyro package, and whether it will be used, depends on further studies of the vehicle bending characteristics.

The rate gyro (Figure 3.3-1) uses a microsyn differential transformer pickoff which is coupled to

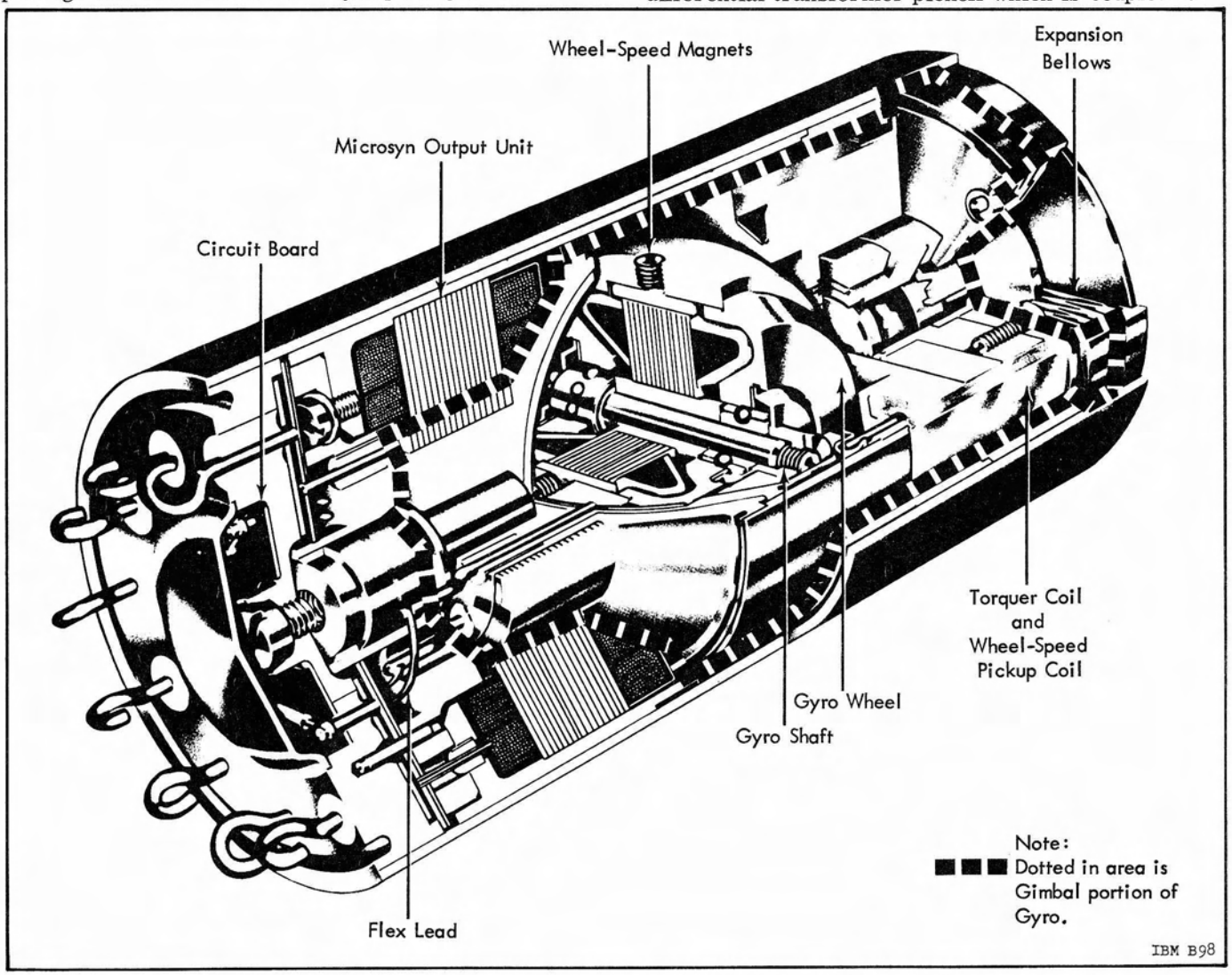


Figure 3.3-1 Cutaway View of a Self-Test Rate Gyro

the gimbal. Angular rate about the input axis of the rate gyro will be translated to an ac voltage output signal from the microsyn. The amplitude of this signal has a definite relationship to the angular rate. This relationship, called the scale factor, is approximately 200 mV rms per degree/second. The rate gyro has the capability of sensing angular rates to 20 degrees/second in either counter-clockwise or clockwise direction.

Each rate gyro is equipped with self-checking capabilities. A self contained electro-magnetic coil can be remotely excited to cause the rate gyro gimbal to be deflected. This deflection provides an output from the microsyn without subjecting the gyro at a rate input. A built-in generator, integral with the gyro rotor, provides ac pulses (the frequency is the indication of the gyro rotor speed).

The rate gyros are fluid-damped devices which maintain a relatively constant damping factor over the range of temperatures in which the damping fluid retains its fluid characteristics. When the gyros are employed in low-temperature environments which exceed the gyro ratings (such as will be found in several locations of the Control Gyro package), the package must be supplied with heaters to ensure proper operation.

3.3.2 CONTROL-EDS RATE GYRO PACKAGE

The Control-EDS Rate Gyro (Figure 3. 3-2) contains nine rate gyros arranged in a triple redundant configuration (Figure 3. 3-3). Each group of three rate gyros provides output signals for angular rate about the pitch axis ($\dot{\phi}_p$), yaw axis ($\dot{\phi}_y$), and roll axis ($\dot{\phi}_r$). Each group of gyros is completely independent of the two other groups. Thus, there are nine separate output signals — one from each gyro. The comparison and selection of the output signals are accomplished in the Control Signal Processor.

Each of the gyro groups receives 400 Hz, single-phase power from a separate power supply.

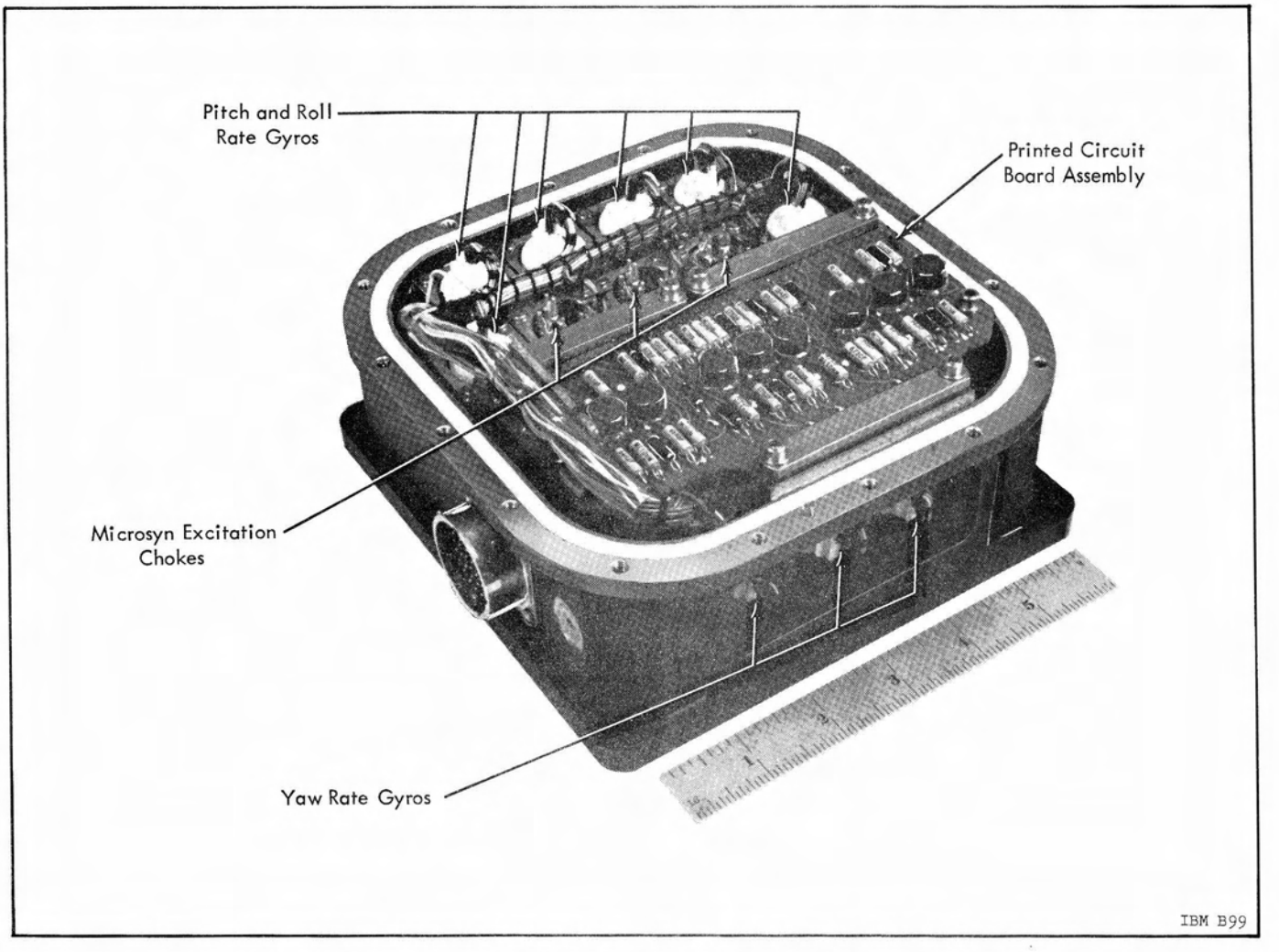


Figure 3. 3-2 Control - EDS Rate Gyro Package with Covers Removed

These supplies are located in the Control Signal Processor.

This triple redundant configuration increases the reliability for the Control-EDS Rate Gyro package which is used throughout the mission (as compared to the Control Rate Gyros, used only during the early phases of the flight).

3.3.3 CONTROL SIGNAL PROCESSOR

The Control Signal Processor converts the ac rate gyro signals into dc signals required as inputs to the Flight Control Computer. It also compares and selects output signals from corresponding redundant rate gyros. A block diagram of the Control Signal Processor is given in Figure 3.3-4.

The 400 Hz output signal from each rate gyro is demodulated to generate a dc voltage which is proportional to the rate output of the gyro. A telemetry output from each demodulator is provided.

Two of the three demodulated outputs (of one channel) are compared within a comparison circuit, and switching logic selects a good demodulator output. The dc outputs (0 - 45 volts) of each channel are used as inputs to the Flight Control Computer. When the dc output of the two compared demodulators differs by a preset amount, a relay selects the output of the spare demodulator as the input to the Flight Control Computer. The relay remains in this position until reset by an external command signal. Closure of the relay is indicated by a telemetry output.

Each rate switch receives the 400 Hz output signal from one gyro and energizes a relay when the amplitude of the signal exceeds the predetermined magnitude. This relay generates an EDS signal which is indicated by the telemetry.

The angular velocities of the gyro rotors are measured by wheel speed sensor circuits which provide outputs to ESE and telemetry for monitoring purposes. The input signals to the speed sensor is a frequency

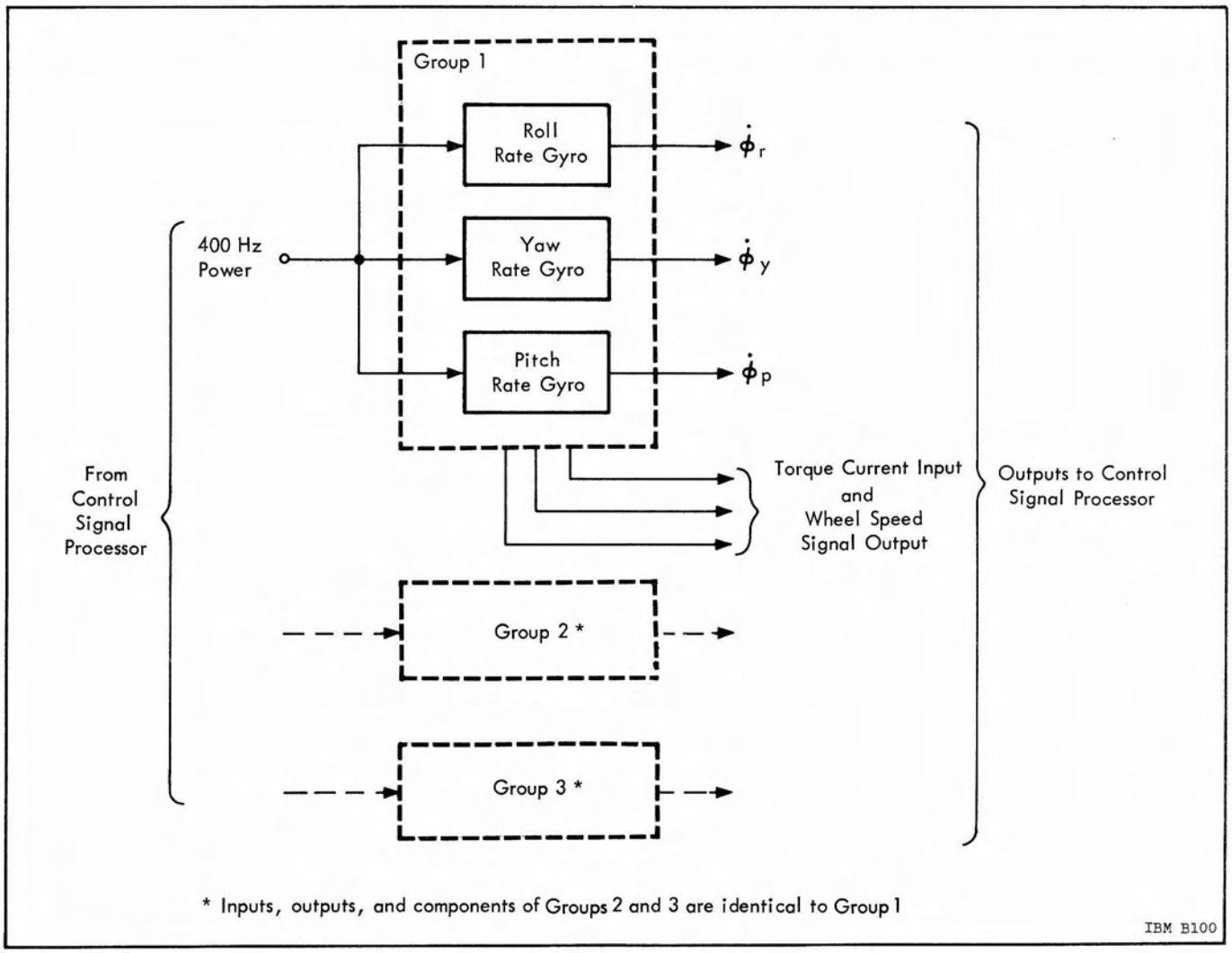


Figure 3.3-3 Control - EDS Rate Gyro Block Diagram

which is proportional to the angular velocity of the gyro rotor. If the frequency of any one input deviates more than ± 50 Hz, the wheel speed sensor will generate a discrete signal for ESE and telemetry indicating gyro overspeed or underspeed conditions. Output signals to the EDS are provided if any of the rate gyro outputs exceed a predetermined value.

The Control Signal Processor contains three power supplies operating from three separate 28-volt batteries. Each power supply provides 60 Vdc for one roll, yaw, and pitch demodulator, and 28 Vdc for the comparison circuit and one roll, yaw, and pitch rate switch.

Three static inverters, also located in the Control Signal Processor, operate from unregulated battery power to generate closely regulated 26 Vac (400 Hz) signals. Each inverter provides motor and microsyn power to one roll, yaw, and pitch rate gyro, and a reference excitation to one roll, yaw, and pitch demodulator.

Since the Control-EDS Rate Gyro package is located on an IU cold plate, it will be maintained at a temperature which will not require the use of heaters within the package.

3.3.4 CONTROL RATE GYRO PACKAGE

The Control Rate Gyro package contains three rate gyros, an inverter, power supply, and electronics. The rate gyros are oriented to sense angular rates about the roll, yaw, and pitch axes.

As indicated in Figure 3.3-5, the Control Rate Gyro package includes a single inverter which supplies the 400 Hz power for gyro spin motor and microsyn excitation. An additional power supply generates the dc voltages required by the demodulators, amplifiers, and wheel speed-sensing circuits. The amplifiers and demodulators convert the ac output of the microsyn to a dc signal with a scale factor of 1 volt per degree/second. The polarity of the dc output depends upon the sign of the input angular rate. These dc signals are directed to the Flight Control Computer. The wheel speed sensing circuit receives the pulses from the gyro speed signal generators and detects deviations from the desired gyro rotor speed which is indicated by a signal frequency of 1600 Hz. When the deviation in frequency exceeds a certain magnitude (in any direction), a telemetry signal will be generated.

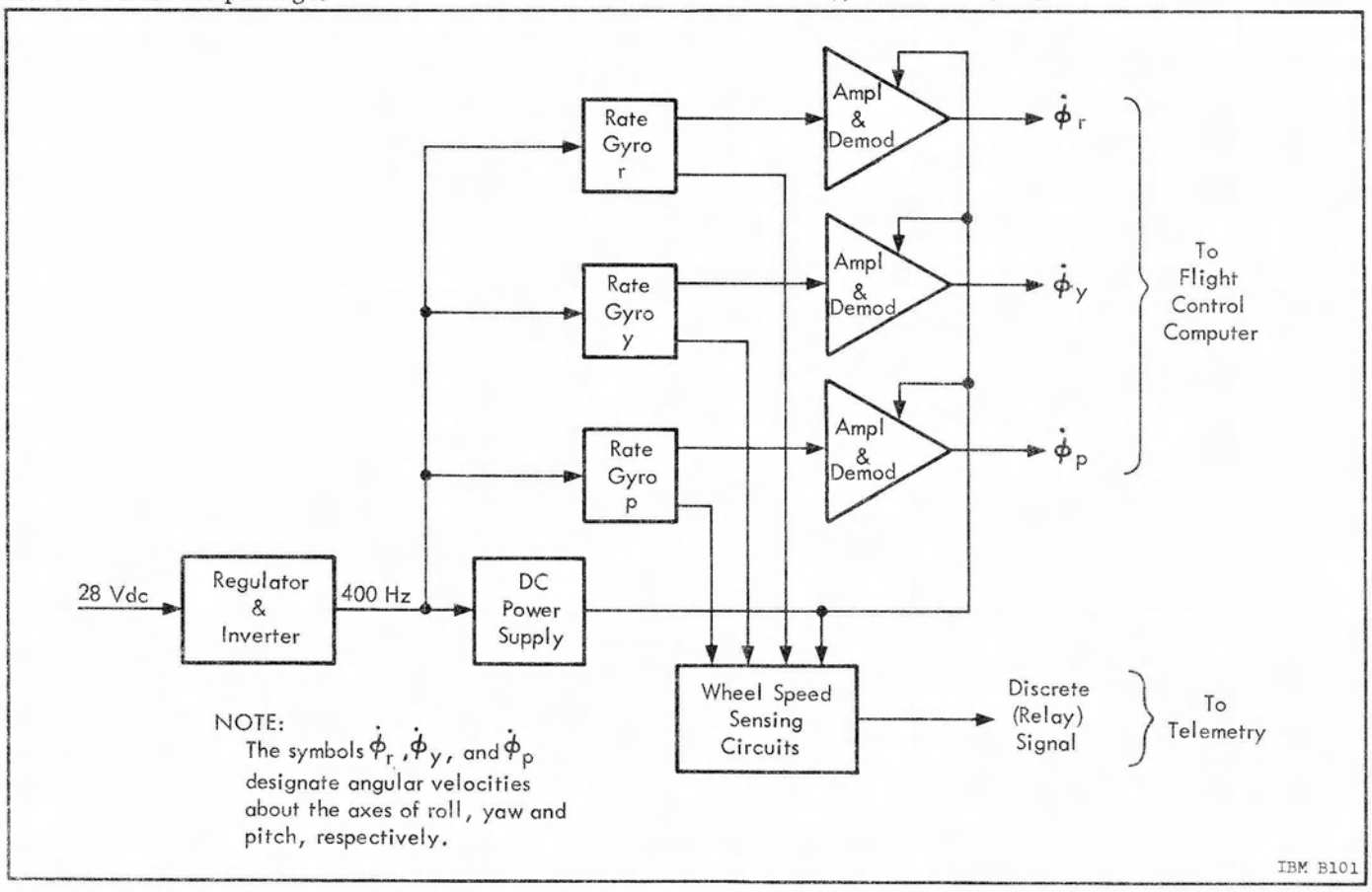


Figure 3.3-5 Control Rate Gyro Block Diagram

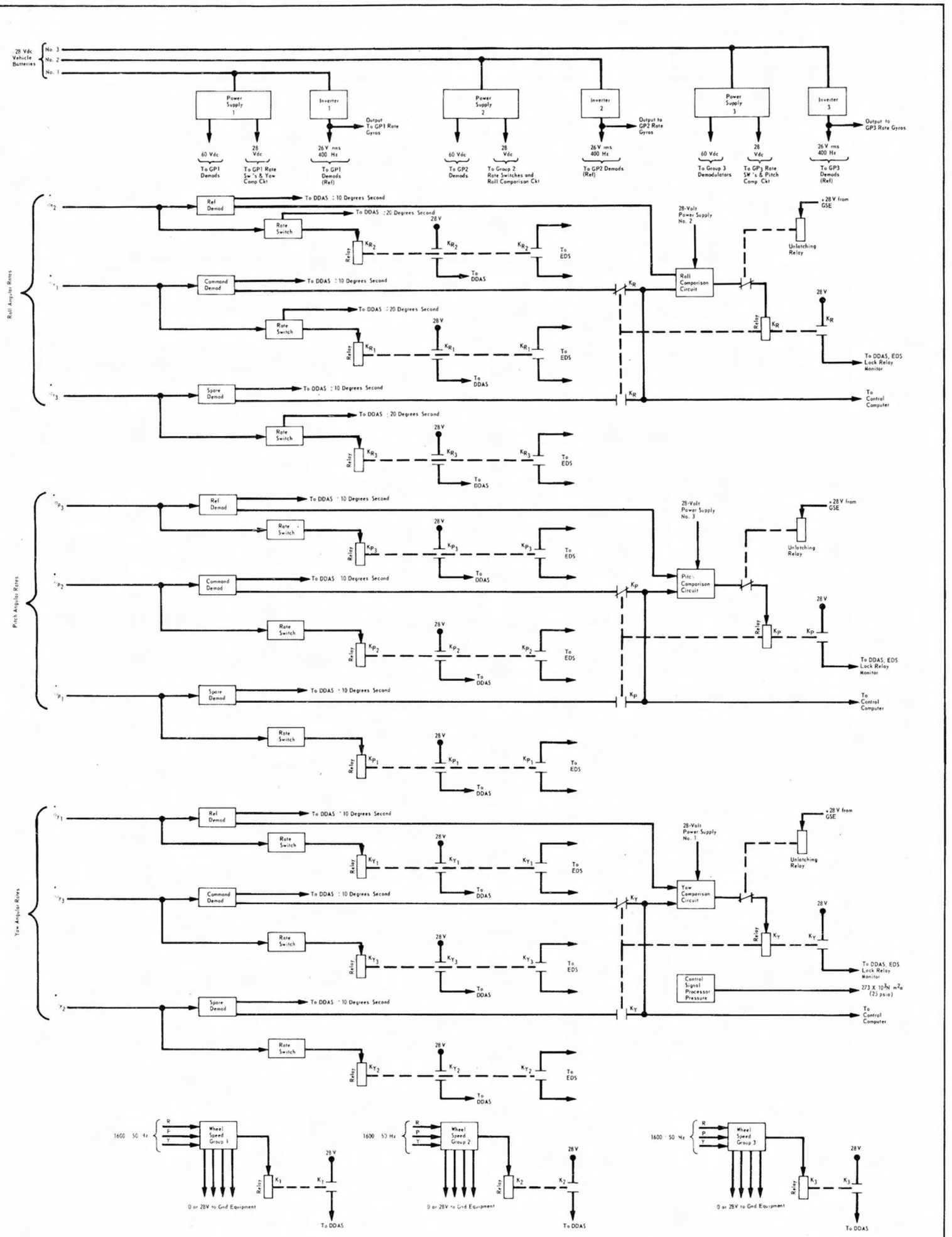


Figure 3.3-4 Control Signal Processor Block Diagram

3.3.5 CONTROL ACCELEROMETER

Two Control Accelerometers are used on the Saturn Vehicles to sense the lateral acceleration of the vehicle perpendicular to its longitudinal axis in the pitch and yaw planes. The output of these instruments is used in the control system to reduce structural loading and to control vehicle deflection due to the lateral winds.

The Control Accelerometer is a linear, spring-mass, fluid damped system with an inductive pickoff. Its excitation is from a self-contained static inverter which converts the 28-volt dc input voltage to a 400-cycle ac voltage (see Figure 3.3-6). The ac output of this sensor is proportional to the applied acceleration in its sensitive axis. This signal is then amplified and demodulated within the assembly to produce a dc output voltage proportional to acceleration. This output is fed to the Flight Control Computer.

The heart of the accelerometer is its spring-mass system. The seismic mass is supported and restrained by a non-pendulous spring suspension system. The springs constrain the mass to pure translational motion with practically no friction and provide extremely low cross-axis sensitivity at the same time.

The spring-mass system is fluid dampened with a silicone fluid. As the accelerometer is subjected to acceleration, the mass moves with respect to the case and causes a positive displacement of the fluid with a resultant damping action. In addition to this effect, the damping fluid provides resistance to shock and vibration. A change in fluid volume with any temperature change is compensated for by an internal bellows.

A special feature of these accelerometers is their self-checking capability. By exciting a separate electro-magnetic coil, it is possible to deflect the seismic mass a calibrated amount and thus check the electrical output of the instrument without subjecting it to acceleration. This provides a means of remotely checking the accelerometers after their installation on the vehicle to assure proper operation before flight. Table 3.3-1 lists the accelerometer characteristics.

Table 3.3-1 Control Accelerometer Characteristics

Measuring range	± 10 ms^{-2}
Natural frequency	9 Hz
Damping ratio	0.8 $\pm$ 0.2 of critical
Cross axis sensitivity	0.002 g/g
Scale factor	1.0 V/ms^{-2}
Power	10 watts

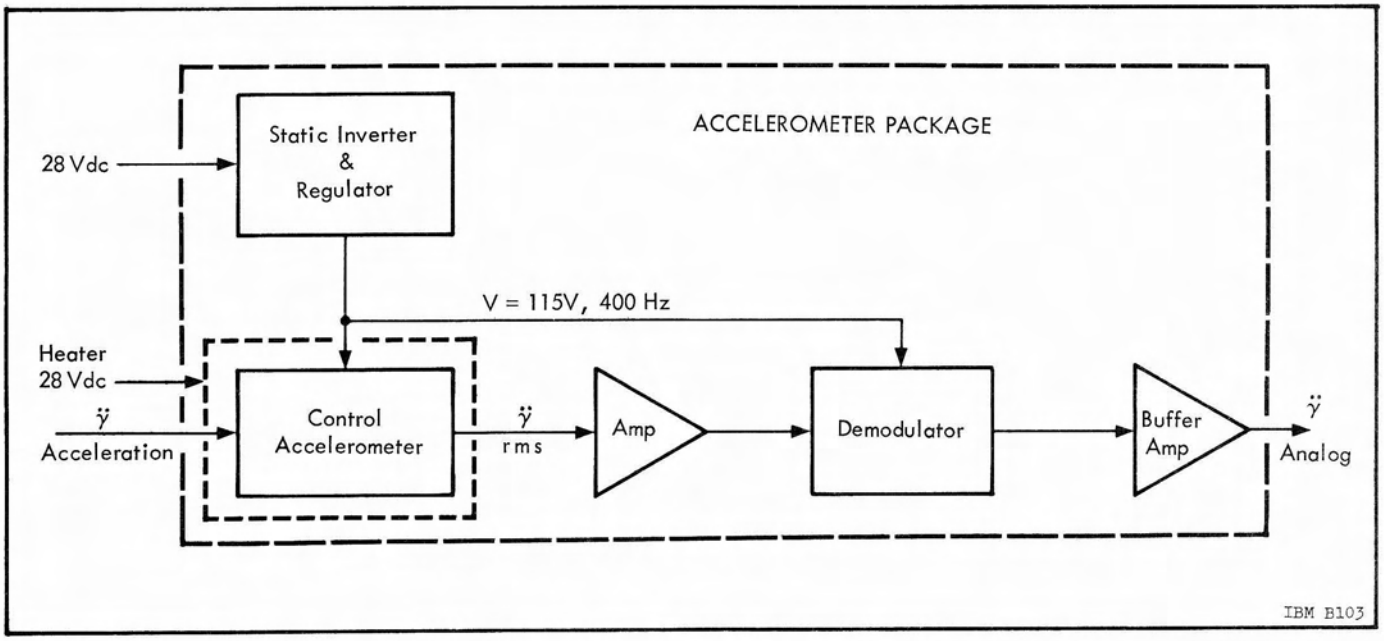


Figure 3.3-6 Accelerometer Block Diagram

SECTION 3.4

FLIGHT CONTROL COMPUTER

3.4.1 GENERAL

The Flight Control Computer is an analog device which generates the proper control commands for the engine actuators and the S-IVB auxiliary propulsion system. The computer accomplishes this by processing and combining the analog signals from the LVDA, control sensors, and Apollo Spacecraft.

The Flight Control Computer is equipped with eight input channels to accept eight different control signals listed in Table 3.4-1. The essential elements of the Flight Control Computer (for powered flight operation) are shown in the simplified block diagram, Figure 3.4-1. The scaling amplifiers provide the proper time variable adjustment of the gain factors ($a_0 a_1 g_2$) during flight. The filters shape the control signals to achieve phase and gain stabilization. Proper adjustment of the signal amplitude is accomplished by scaling resistors.

The processed signals are then summed and the resulting signals are amplified by a servo amplifier. These signals are the control signals for the engine servo actuators which control the thrust vector deflection angle (β).

The Flight Control Computer also generates the control signals for operation of the S-IVB auxiliary propulsion system which provides roll control during S-IVB powered flight and complete attitude control during coast flight. A simplified diagram of the

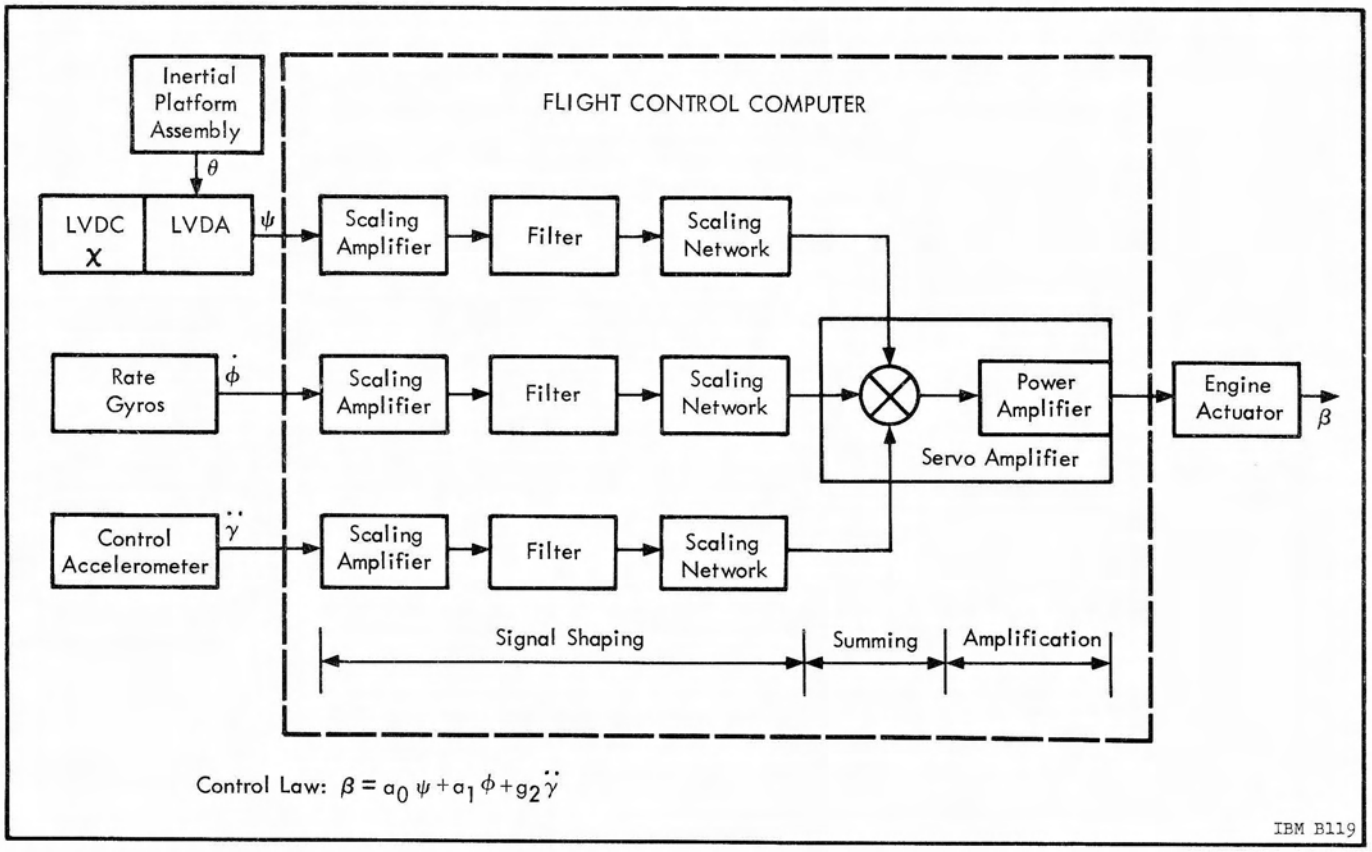


Figure 3.4-1 Simplified Diagram of the Flight Control Computer for Powered Flight Operation

Flight Control Computer configuration during coast flight is given in Figure 3.4-2. The attitude error signal (ψ) is provided by the LVDA or the Apollo Spacecraft. Signals from the spacecraft are limited in the Flight Control Computer while the signals supplied by the LVDA have been limited in the LVDC/LVDA. Angular rate signals ($\dot{\phi}$) are obtained from the Control - EDS Rate Gyros in the IU. The scaling amplifiers provide the proper adjustment of the signal amplitudes before the ψ and $\dot{\phi}$ signals are summed in the spatial amplifiers. The pseude rate modulator generates the control signals (ON-OFF) for the auxiliary propulsion system attitude control engines.

The Saturn V and the Saturn IB Flight Control Computers are designed according to the same general scheme. The configurations of both computers, however, are somewhat different for the powered flight phases since the Saturn V is a 3-stage vehicle while Saturn IB is a 2-stage vehicle. See paragraph 3.4.2. Both types of computers have the same configuration for S-IVB powered flight attitude control and coast flight attitude control.

Table 3.4-1 Input Signals to the Flight Control Computer

Input Signals		Symbol	From
Attitude Angle Error	Pitch	ψ_p	LVDA or Spacecraft
	Yaw	ψ_y	
	Roll	ψ_r	
Angular Rate	Pitch	$\dot{\phi}_p$	Rate Gyros (launch vehicle)
	Roll	$\dot{\phi}_r$	
	Yaw	$\dot{\phi}_y$	
Lateral Acceleration	Pitch	$\ddot{\gamma}_p$	Control Accelerometer (launch vehicle)
	Yaw	$\ddot{\gamma}_y$	

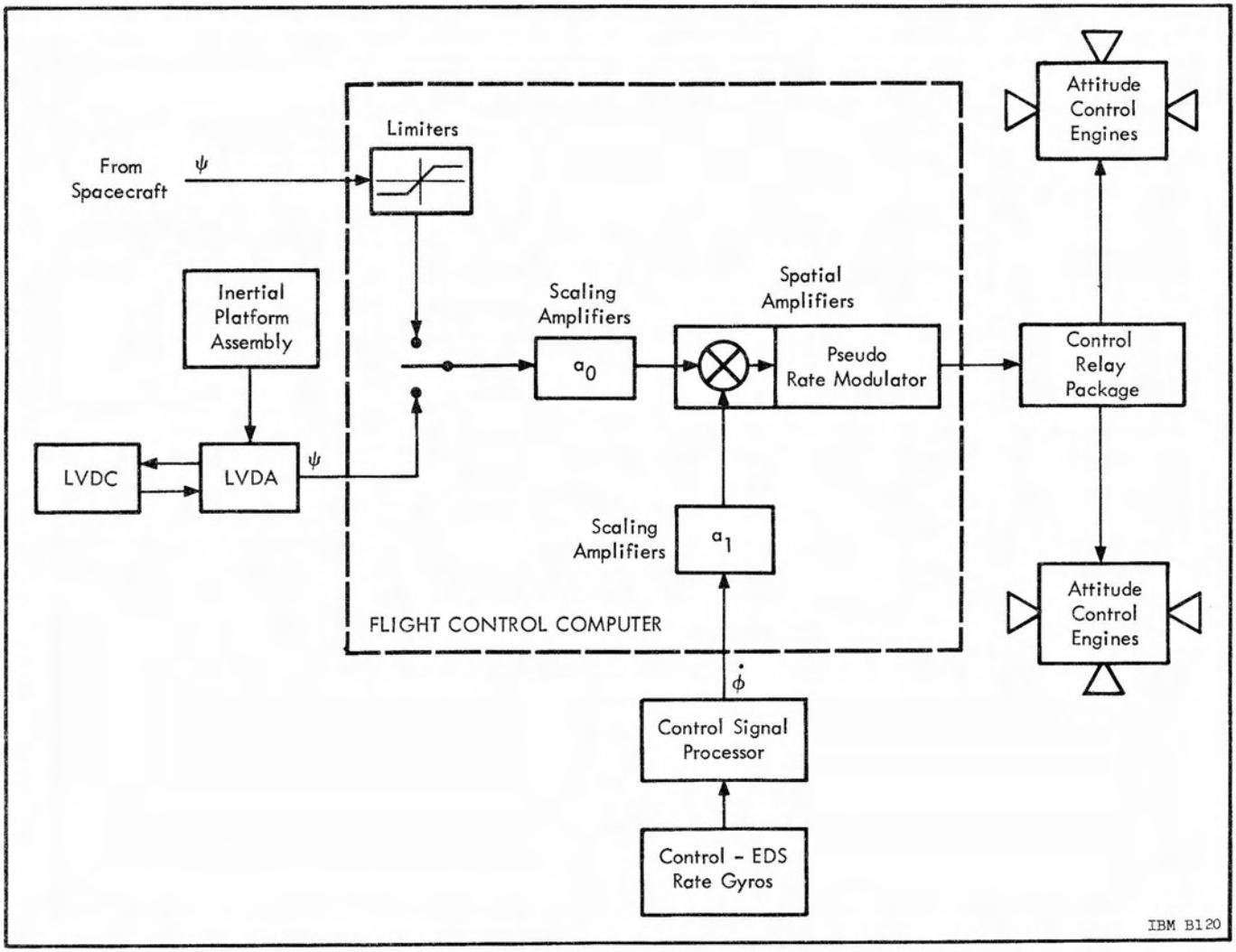


Figure 3.4-2 Simplified Diagram of Flight Control Computer APS Control

3.4.2 FLIGHT CONTROL COMPUTER OPERATION DURING POWERED FLIGHT

The Saturn IB Flight Control Computer differs from the Saturn V Flight Control Computer in several areas.

The Saturn IB Flight Control Computer contains a channel for Control Accelerometer signals (for first-stage powered flight). One type of servo amplifier is used to control the engine actuators of the S-IB Stage. Another type of servo amplifier (the same used in Saturn V) controls the S-IVB engine actuators. The engine actuator control loops for the S-IB Stage use electrical feedback. The computer contains amplifiers, filters, and the necessary switching devices for two vehicle stages.

The Saturn V Flight Control Computer has no channels for Control Accelerometer signals. The same type of servo amplifier is used to control the engine actuators in each stage (S-IC, S-II, and S-IVB). The computer contains amplifiers, filters, and the corresponding switching relays for three vehicle stages. The control loops for the engine actuators use mechanical feedback.

SATURN IB FLIGHT CONTROL COMPUTER

Figure 3.4-3 is a block diagram of the Saturn IB Flight Control Computer. During first-stage powered flight, each input signal to the computer passes through a dc amplifier, an attenuator, and a filter before it enters the servo amplifiers.

The attenuators are of 2 types, motor-driven cam-controlled potentiometers called control attenuation timers and relay-switched, fixed resistor networks. The control attenuation timers can provide attenuation that varies continuously as a function of time, while the relay-switched resistor networks change attenuation in discrete steps at predetermined time intervals.

A typical time program for a_0, a_1, and g_2 is shown in Figure 3.4-4. The gain factor (g_2) has a maximum value during the time period of high aerodynamic pressure, thus emphasizing the lateral acceleration control signals. These Control Accelerometer signals are used during the S-IB flight phase only.

In the C. A. T. device, a rocker arm drives two coupled potentiometers which are electrically connected to the appropriate channels. The outputs

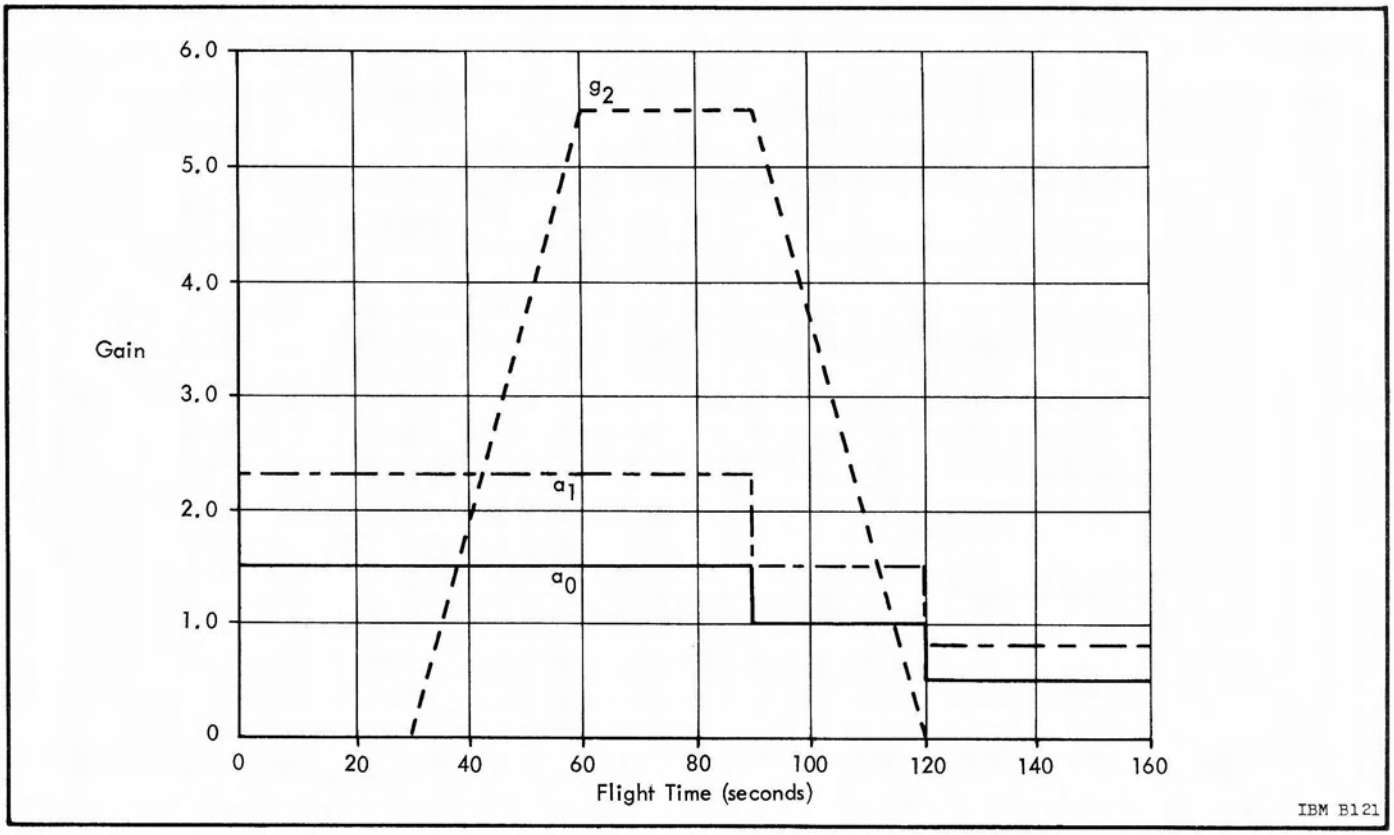


Figure 3.4-4 Typical Gain Program for a_0, a_1, g_2 Coefficients

from the potentiometers are time-varying functions of the input signals; i.e., the $\ddot{\gamma}$ signal inputs to the attenuator appear at the attenuator output modified by g_2. The cam is driven by a 115V, 400-cycle, single-phase, synchronous motor. The cam speed is determined by a gear train arrangement.

The gain coefficients (g_2) for Control Accelerometer signals are varied by a C. A. T. The other gain factors (a_0 and a_1) may be changed by a C. A. T. or in steps by relay switching of resistors. The relays are commanded by signals from the LVDC/LVDA.

The filters are passive RLC networks which provide gain and phase stabilization in the control loop to prevent undesirable signal frequencies from affecting the attitude control. The filter blocks shown in Figure 3.4-3 also contain the scaling resistor networks.

A different set of attenuators and filters is used during the S-IVB powered flight phases since the dynamic characteristic of the vehicle is changed after separation of the S-IB Stage and aerodynamic forces no longer exist. The required filters for each stage are selected by relays according to the flight program. No filters are used for operation of the S-IVB auxiliary propulsion system (during coast flight and for roll control during powered flight).

The servo amplifiers (Figure 3.4-5) are magnetic amplifiers which sum and amplify the filtered and scaled control signals to generate the control signals for the engine actuators. Differential integrating amplifiers provide high dc gain and attenuation of ripple. The output stage of the integrating amplifier is a low-impedance differential driver which can provide up to 12 milliamperes (S-IB) or 50 milliamperes (S-IVB) of current to the torque motor-operated control valve of each hydraulic servo actuator. A portion of this output current is returned through a feedback network to provide required accuracy in gain and linearity.

The Flight Control Computer contains eight servo amplifiers for the actuators of the S-IB Stage and six servo amplifiers for the actuators of the S-IVB Stage.

There is one servo amplifier for each engine actuator in the S-IB Stage; i.e., four pitch servo amplifiers and four yaw servo amplifiers. The three yaw output control signals (ψ_y $\dot{\phi}_y$ $\ddot{\gamma}_y$) to the Flight Control Computer are fed into each of the four yaw amplifiers. Correspondingly, the three pitch input channels are connected to each of the four pitch amplifiers. The two roll input signals (ψ_r and $\dot{\phi}_r$) are sent to all eight S-IB servo amplifiers since it is necessary to deflect the engines in pitch and yaw simultaneously for execution of a roll maneuver.

The six servo amplifiers for the S-IVB powered flight are used in a triple redundant configuration to control the two servo actuators of the single J-2 engine.

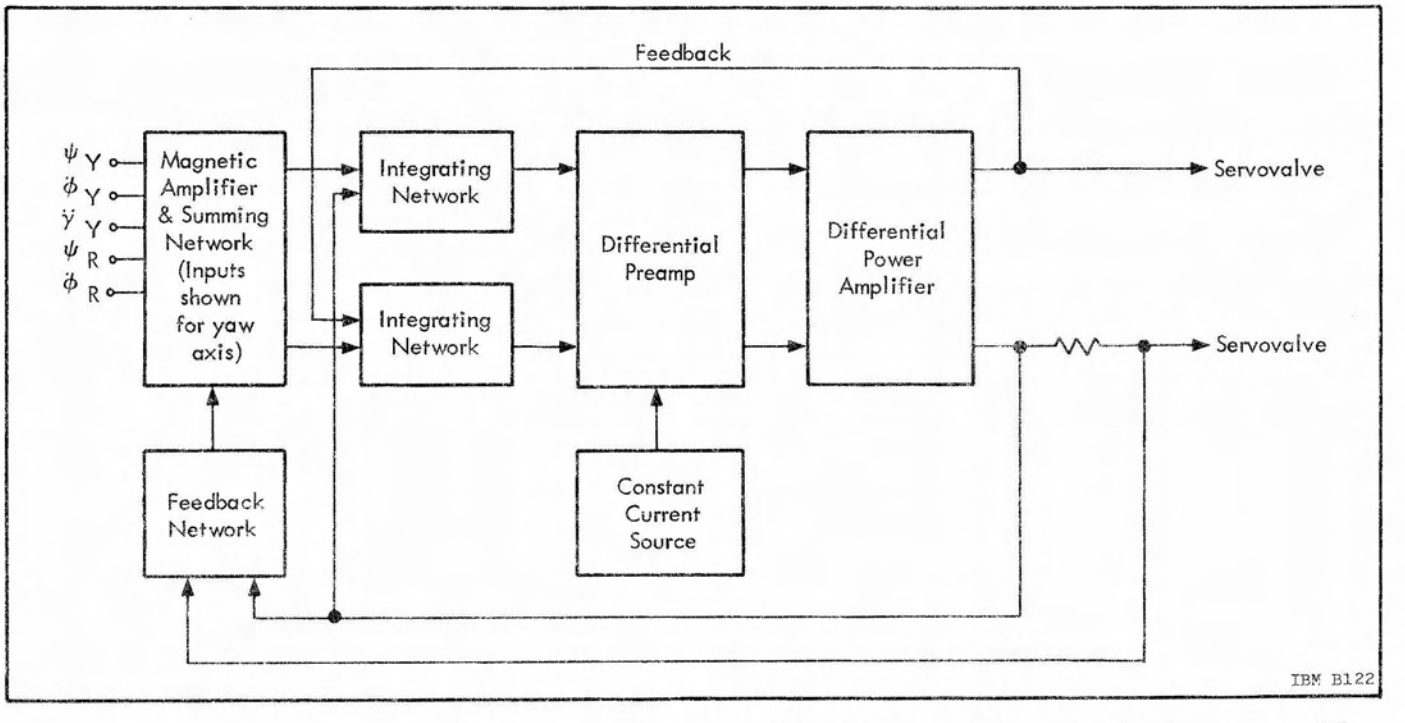
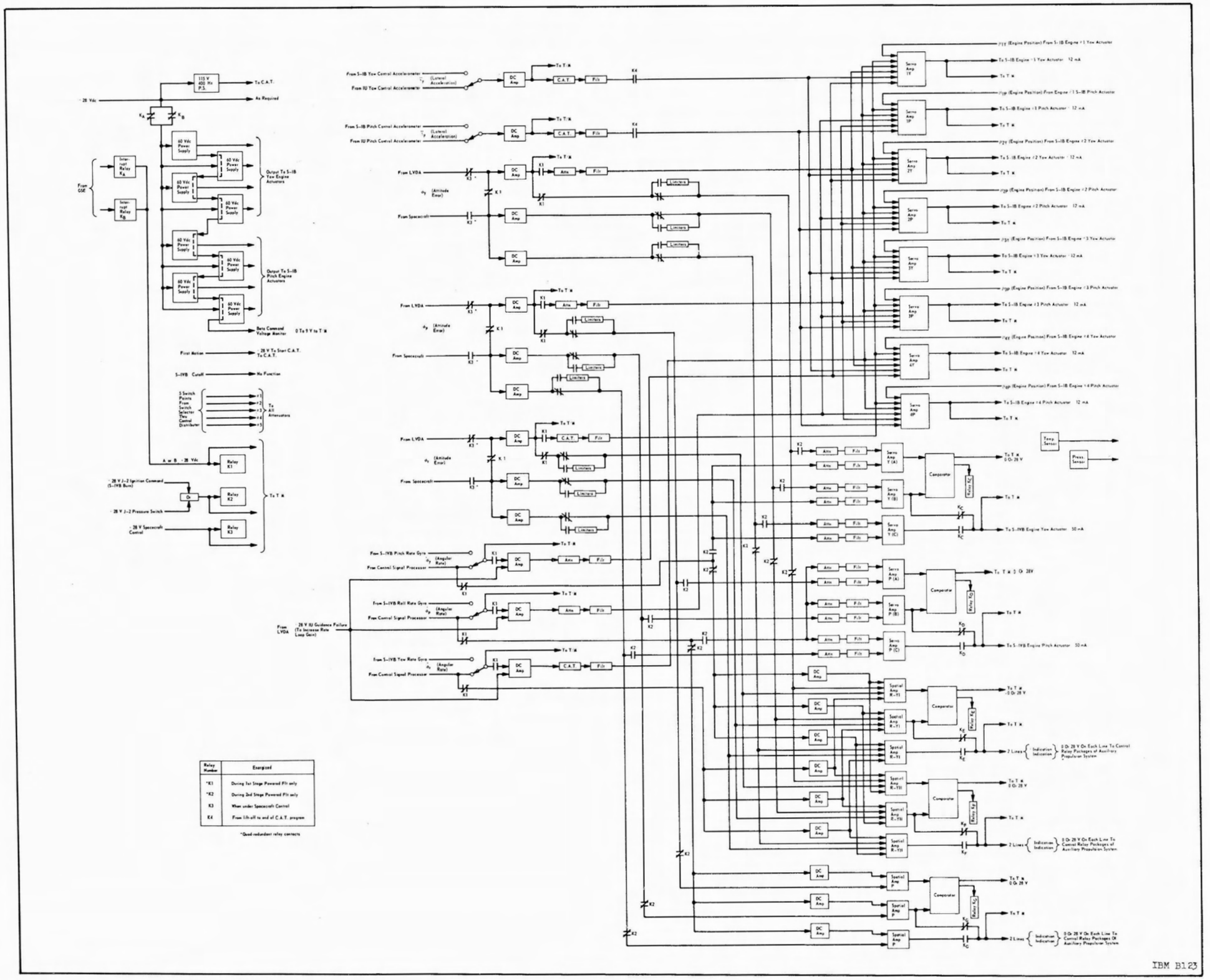


Figure 3.4-5 Block Diagram of the Servo Amplifier in the Flight Control Computer (For Powered Flight)



Relay Number	Energized
*K1	During 1st Stage Powered Flt only
*K2	During 2nd Stage Powered Flt only
K3	When under Spacecraft Control
K4	From Lift-off to end of C.A.T. program

*Quad-redundant relay contacts

Figure 3.4-3 Saturn IB Flight Control Computer Block Diagram

The output signals of two yaw servo amplifiers are compared, and if they agree, one is used to control the yaw actuator. If those two output signals disagree, the output of the third yaw servo amplifier is switched to the actuator. The same scheme applies to the pitch channel.

The operation of the Flight Control Computer in connection with the APS is described in paragraph 3.4.3.

SATURN V FLIGHT CONTROL COMPUTER

Figure 3.4-6 is a block diagram of the Saturn V Flight Control Computer. The attitude error signals (ψ), originating either from the LVDA or the spacecraft, are switched by a quad redundant relay configuration to three scaling amplifiers in each of the three channels (yaw, pitch, and roll). A different set of filters is switched in for each powered flight phase (S-IC, S-II, S-IVB). The scaling amplifiers provide the proper adjustment of the gain coefficients' (a_0 and a_1) time variable if required (by C.A.T. or resistor switching).

The attitude error signals and angular rate signals from the filters are summed in the magnetic servo amplifiers and the resulting signal is used to generate the actuator control signals. The Flight Control Computer contains eight servo amplifiers of the same type. Each amplifier provides a maximum output current of 50 milliamperes to torque the motor-operated control valves of the actuators. Each servo amplifier controls one of the eight engine actuators in the S-IC Stage or S-II Stage.

The S-IVB Stage has only two engine actuators. Six of the eight servo amplifiers are used in a triple redundant arrangement for the S-IVB powered flight phase as has been described for the Saturn IB Flight Control Computer.

The roll signals (ψ_r and $\dot{\phi}_r$) are distributed to all eight servo amplifiers. The yaw signals (ψ_y and $\dot{\phi}_y$) are connected to all four yaw servo amplifiers and the pitch signals (ψ_p and $\dot{\phi}_p$) are connected to all four pitch servo amplifiers.

The switching of input signals, filters, attenuators, and servo amplifiers in the Flight Control Computer is controlled by the LVDC/LVDA through Switch Selector circuitry. See Section 4.2.

3.4.3 FLIGHT CONTROL COMPUTER OPERATION DURING COAST FLIGHT

A detailed description of the operation of the auxiliary propulsion system has been given in Section 3.2. The Flight Control Computer configurations of the Saturn IB and Saturn V are identical for coast flight attitude control (Figures 3.4-3 and 3.4-6).

No filters are contained in the signal channels (ψ and $\dot{\phi}$) of the APS. Attitude error signals (ψ) from the spacecraft are limited in the Flight Control Computer between the dc amplifiers and the spatial amplifiers. The limiter circuits provide signal limiting corresponding to an angular rate of 0.5 degree/second in roll and 0.3 degree/second in pitch and yaw. They are switched into the circuit only during the spacecraft control mode of operation.

The scaling amplifiers adjust the gain coefficients (a_0 and a_1) to the proper value. The signals from the scaling amplifiers are sent to the spatial amplifiers. The spatial amplifiers sum the input signals (ψ and $\dot{\phi}$) and compare the resulting signal level with a predetermined threshold level. When the combined control signals exceed the limits set by the threshold, a switching amplifier energizes the relays in the control relay package, which in turn operates the values of the proper attitude control engines. The Flight Control Computer contains nine spatial amplifiers used in a triple redundant configuration (three spatial amplifiers for each pitch, yaw, and roll control). A comparator circuit selects 1 of 2 amplifiers out of the 3 triple-redundant amplifiers in each channel. The spatial amplifiers for pitch control switch either the (+) pitch or the (-) pitch nozzle on. See Figure 3.4-7. They require only the two input signals (ψ_p and $\dot{\phi}_p$). The remaining 2 groups of spatial amplifiers both control yaw and roll maneuvers. Each of these amplifiers receives roll and yaw input signals (ψ_r, ψ_y, $\dot{\phi}_r$, $\dot{\phi}_y$) since the same nozzles are used for yaw and roll control (see Figure 3.4-7). The control relay package which operates the valve coils is discussed in Section 3.2.

Figure 3.4-8 shows a simplified block diagram of a spatial amplifier.

3.4.4 REDUNDANCY IN THE FLIGHT CONTROL COMPUTER

The attitude rate signals ($\dot{\phi}$) and the attitude error signals (ψ) enter the Flight Control Computer via separate duplex lines. The duplex lines continue until they branch into the three scaling amplifiers

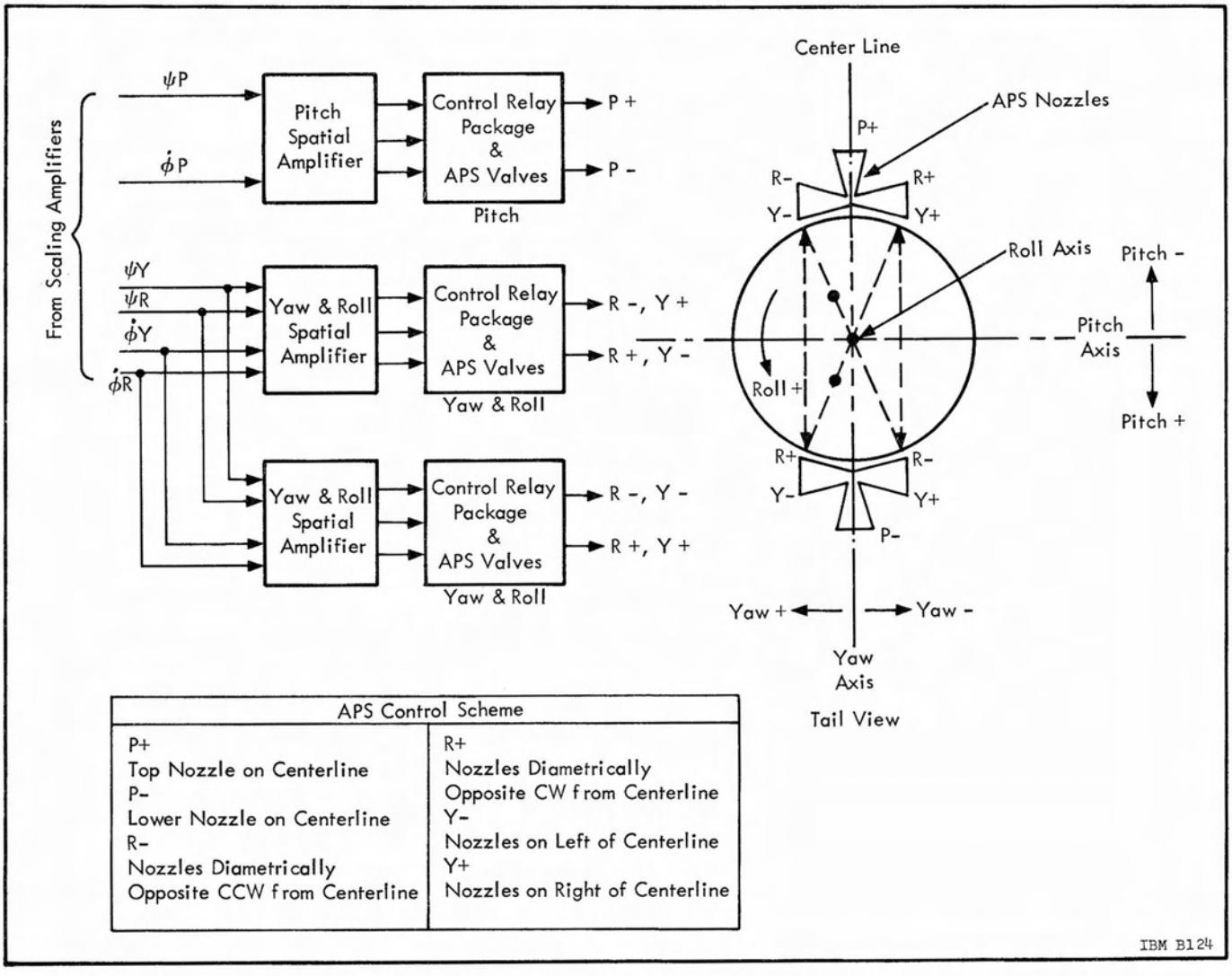


Figure 3.4-7 Connection of Control Signals to Spatial Amplifiers

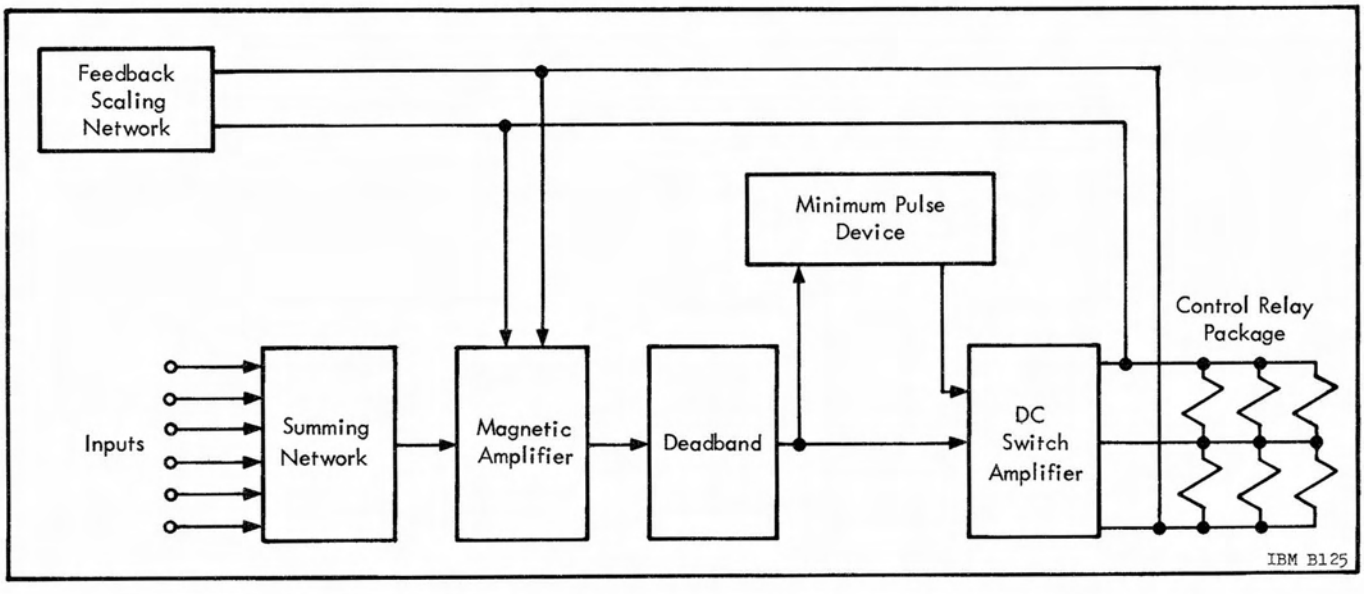


Figure 3.4-8 Block Diagram of a Spatial Amplifier in the Flight Control Computer

Figure 3.4-6 Saturn V Flight Control Computer Block Diagram

as shown in Figure 3.4-9. (The switchover between attitude error signals from the LVDA or the spacecraft is accomplished by relays arranged in a quad redundant configuration.)

For the S-IVB powered flight and coast flight attitude control, the Flight Control Computer has a triple redundant configuration in each channel (see Figures 3.4-3 and 3.4-6). For each of the six input control signals (ψ_p, ψ_y, ψ_r, $\dot{\phi}_p$, $\dot{\phi}_y$, $\dot{\phi}_r$), there are three redundant, completely independent channels. Each channel contains individual scaling amplifiers, filters (if used), and relays. These triple redundant signal channels are connected to a triple redundant arrangement of servo amplifiers or spatial amplifiers. The outputs of two of the three triple redundant servo (or spatial) amplifiers are compared and, if they agree, one output is applied to the engine actuator (control relay package). If the compared signals do not agree, the output of the third servo (spatial) amplifier is used.

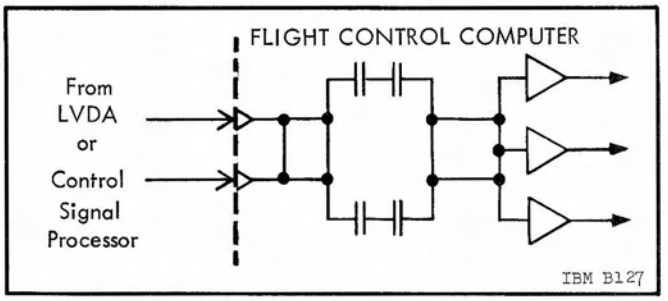


Figure 3.4-9 Redundant Cabling in the Flight Control Computer

SECTION 3.5
ENGINE SERVO ACTUATORS

The angular direction of the thrust vector of Saturn IB and V engines is controlled by swivelling the gimbal-mounted propulsion engines. This control is obtained by linear hydraulic servo-actuators in the pitch and yaw planes.

The actual arrangement of the actuators for the multi-engine stages and the single-engine S-IVB Stage of the Saturn Launch Vehicle is shown in Figure 3.5-1. Independent hydraulic systems for each gimbaled engine are used to provide the following advantages:

- Flight system can be qualified by single-engine test.
- One system can be verified at a time.
- Malfunction and replacement can be isolated to 1 system.
- Post flight performance comparisons are easily accomplished and problem areas are quickly isolated.
- Redundant capability.

For the multi-engine vehicle stages, the redundant capability is further increased by sizing the swivel range so that, despite the failure of one control engine, the remaining gimbaled engines can maintain satisfactory control. The failure modes may be:

- Loss of thrust (engine out).
- Loss of hydraulic pressure (hydraulic system failure).
- Any actuation malfunction caused by servo valve failure, failure in signal lines, or Flight Control Computer output stage.

During operation of the rocket engines in the S-IC and S-II Stages, the hydraulic power supply provided by a hydraulic pump driven by the engine turbine and an accumulator-reservoir to cover peak loads. An auxiliary pump, driven by an electric motor, provides hydraulic pressure for static checkout of the hydraulic system.

For the first-stage engines, the hydraulic pressure is obtained directly from the fuel turbopump; the fuel is used as hydraulic fluid. The available low operating pressure requires a large servo valve and actuator piston area; however, the pressurization system is very simple and even the accumulator-reservoir can be omitted as a result of the almost unlimited availability of pressurized fuel.

The transformation of the electrical signal from the Flight Control Computer, which commands the angular deflection (β) of the engine into a linear displacement, is performed by servo actuator assemblies. The servo valves are four-way, flow-control devices, with internal dynamic pressure feedback and mechanical feedback of the actuator piston position. Figure 3.5-2 is a symbolic representation of the valve. The servo valve operates in the following manner. The error signal from the Flight Control Computer is applied to the torque motor coil which displaces the flapper valve and restricts the flow of hydraulic fluid in one branch (e.g., the left one in Figure 3.5-2). The increasing pressure in that branch drives the second stage power spool to the right, which in turn allows hydraulic pressure build up on the left side of the actuator piston, causing a linear displacement of the actuator to the right. The mechanical feedback linkage displacement places a counter torque on the flapper valve. When this feedback torque equals the applied torque from the servo valve torque motor, no further motion of the actuator can occur. The potentiometer measures the actuator position for telemetry purposes.

In the S-IB Stage servo actuators only, an electrical potentiometer is used as a feedback transducer. It applies a "β" feedback signal to the Flight Control Computer servo amplifier. The mechanical feedback provides higher reliability, which results primarily from the elimination of the feedback potentiometer and its associated wiring, connections, and power supply, and reduction in corresponding failure modes. Further, the mechanical feedback has an important advantage in that the actuator goes to a null position ($\beta = 0$) if the "β" command signal from the Flight Control Computer fails in the zero level.

The characteristics of the hydraulic servo actuator systems are given in Table 3. 5-1.

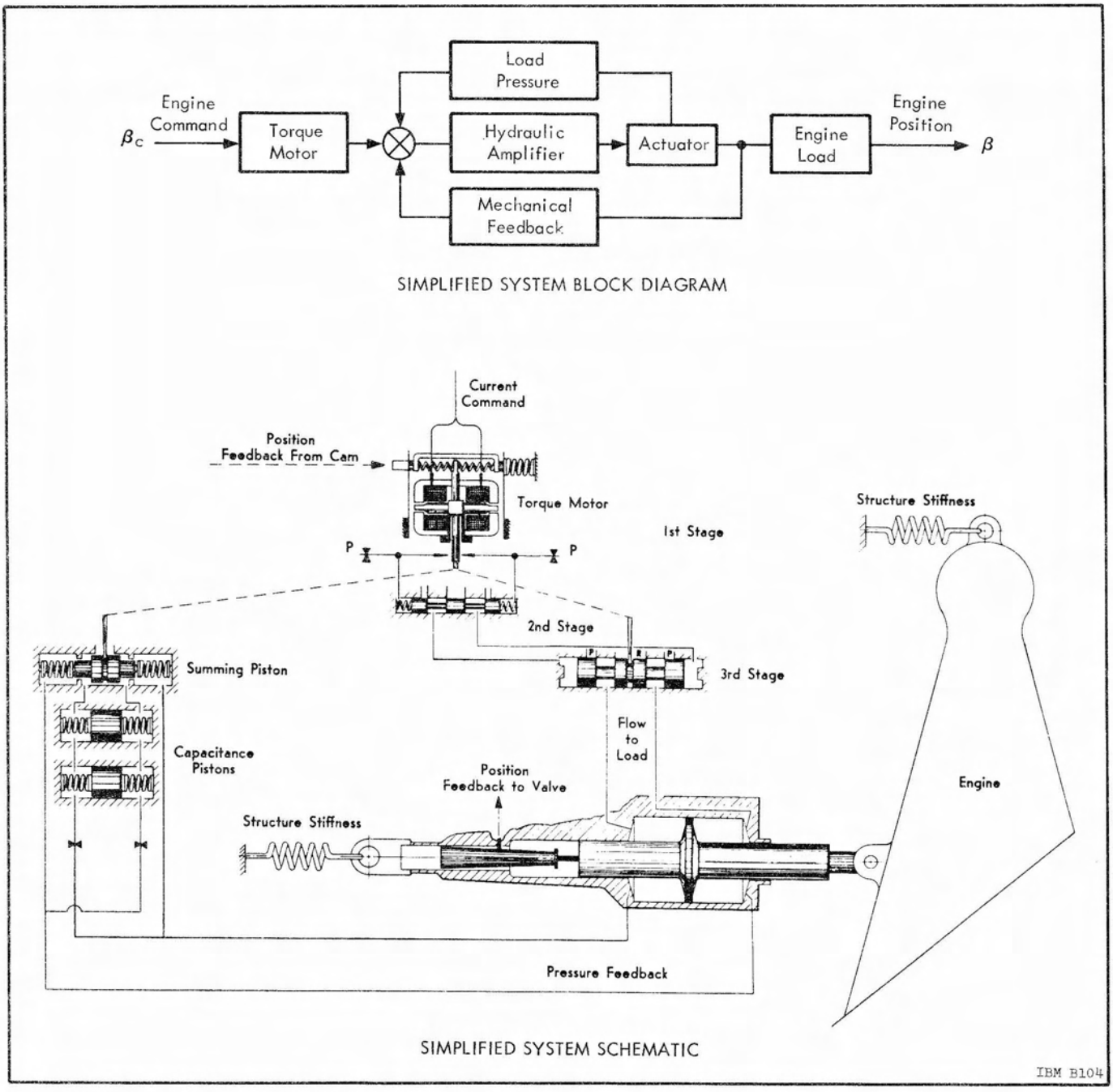


Figure 3. 5-1 Hydaulic Actuator System

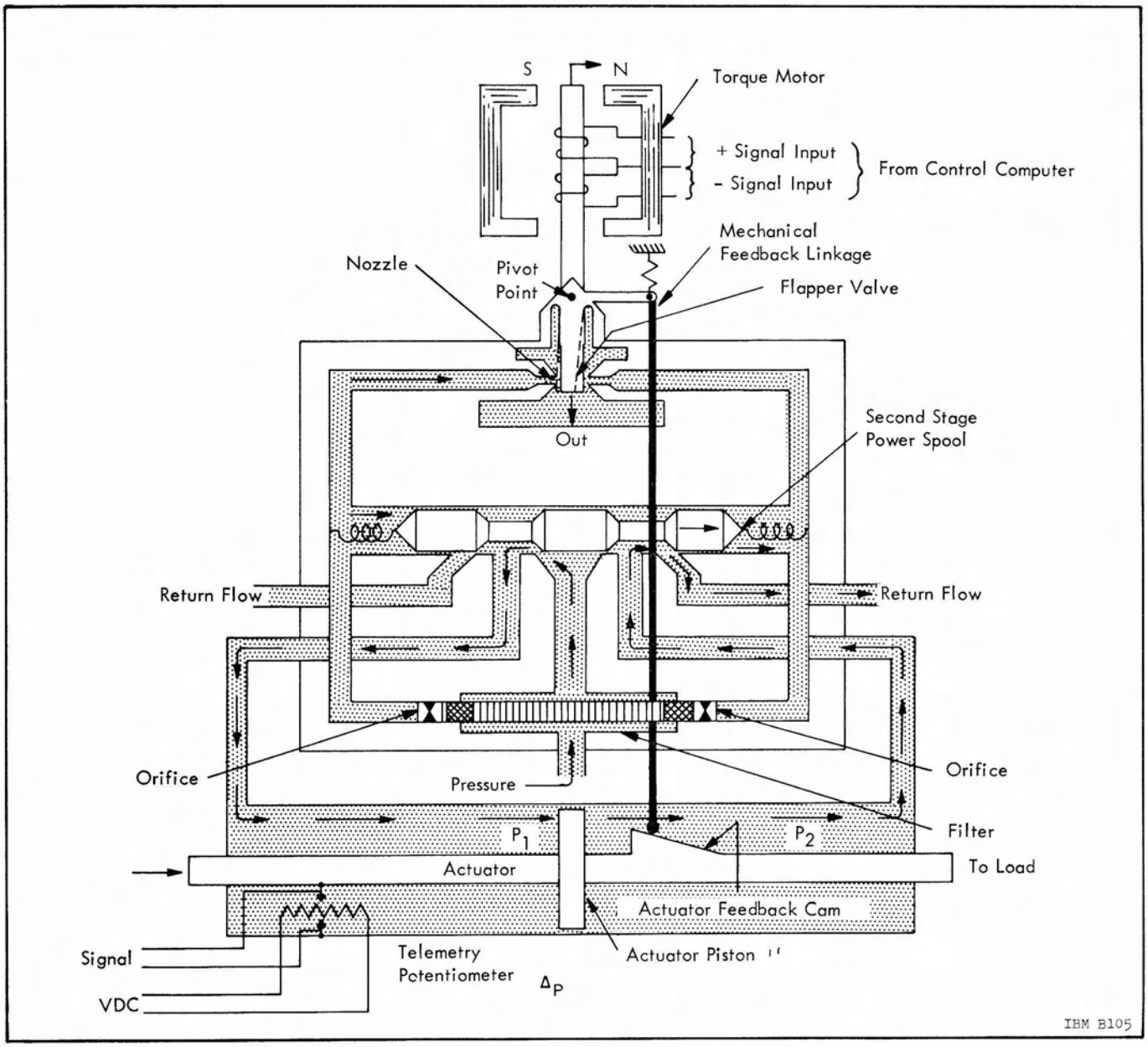


Figure 3.5-2 Flow- through Valve and Actuator with Mechanical Feedback

Table 3.5-1 Servo Actuator Characteristics (Design Goals)

Parameter	S-IC F-1 Engine	S-II J-2 Engine	S-IVB J-2 Engine	S-IB H-1 Engine
Engine				
Moment Arm				
meters	1.620	0.301	0.295	0.699
inches	63.8	11.9	11.6	27.5
Moments of Inertia				
kg m^2	42,000	1,990	1,970	750
slug ft^2	56,760	2,690	2,660	1,015
Servo Actuator				
Piston Area cm^2	368	83.9	76	32.3
in^2	57	13	11.78	5
Stroke cm	29.2	7.7	7.4	9.7
inches	11.5	3.02	2.9	3.82
Supply Pressure				
N/cm^2	12.4×10^6 to 15.2×10^6	24.2×10^6	25.2×10^6	20.7×10^6
psig	1,800-2,200	3,500	3,650	3,000
Torque Motor Current				
ma	50	50	50	12
System				
Angular Deflection				
degrees	±5.15	±7	±7	±7.99
Angular Velocity				
deg/s	5	9.6	8.0	
Load Resonance	8.0	7.9	7.1	

CHAPTER 4

MODE AND SEQUENCE CONTROL

TABLE OF CONTENTS

SECTION 4.1

INTRODUCTION

The terms mode and sequence control will be defined to explain their relationship with the Astrionics System. The LVDC memory contains a predetermined number of sets of instructions which, when initiated, induce the entire Astrionics System, or portions of the system, to operate in a particular mode. An example of a mode operation is the solving of guidance equations with interlaced attitude control and sequencing commands during the first stage flight. Each mode consists of a predetermined sequence of events. The computer also generates the appropriate control signals (e.g., engine cutoff and ignition, stage separation). Such a predetermined sequence of events is initiated by commanding the computer to operate in a particular mode.

Mode selection and initiation is accomplished through one of 3 actions: the successful completion of a previous mode, computer switching to a new mode based on real time, or an event occurrence. In addition to these internal mode selections which the system makes, mode switching is also accomplished by commands from the ground checkout equipment (before launch), the IU command system, or the Apollo Spacecraft. A built-in safeguard feature gives the system the capability of refusing conflicting commands or commands that would be detrimental to vehicle safety.

Examples of modes of operation that occur during flight in the Astrionics System are:

- First-stage guidance, control, and sequencing.
- Second-stage guidance, control, and sequencing.
- Third-stage guidance, control, and sequencing.
- Orbital operations —

  Vehicle attitude stabilization commanded by the IU.

  Spacecraft command of the vehicle attitude.

- Guidance, control, and sequencing of the third stage (second burn) into lunar trajectory —

  Using the IU navigation, guidance, and control system.

  Using the spacecraft navigation, guidance, and control system.

- Control of stage sequence functions from ground stations through the IU command system (emergency mode).
- Insertion of data into the LVDC through the IU command system.

The mode and sequence control scheme is very flexible since changes of modes and flight sequences are made by changing the instructions and programs in the LVDC memory, rather than by hardware modifications. The equipment involved in mode and sequence control of the launch vehicle is indicated in Figure 4.2-1. The LVDC issues flight sequence commands through the LVDA to the Switch Selector of the particular stage where the command must be executed. The Switch Selector of the addressed stage activates the appropriate circuit to perform the commanded function (e.g., engine cutoff, power ON or OFF). The Switch Selector operation is discussed in Section 4.2.

Mode commands from the spacecraft to the LVDA change the operational mode of the IU guidance and control system. When the Astronaut wants to control the attitude of the vehicle during coast flight, in

orbit, and after translunar injection, he initiates the proper mode command to the LVDA. The mode command is processed by the LVDA and LVDC, and the necessary sequence signals are generated to allow attitude control signals from the spacecraft to feed into the IU Flight Control Computer. Control is returned to the IU attitude control system when the Astronaut issues another mode command. In a similar manner, the back-up guidance mode may be selected. In this mode, the navigation and guidance system of the spacecraft guides the vehicle during powered flight.

During coast flight, the IU command system may be used to command mode changes from the ground.

Before launch, the ground checkout equipment exercises all operational modes of the Astrionics System. This includes simulated launch and orbit programs. The launch computer commands a particular mode of system operation by sending a coded command to the LVDA which "reads" it into the LVDC. The mode command is decoded, and the set of instructions or program, which is defined by the decoded mode command, is selected from the LVDC memory. The LVDC then begins to execute (within itself or elsewhere in the system) the instructions in that mode program.

Some events of the flight sequence are controlled by "discrete" signals generated by the LVDC according to a time program. Other events of the flight sequence are initiated when a particular event has occurred. For example, a signal is sent to the IU indicating S-IC engine cutoff — the LVDC then sends a signal to shutdown the S-II recirculation system.

A new time base for the time-controlled program is initiated during operation as a result of certain flight events (e.g., at lift-off, by the actuation of the first stage propellant level sensors, and S-IVB engine cutoff). A discrete signal is given to the LVDC as a reference for each time base.

SECTION 4.2

SWITCH SELECTOR

Each stage and the Instrument Unit of the Saturn Launch Vehicles contain a Switch Selector. The Switch Selector is the connecting link between the LVDA/LVDC, which generate the flight sequence commands, and the circuitry in a vehicle stage where the command is to be executed. The Switch Selector consists of relay circuits which decode the digital flight sequence command from the LVDA/LVDC and activate the proper stage circuits to execute the command.

Each Switch Selector can activate 112 different circuits in its stage, one at a time. The Switch Selectors of the stages are connected in parallel to the LVDA. The selection of a particular stage Switch Selector is accomplished through the command code. Coding of flight sequence commands and decoding in the stage Switch Selectors reduces the number of interface lines between stages and increases the flexibility of the system with respect to timing and sequence. In the Saturn V Launch Vehicle, which contains 4 Switch Selectors, 448 different functions can be controlled with only 28 lines from the LVDA (two IU +28-volt and two signal return lines from the control distributor are also used). Flight sequence commands may be issued at time intervals of 100 milliseconds.

Figure 4.2-1 illustrates the Saturn V Switch Selector configuration. As shown, all Switch Selector control lines are connected through the Control Distributor in the IU to the LVDA and the electrical support equipment.

There are two different methods of controlling the Switch Selector: manually, from the ground equipment by way of the Switch Selector test panel, or automatically, through the ground control computer. The ESE can individually command each stage Switch Selector's power ON or OFF. In the internal power OFF position, ESE power is available to the Switch Selectors.

Two measurement signals are returned from each stage directly through the umbilical to the ESE; one indicates that the Switch Selector is operating on internal power, and the other that the Switch Selector is reset. This reset signal, or zero indication, is the output obtained with all register relays reset to zero.

Except for these special lines from the ESE, the Switch Selector operation is the same whether under ESE or LVDC/LVDA control. In the following paragraphs, only the LVDC/LVDA control will be described.

The flight sequence commands are stored in the LVDC memory and are issued according to the flight program. When a PIO instruction is given, the LVDC sends the flight sequence command, consisting of 15 bits in serial form, to the switch selector register in the LVDA where they are stored. The Switch Selector word format is shown in Figure 4.2-2. Eight bits represent the flight sequence command; five bits are provided for selection of a particular stage Switch Selector; one bit, the read command, is used to activate the addressed Switch Selector for execution of the command; and the remaining bit is used to reset all Switch Selector relays.

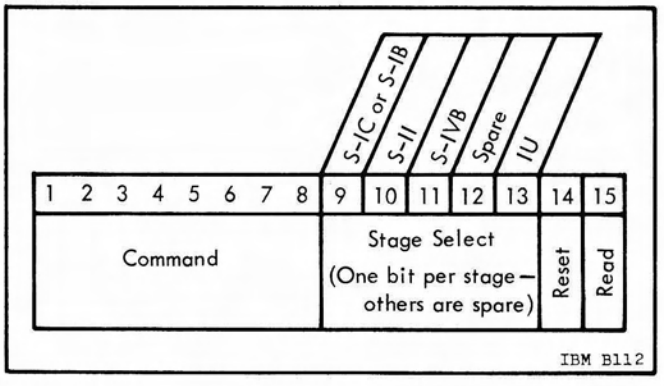


Figure 4.2-2 Switch Selector Register Word Format

To maintain power isolation between vehicle stages, the Switch Selector is divided into 2 sections: (1) the input section, composed of latch relays (for bit selection, verification, and stage select), and non-latching relays (for read and reset). The relays are powered from the LVDA (+28 Vdc IU power); (2) the output relay drivers, which are powered from stage supplies (+28 Vdc). The input and output are coupled together through a diode matrix which decodes the 8-bit input code and activates an output from one of the relay driver outputs. Each Switch Selector is connected to the LVDA through 22 lines:

2 stage select lines
2 read command lines
2 reset (forced) lines
8 bit register output lines
8 verification lines

In addition, there are 2 lines for IU +28 Vdc and 2 lines for signal return between the Control Distributor and the Switch Selectors.

The wire pairs for stage select, read command, forced reset, IU +28 Vdc, and signal return are redundant. Only one of each pair is required for normal operation.

All connections between the LVDA and the Switch Selectors, with the exception of the stage select inputs, are connected in parallel as shown in Figure 4. 2-3.

The output signals of the LVDA switch selector register, with the exception of the 8-bit command, are sampled at the Control Distributor in the IU and sent to the IU PCM telemetry system. Each Switch Selector also has 3 outputs to the telemetry system within its stage. The Switch Selector is designed to execute flight sequence commands given by the 8-bit code or by its complement. This feature increases reliability and permits operation of the system despite certain failures in the LVDA switch selector register, line drivers, or Switch Selector register relays.

After setting up the Switch Selector input relays by the 8-bit command, the complement of the received code is sent back to the LVDA/LVDC (over eight parallel lines). The feedback (verification information) is returned to the digital input multiplexer of the LVDA and is subsequently compared with the original code in the LVDC. If the feedback agrees with the original information, a read command is given. If the feedback does not agree with the code issued originally, a reset command is given (forced reset), and the LVDC/LVDA reissues the 8-bit command in complement form.

A simplified diagram of the Switch Selector (Model II) is shown in Figure 4. 2-4. The basic circuits of the Switch Selector are as follows:

Stage selection

Input bit relays

Verification relays

Reset (forced) relay

Read command relays

Reset (automatic)

Decoding matrix

Output telemetry

A typical operation cycle to initiate a given function in a particular stage is accomplished as follows (see the timing chart, Figure 4. 2-5):

- The verify lines are sampled to ensure that all stage select relays have been reset. Zero voltage on all lines indicates that the relays have been reset. The presence of IU +28 Vdc on the verify lines indicates that the verify lines are "enabled" because a stage select relay is not reset. Having detected this situation, the LVDC commands a "force reset" and then rechecks the verify lines.

- The LVDC inserts the 8-bit command of the function to be initiated into the LVDA switch selector register. At the same time, a stage select command is sent to the appropriate Switch Selector. The stage select command completes the signal return path for the command bit input relays to allow the 8-bit command to be stored in the input bit register.

- The verification lines are sampled to determine if the command transfer was correct.

- If the verification is correct, the LVDC sends a read command to the Switch Selector which activates the proper output channel.

Notes: •Signal return lines from the Switch Selectors, through the Control Distributor, to the LVDA are not shown in this Figure.
•The letters used to label interstage connections between units are not actual pin or cable connectors. The letter code is denoted below:

a = 8-digit address (8 lines)
b = Force reset (register) (1 line + 1 redundant line)
c = Register verification (8 lines)
d = Read command (1 line + 1 redundant line)
e, f, g, h = Stage Select Lines (1 line + 1 redundant line)
j = b, c, d, e, f, g, and h to IU telemetry
k = Register test, Zero indicate, Sw Sel output — To stage telemetry (1 line each)
m = +28 Vdc from the Instrument Unit

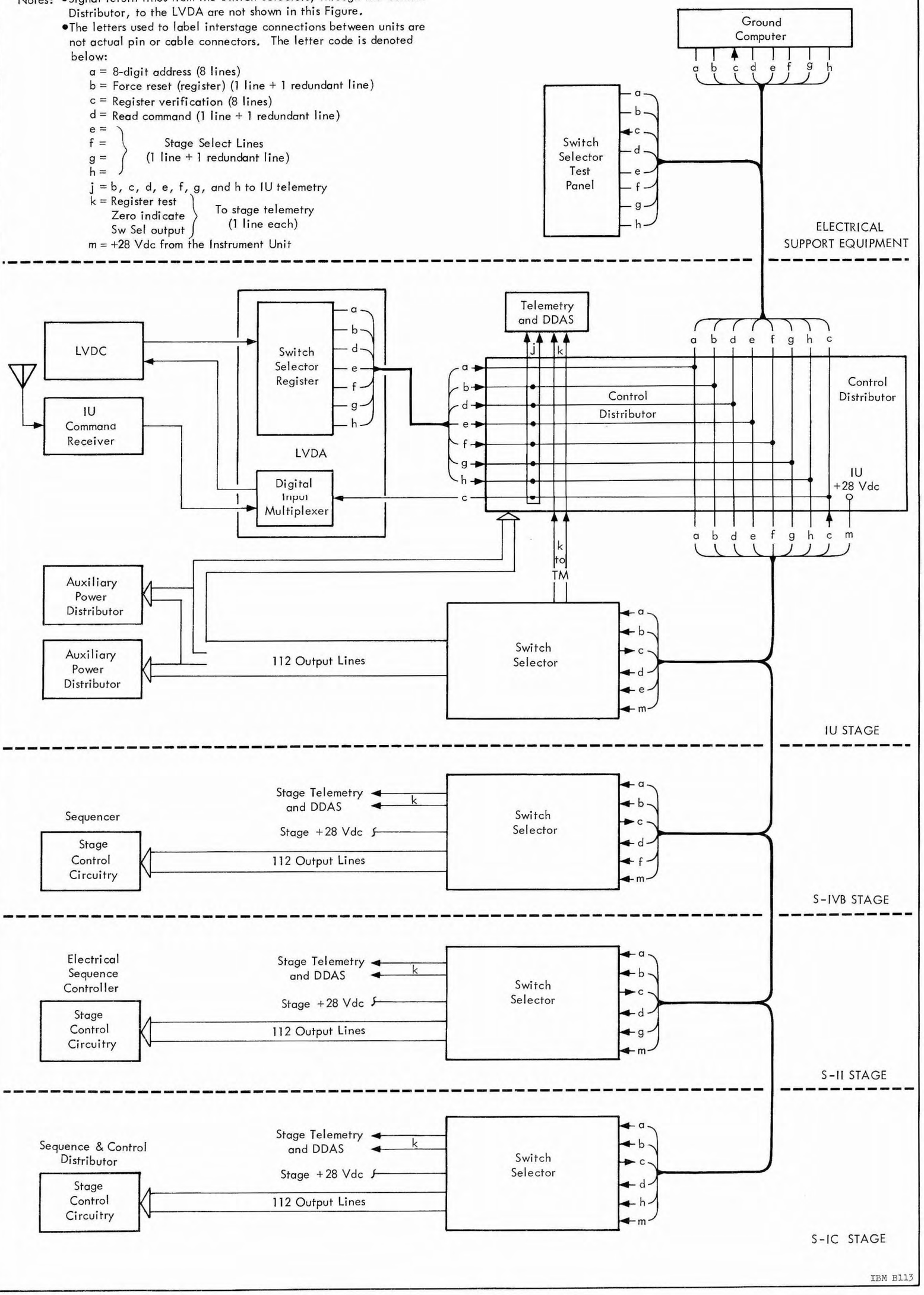
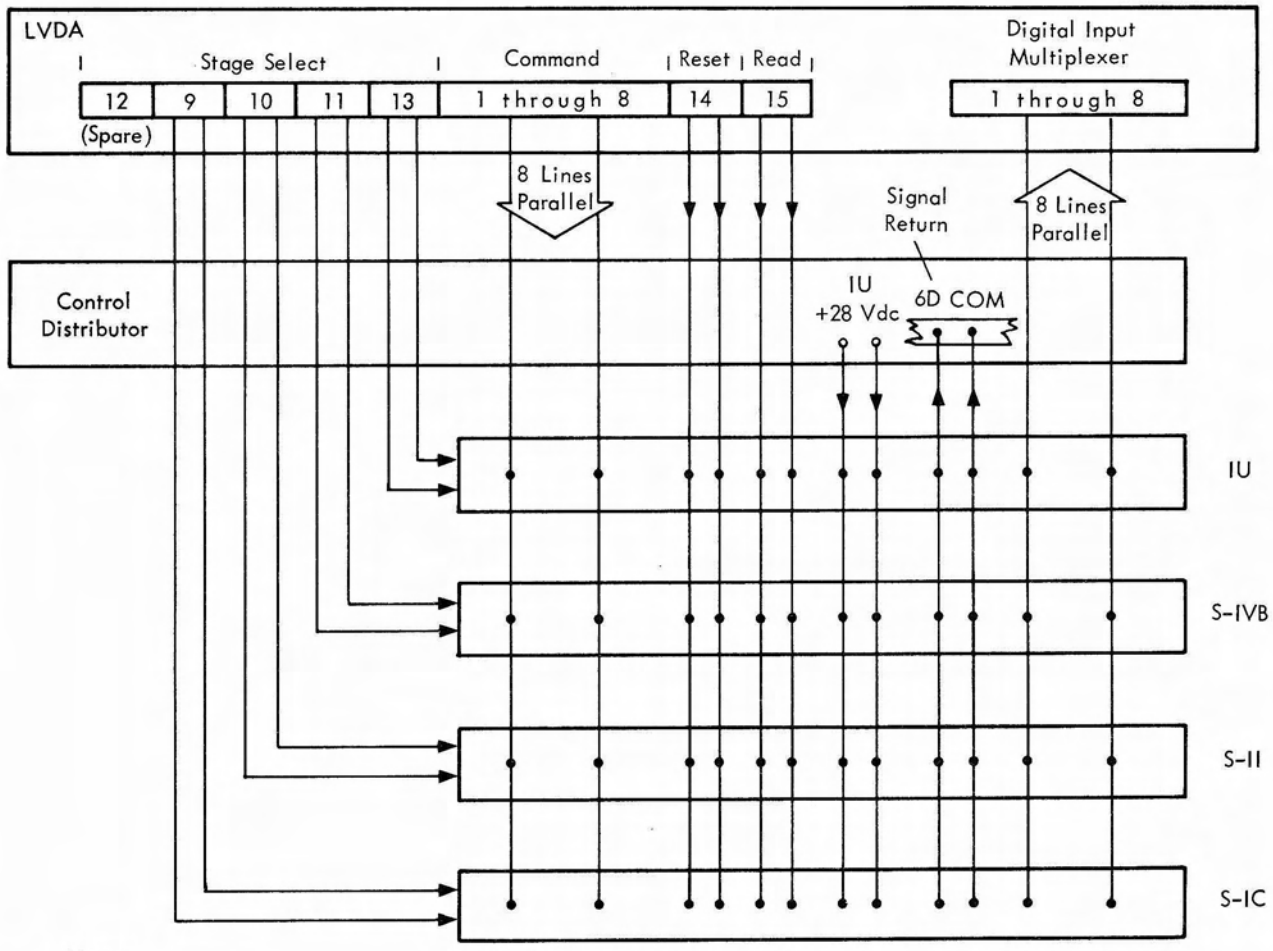


Figure 4.2-1 Switch Selector Configuration

- If the verification is not correct, the LVDC initiates a reset command to prepare the Switch Selector to receive the complement of the original word.
- After the forced reset is completed, the LVDC initiates the stage select command and the complement of the previously sent word. The LVDC neglects the verification information that occurs after the complement word is inserted. However, this information is transmitted via telemetry.
- The LVDC now initiates a read command signal which produces an output from the selected Switch Selector channel. The read command signal also energizes the automatic reset circuitry which returns the Switch Selector to the reset condition to prepare it for a new cycle.

A more detailed description of the Switch Selector operation is given in the following paragraphs.



Notes:

1. 22 lines between each Switch Selector and LVDA.
2. 26 lines between all Switch Selectors and LVDA (Saturn IB) (3 Switch Selectors).
3. 28 lines between all Switch Selectors and LVDA (Saturn V) (4 Switch Selectors).
4. 30 lines (maximum number) available to Switch Selectors from LVDA (5 Switch Selectors).
5. 4 lines (IU +28 Vdc and signal return) to all Switch Selectors from Control Distributor (Saturn IB and V).

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Figure 4.2-3 LVDC - Switch Selector Interconnection Diagram

STAGE SELECTION

The stage select command (1 bit) is transmitted individually on a separate line to each Switch Selector. No more than 2 Switch Selectors can be addressed simultaneously.

The stage select command, from the LVDA to a particular Switch Selector, sets three latch-type relays in that Switch Selector. The setting of these relays completes a ground path for the read command relay, the Set (S) bit relays, and the power inverter which controls the verify power relay (see Figure 4.2-4). This conditions the read relays and the bit relays to receive commands from the LVDA and allows the power inverter to energize the verify power relay. When the verify power relay contacts close, +28 Vdc power from the IU is applied through a set of stage select contacts to the verify relay contacts, and stage +28 Vdc is applied to the verify relays through the third set of stage select relay contacts. The Switch Selector can now accept the 8-bit command from the LVDA, store it in the bit relays, and make verification information available to the LVDA.

INPUT BIT RELAYS

The input register in the Switch Selector is made up of eight latch-type relays which are controlled by the coded command from the LVDA. The logic for the Switch Selectors is positive logic (i.e., +28 Vdc for a binary "1" and 0 Vdc for a binary "0").

The coded command is available to the Switch Selector during the same period of time the stage select signal is present. As soon as the stage select relays are set, a signal return path is provided for the coded address through the bit relays. This allows the coded address to be stored in the bit relays (latch type).

When a "1" is applied to a bit relay set coil, stage ground (0 Vdc) is switched to the "bit" input line of the decoder matrix and stage +28 Vdc to the "bit not" input line of the decoder matrix. If the input to the bit relay is a "0", the "bit" input line of the decoder matrix is at +28 Vdc and the "bit not" input line of the decoder matrix is at 0 Vdc.

VERIFICATION

The contacts of the bit relays control the output of the verification register. When a "1" is applied to the bit relay set coil, stage ground is switched to the verify relay set coil to cause the normally closed verify relay contact to open, indicating a "0" to the LVDA. When a "0" is applied to the bit relay set coil, the bit relay contacts remain in the reset condition. Stage ground is then applied to the verify relay reset coil, allowing the verify relay contact to remain in its normally closed position. Therefore, the verification output of a Switch Selector is the complement of the input command.

RESET (FORCED) RELAY

A forced reset is initiated by the LVDC when the verification information does not agree with the given command. The reset signal is applied to the forced reset relay coil causing the forced reset contacts to close. This applies stage +28 Vdc to the stage select reset and bit relay reset coils to force the Switch Selector into the reset condition shown in Figure 4.2-4. After a forced reset has been completed, the stage select command and the same flight sequence command are transmitted to the Switch Selector again. However, the command is now represented by the complement of the original 8-bit code. The complement command is not verified by the LVDC before the read command is issued.

READ COMMAND

Immediately after verification of the command, the read command is initiated. If verification of the original command proved to be false, the read command will not be initiated by the LVDC until the forced reset, stage select, and complemented command have been transmitted to the Switch Selector.

Three conventional type relays are picked when the read command is received from the LVDA. One side of the coils of these relays is connected to the read command signal, the other side is connected to the IU signal return through the stage select relay contacts. Thus, a stage select signal must have been received before a read command relay can be energized. When the read relay contacts close, stage +28 Vdc is applied to the AND gate generator (AG1, AG1N) portion of the decoder matrix. See Figure 4.2-4.

BIT RESET (AUTOMATIC)

The automatic reset is accomplished by a pulse which is automatically generated within the Switch Selector. This pulse is initiated by the operation of the conventional read command relays. A capacitor network (C, Figure 4.2-6) is connected between the read command relay contants and stage ground. When the +28 Vdc stage power is initially

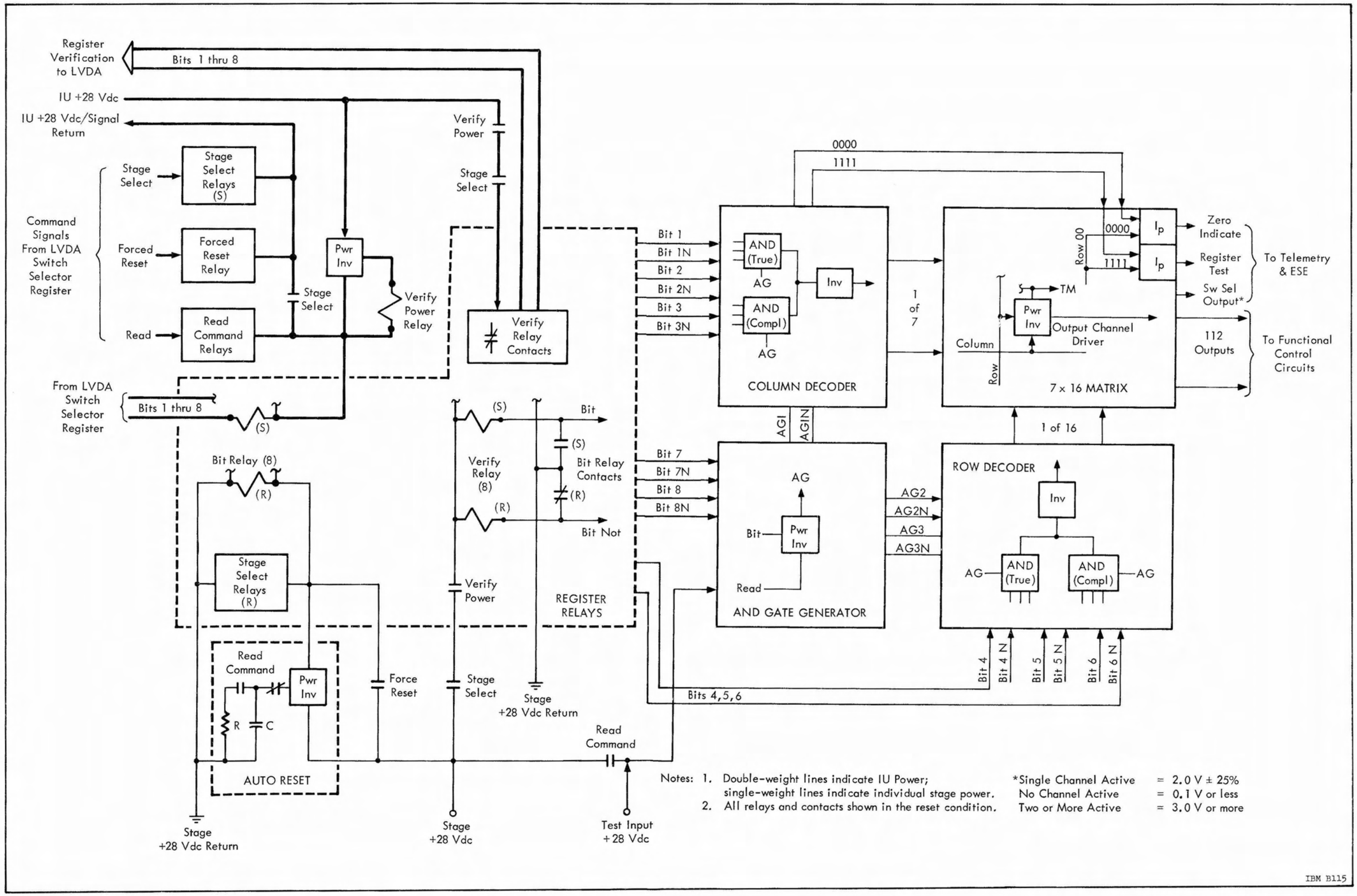


Figure 4.2-4 Switch Selector (Model II) Simplified Diagram

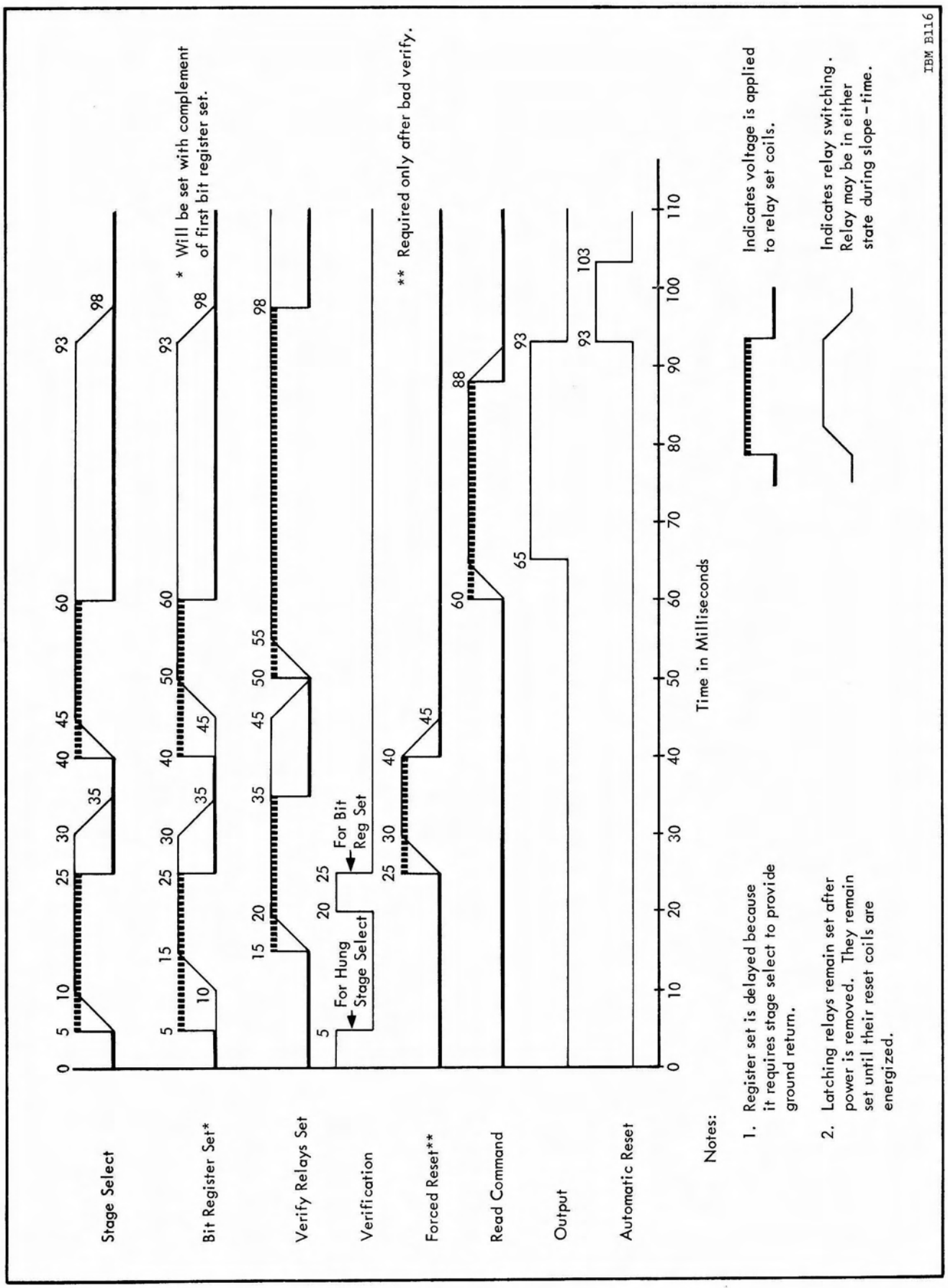


Figure 4.2-5 Switch Selector Timing Diagram

applied to the Switch Selector, the read command contacts are in their reset condition (as shown in Figure 4.2-6). Therefore, the capacitor network is allowed to charge to stage +28 Vdc through resistor R_2 in the power inverter circuitry. When the capacitor network is sufficiently charged, the output of the power inverter drops to zero and no voltage is applied across the bit relay reset coil. Thus, a power-ON reset is automatically provided.

When the read command is initiated, the normally closed read command contact opens. At the same time, the capacitor network (C) is connected to stage return through resistor R_1, and the capacitor discharges through R_1. At the end of the read command, the read relay contacts return to their normal state and return capacitor network (C) to the power inverter circuit. Capacitor network (C) momentarily acts as a low-impedance path for the 28 Vdc on the input of the power inverter. This allows the input to go toward ground potential and enable the power inverter to turn ON to produce the 28-volt reset pulse. The reset pulse is present until the capacitor network (C) is recharged to 28 Vdc. The length of this pulse is determined by the charge time of the capacitor network (C) through resistor R_2. The reset pulse is applied to the stage select reset and bit relay reset coils. The operation of these relays returns the Switch Selector to the reset condition shown in Figure 4.2-4.

DECODING TECHNIQUE

The 112 output channels of the Switch Selector are arranged in a 7 by 16 matrix configuration (7 columns and 16 rows). The coordinate selection is similar to the X-Y coincidence method common in core memory technology. An output channel driver

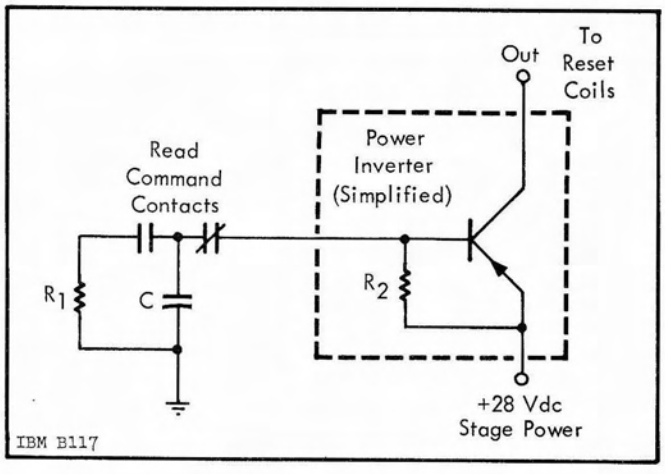


Figure 4.2-6 Automatic Reset Circuitry

(PNP inverter) with the dimension X_i, Y_j is activated when the row circuitry X_i and the column circuitry Y_j are turned ON by application of the read command. The 8-bit command provides 256 possible combinations. However, any address and its complement are capable of selecting the same output channel. This reduces the number of possible combinations to 128. A further reduction to 112 possible combinations is the result of omitting certain codes.

The 8-bit command is sub-divided into groups for decoding and output channel driver selection. The three least significant bits (1, 2, and 3) are decoded to enable the column selection circuitry. The next three bits (4, 5, and 6) are decoded to enable the row selection circuitry. Bits 7 and 8 and the read command are applied to the AND gate generator where they are decoded to supply the appropriate AND gate to the row and column decoders. The eighth bit determines whether the address is a true or complement word. The chart below illustrates the Boolean expressions for decoding bits 7 and 8.

$$
\begin{aligned}
AG1N &= B8N \cdot \text{Read Command} \\
AG1 &= B8 \cdot \text{Read Command} \\
AG2N &= AG1N \cdot B7N \\
AG2 &= AG1 \cdot B7 \\
AG3N &= AG1N \cdot B7 \\
AG3 &= AG1 \cdot B7N
\end{aligned}
$$

Note:

B8N = B8 Not = Bit 8 is a zero
B8 = Bit 8 = Bit 8 is a one

Therefore, decoding a typical word, 01010101, where bits 8 through 1 run from left to right, the column is determined by 8, 3, 2, and 1 or 0101 or more completely by AG1N · B3 · B2N· B1. Similarly, the row is determined by 8, 7, 6, 5, and 4 or 01010 or more completely AG3N · B6N · B5 · B4N. If the input register transfer circuitry shows a failure, the complement of this word must select the same XY coordinate of the output matrix. Therefore, the location X_iY_j, defined by 01010101, must also be defined by 10101010. The column is determined by AG1 · B3N · B2 · B1N, and the row by AG3N · B6 · B5N · B4. Therefore, the total expression to define this particular X_iY_j channel is:

$$
\begin{aligned}
X_iY_j &= AG1N \cdot AG3N \cdot B6N \cdot B5 \cdot B4N \cdot B3 \cdot B2N \cdot B1 \text{ or} \\
&= AG1 \cdot AG3 \cdot B6 \cdot B5N \cdot B4 \cdot B3N \cdot B2 \cdot B1N
\end{aligned}
$$

OUTPUT TELEMETRY

Each Switch Selector sends 3 signals directly to its stage PCM telemetry system. These signals are register test, zero indication, and Switch Selector output. Each of the measurements is a special output of the output driver matrix. The register test output is generated by an output driver when the input address selection is all ones and the read command has been given. The zero indication is generated when the address is all zeros. No other condition is required. These are used to test the address selection relays to show that they can be set and reset properly. The Switch Selector output signal is a special telemetry output from the output driver circuit. These outputs are all tied together, and the signal which goes to PCM telemetry indicates whether none, one, or more than 1 output is ON at the same time. If no channel is active, the output is 0.2 Vdc; one channel active is 2.0 Vdc; and more than one channel active is 3.0 Vdc or more. When the Switch Selector is operating properly, only one channel is activated. In the event of flight failure, this information is provided to aid in failure cause analysis. This type of output requires that the signal be connected to the Model 270 Multiplexer associated with PCM and not directly to the PCM/DDAS Assembly like the register test and zero indication outputs.

RELIABILITY

Reliability in the Switch Selector is accomplished through use of quadruple and triple modular redundant circuits. Redundant lines are also provided for the following signals: read command, stage select, reset, and signal return. The reset, stage select, and read command relays are redundant, offering improved reliability in relay coil operation and its associated contacts. The Switch Selector operates also in the presence of certain failures, since either the code or its complement will activate a specific driver. A ground rule used in the Switch Selector design is to prevent any single failure in the equipment from causing a catastrophic failure in the Switch Selector operation. Inability to activate a given channel at a desired time, or activation of a wrong channel, is considered a catastrophic failure.

SECTION 4.3

SATURN V OPERATION SEQUENCE

The Saturn V Operation sequence starts during the prelaunch phase at approximately T-15 hours when the electrical power from the ground support equipment is applied to all stages of the launch vehicle. Figure 4. 3-1 provides an overall view of the prelaunch sequence. During this time, the sequencing is controlled from the launch control center-launcher-umbilical tower complex, utilizing both manual and automatic control to checkout the functions of the entire Astrionics System.

After the umbilical is disconnected, the sequencing is primarily controlled by the LVDC. Each phase is numbered and a detailed sequence of that phase is given under that number. Some conditioning of the engines will occur previous to ignition and, although this occurs outside the time period shown, it is described with stage burn, as it is best associated with that stage.

There are other events controlled by the LVDC through the Switch Selector that are not given at this time because their place in sequence is unknown. They are mainly concerned with telemetry calibrations, tape recording operations, and transmitter operations. They will be included as details become available.

Table 4. 3-1 is a breakdown illustrating the phases and times within each phase. It should be pointed out that the time increment differences (hours, seconds, minutes) used were the most appropriate. The events, as they occur within each phase of a typical Saturn V flight sequence, are listed in Tables 4. 3-2, 4. 3-3, and 4. 3-4.

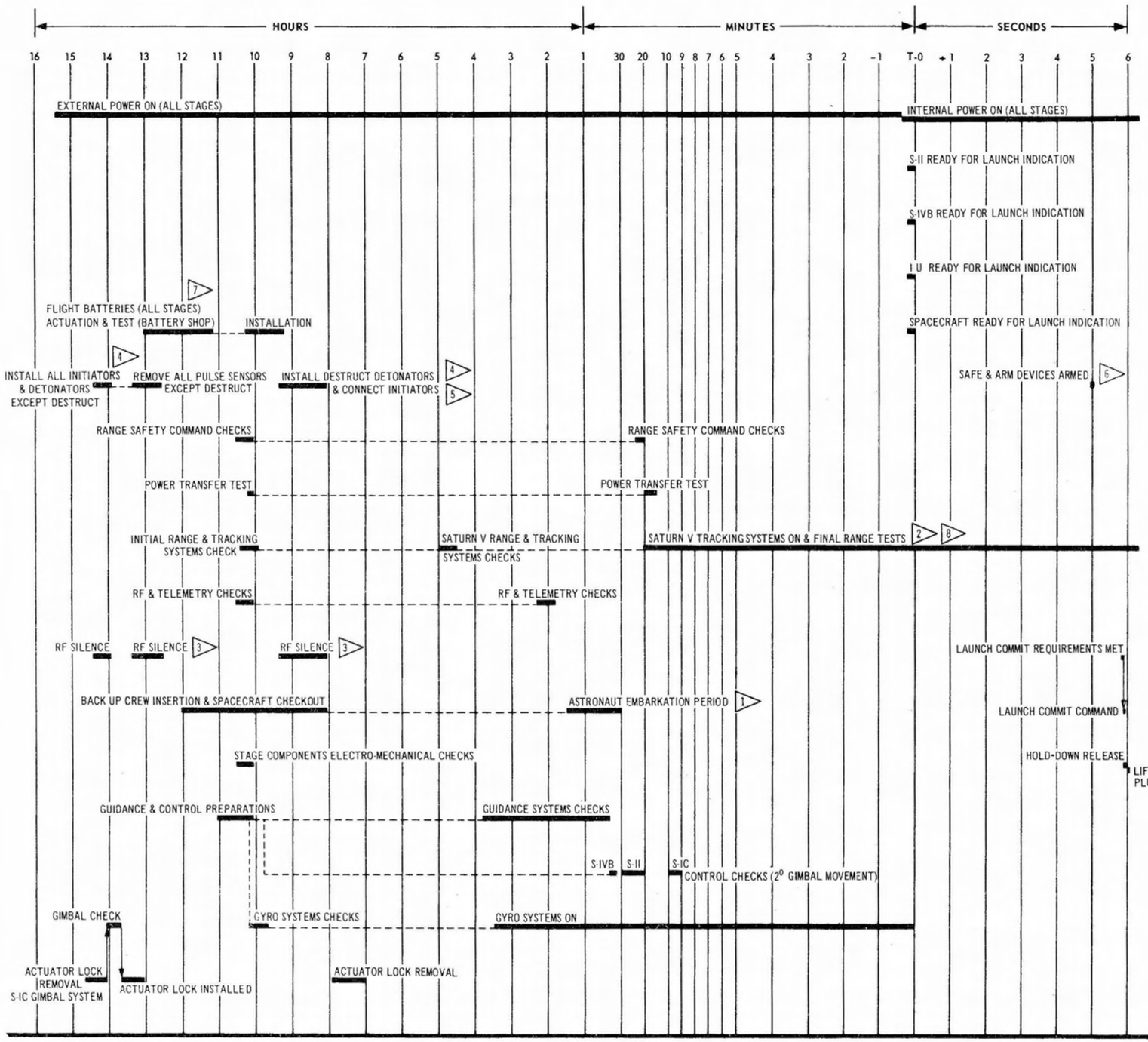
Note: All times are expressed in seconds except where designations H (hours) or M (minutes) are used. The abbreviation "TBD" indicates "To Be Determined".

Table 4. 3-1 Phase, Sequence, and Time Breakdown

Phase	Sequence	Time
1	Prelaunch (Power-on all stages)	15. 5 hours
2	S-IC Burn	146. 3 seconds
3	S-II Burn	375 seconds
4	S-IVB Burn	169. 8 seconds
5	Orbital Coast	4. 5 hours
6	S-IVB Restart	313. 1 seconds
7	Docking	Unknown

Table 4. 3-2 Saturn V Flight Sequence, Phase 1 - Prelaunch

Time to Ignition	Event
T-15. 5H	External power on all stages.
T-14. 7H	Gimbal system S-IC actuator lock removal.
T-14. 4H	RF silence, maintained during ordnance installation of electrical connection as a safety precaution.
T-14. 4H	Install all initiators and detonators except destruct.
T-14. 1H	Gimbal check S-IC.
T-13. 9H	Installation of all initiators and detonators except destruct completed.
T-13. 9H	RF silence completed.
T-13. 7H	Gimbal check S-IC completed, actuator lock installation begun.
T-13. 4H	Remove all pulse sensors except destruct begun.
T-13. 4H	RF silence begun.
T-13. 1H	Flight batteries (all stages) test and installation.
T-13. 1H	Gimbal system S-IC, actuator lock installation completed.
T-12. 5H	Removal of all pulse sensors except destruct completed.
T-12. 5H	RF silence completed.
T-12. 1H	Back-up crew insertion and Spacecraft checkout.
T-11. 1H	Guidance and control preparations and checks.
T-10. 6H	Range safety command checks begun.
T-10. 6H	RF and telemetry checks begun.
T-10. 6H	Stage components electro-mechanical checks begun.
T-10. 5H	Range and tracking systems tests, continue to lift-off.
T-10. 3H	Power transfer test begun.
T-10. 2H	Gyro systems checks begun.
T-10. 1H	Stage components electro-mechanical checks completed.
T-9. 4H	Destruct detonators and connect initiators installation begun.
T-9. 4H	RF silence begun.
T-9. 3H	Flight batteries (all stages) installation completed.
T-8. 1H	Destruct detonators and connect initiators installation completed.
T-8. 1H	RF silence completed.
T-7. 9H	S-IC gimbal actuator removal begun.
T-7. 3H	S-IC gimbal actuator removal completed.
T-3. 5H	Gyro systems checks completed, gyro system ON.
T-1. 8H	RF and telemetry checks completed.
T-40. 0M	Guidance system checks completed.
T-40. 0M	S-IVB control checks begun, 2 degrees gimbal movement.
T-35. 0M	S-IVB control checks completed.
T-30. 0M	S/C checkout completed and Astronauts have embarked.
T-30. 0M	S-II control checks begun, 2 degree gimbal movement.
T-20. 0M	Range safety command checks completed.
T-20. 0M	S-II control checks completed.
T-15. 0M	Power transfer test completed.
T-10. 0M	S-IC control checks begun, 2 degree gimbal movement.
T-9. 0M	S-IC control checks completed.
T-0. 4M	Internal power ON all stages.
T-0. 2M	S-II ready for launch indication.
T-0. 2M	S-IVB ready for launch indication.
T-0. 2M	IU ready for launch indication.
T-0. 2M	S/C ready for launch indication.
T-0M	Ignition command.
T+5. 0	Safe and arm device, armed.
T+5. 8	Launch commit requirements met.
T+5. 9	Launch commit command.
T+5. 9	Hold-down release.
T+6. 0	Lift-off umbilicals and tail plugs disconnect.



GUIDELINES USED IN PREPARING THIS SEQUENCE

1. ASTRONAUT EMBARKATION PERIOD INCLUDES PERSONNEL TRANSPORTATION TIME TO PAD, CREW INSERTION, SECURING ACCESS DOOR AND TIME REQUIRED FOR PERSONNEL TO CLEAR PAD.
2. TRACKING WILL UNDERGO PERIODIC CHECKS DURING A LONG COUNTDOWN TIME SUCH AS THAT REQUIRED FOR SATURN V/APOLLO TO ENSURE THAT UNDUE DRIFT IS NOT OCCURRING.
3. RF SILENCE WILL BE MAINTAINED DURING PERIODS OF ORDNANCE INSTALLATION OR ELECTRICAL CONNECTION AS A SAFETY PRECAUTION.
4. PRIOR TO ELECTRICAL CONNECTIONS OF ORDNANCE ITEMS "NO VOLTAGE" CHECKS WILL BE MADE AND FINAL RANGE SAFETY AND SEPARATION CHECKS WITH EBW PULSE SENSORS CONNECTED.
5. IT HAS BEEN ASSUMED THAT LIVE EBW'S CAN BE INSTALLED WITHOUT REMOVING EBW PULSE SENSORS THEREBY ALLOWING MAXIMUM FLEXIBILITY TO THE TIMING OF INSTALLATION AND ELECTRICAL HOOK-UP.
6. THE S&A'S ARE SHOWN ARMED PRIOR TO LAUNCH COMMIT (INSTEAD OF AT LIFT-OFF AS SHOWN IN OTHER SEQUENCES) TO PROVIDE RANGE SAFETY WITH AN INDICATION OF DESTRUCT CAPABILITY TO SATISFY THEIR LAUNCH COMMIT REQUIREMENT. REMOTE ROTATION OF THE S&A'S AND MICRO-SWITCH PICK-UP FOR "ARMED" INDICATION IN THE LCC MAY REQUIRE THIS FUNCTION TO OCCUR EVEN EARLIER THAN T-5 SECONDS.
7. BATTERY INSTALLATION IS DEPENDENT ON THE REQUIREMENT FOR THE FIRST POWER TRANSFER TEST WHICH WILL OCCUR IN THE TIME PERIOD SHOWN. BATTERY ACTIVATION AND TEST (IN THE ELECTRICAL LAB) PRECEDES THE INSTALLATION PERIOD BY A SUFFICIENT TIME PERIOD TO ALLOW DELIVERY TO THE UMBILICAL TOWER LOCATIONS AND ACTIVATION OF SPARE BATTERIES IF REQUIRED.
8. AFTER MAIN CRYOGENIC LOADING AND PRIOR TO IGNITION COMMANDS ALL SYSTEMS WILL UNDERGO FINAL CHECKS TO VERIFY ALL SYSTEMS READY FOR AUTOMATIC LAUNCH SEQUENCING.

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Figure 4.3-1 Typical Saturn V Astrionics System Prelaunch Sequence

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast

Time From Lift-off	Stage	Event	Remarks
0.0	VEH	Lift-off (LO)	Lift-off sets the computer time base. Fuel pressurizing valve No. 1 is sequenced open at this time. The pressure switch controlling fuel pressurizing valve No. 5 is enabled and controls the valve throughout S-IC burn.
TBD	S-IC	Signal from computer to enable engine cutoff capability.	This signal enables cutoff of any engine due to rough combustion or low thrust. The time this event occurs will be determined at a later date. Any 2 of 3 accelerometers located on each engine Flight Combustion Monitor (FCM) detecting combustion instability or any 2 of 3 thrust OK switches located on each engine indicating low thrust causes the malfunctioning engine to cut off after this signal.
49.5	S-IC	Signal from computer to open fuel pressurizing valve No. 2.	Fuel Pressurizing Valve sequence times are preliminary. Fuel pressurizing valve No. 1 (normally open) is opened at lift-off.
95.3	S-IC	Signal from computer to open fuel pressurizing valve No. 3	
133.5	S-IC	Signal from computer to open fuel pressurizing valve No. 4.	
137.3	S-IC	Signal from computer to arm inboard engine propellant depletion sensors.	Two upper fuel level sensors located in the fuel container and one upper LOX level sensor in the center LOX suction line are armed at this time.
142.3	S-IC	Signal to cut off inboard engine.	This signal will reset the computer time base. There are two different methods by which the S-IC inboard engine can be cut off normally. They are: (1) Actuation of LOX upper level sensor will initiate a one second timer which at expiration will cut off the inboard engine. (2) Actuation of either of two fuel upper level sensors will immediately cut off the inboard engine. Resetting of the computer time base at inboard engines cutoff should be independent of the malfunction cutoff signal (thrust OK or FCM).

Table 4. 3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
142. 7	S-II	Signal from computer to open S-II LH_2 prevalves.	The LH_2 prevalves must be opened at this time to provide a means of flushing out that portion of the main propellant feed duct between the prevalve and the tank outlet which has not been conditioned.
143. 0	S-IC	Close inboard engine LOX prevalves.	A 0. 7 second timer, located on the S-IC stage, will be started at inboard engine cutoff. Expiration of the timer will cause LOX prevalves to close.
143. 85	S-IC	Close inboard engine fuel prevalves	A 1. 55 second timer will be located on the S-IC stage which will be started at inboard engine cutoff. Expiration of the timer will cause fuel prevalves to close.
145. 3	S-IC	Signal from computer to arm S-IC outboard engine's propellant depletion sensors.	The time shown for this event is preliminary. Two low level fuel sensors located in the fuel container and four low level LOX sensors located one per outboard LOX suction line are armed at this time.
146. 3	S-IC	Signal to cut off outboard engine.	S-IC outboard engines cutoff will reset the computer time base. There are two different methods by which the S-IC outboard engine can be cut off normally. They are: (1) Actuation of any two LOX level sensors will initiate a one second timer which will cut off the S-IC outboard engines upon expiration. (2) Actuation of either of two fuel lower level sensors will initiate a one second timer which will cut off the S-IC outboard engines upon expiration.
146. 8	S-II	Signal from computer to trigger ullage rockets (8).	The S-II ullage rockets reach full thrust approximately 0. 170 seconds after the signal to trigger the ullage rockets is initiated by the computer. Ullage rockets are required to be at full thrust when the separation structure is severed. The S-II ullage rockets must burn until the S-II stage engines reach approximately 30 percent thrust. The effective burn time is 3. 7 seconds.

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
147.0	S-IC/ S-II	Signal from the computer to: (a) Fire separation device (b) Fire retrorockets (4).	Separation is initiated when the F-1 outboard engines thrust has decayed to the 10 percent level. Circuit delays of approximately 10-15 milliseconds (ms) are built in to the separation circuitry so that retrorocket ignition occurs after separation device ignition, to prevent possible unseating of the S-II stage propellants.
147.0	S-IC	Close outboard engines LOX prevalves.	A 0.7 second timer located on the S-IC stage which is started at outboard engines cutoff will cause the LOX prevalves to close when it expires.
147.07	S-IC/ S-II	Separation structure completely severed.	Occurs approximately 0.070 seconds after separation signal is initiated by the computer. First possible S-II axial motion relative to S-IC.
147.1	S-IC	Retrorocket thrust buildup begins.	Thrust buildup for the S-IC retrorockets occurs approximately 0.1 seconds after the separation signal from the computer. Successful separation can be accomplished with one retrorocket out.
147.3	S-IC/ S-II	S-IC/S-II Umbilical disconnect.	Voltage is supplied from the S-IC stage to the IU. When separation occurs, a plug is disconnected and voltage is no longer supplied which indicates physical separation has occurred.
147.4	S-II	Signal from the computer to switch engine position control from the S-IC to S-II.	Engine gimballing control is switched from the S-IC stage to the S-II stage. This is accomplished in the IU.
147.6	S-II	Signal from computer to: (a) Close LH_2 recirculation return line valve (1) (b) Close LOX recirculation return line valves (5) (c) Close LH_2 recirculation pump discharge valves (5).	
147.7	S-II	Signal from the computer to initiate J-2 engine start sequence	The S-IC/S-II stages are separated by a minimum of 31 cm (1 ft) at this time. The J-2 engine chilldown begins at this time. When the 0.5 second chilldown timers expire the start tank discharge valves open regardless of whether the thermocouples indicate proper chilldown temperature. Physical separation signal is interlocked in the S-II engines start command. The thermocouple override signals to the S-II engines are supplied when power is transferred to the S-II stage.

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
147.85	S-IC	Close outboard engine fuel prevalves.	A 1.55 second timer, located on the S-IC stage, will be started at outboard engine cutoff. Expiration of the timer will cause fuel prevalves to close.
148.2	S-II	Signal from engine sequence to open start tank discharge valves.	This signal is initiated by an engine timer 0.5 second after engine start sequence is initiated.
148.8	S-II	Engine mainstage signal from the engine sequencer.	This signal occurs approximately 0.6 second after start tank discharge signal (typical 5 engines). At this time, if augmented spark igniter combustion in the thrust chamber is not detected or if the start tank is not depressurized, cutoff will occur, otherwise, the signal will energize the mainstage control solenoid valve.
149.0	S-II	Signal from computer to unlock hydraulic accumulators.	Unlocking the hydraulic accumulators enables gimballing of the S-II stage engines.
149.1	S-II	J-2 Engines at 10 percent thrust.	The J-2 engines reach 10 percent thrust approximately 1.4 seconds after S-II engine start sequence is initiated.
150.9	S-II	J-2 Engines at 90 percent thrust.	The J-2 engines reach 90 percent thrust approximately 3.2 seconds after S-II engine start sequence is initiated.
153.2	S-II	Signal from computer to activate Propellant Utilization system.	
153.6	S-II	Signal from computer to arm start phase limiter.	A start sequence halt, due to timer malfunction, etc., will prevent the malfunction cutoff circuitry being armed by the engine sequencer. This signal is a backup for arming the mainstage OK switch to give cutoff if a malfunction in the engine sequencer has occurred. This signal will enable the individual cutoff circuitry of each J-2 engine to shutdown the engine when mainstage OK is not energized.
154.6	S-II	Signal from computer to disarm start phase limiter.	This signal prevents inadvertent engine cutoff before depletion.
TBD	IU	Signal from computer to open solenoid valve connecting IU H_2O reservoir and in-flight heat exchanger.	No cooling is available for the IU from the end of the prelaunch phase until this time. The approximate time this event will occur is LO + 160.0 seconds to LO 165.0 seconds. The exact time that this condition will occur will be determined at a later date.

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
176.9	S-II	Signal from computer to trigger S-IC/S-II interstage separation devices (second plane separation).	
181.9	LES	Signal from computer to jettison launch escape system.	The launch escape system is jettisoned approximately 5 seconds after interstage separation.
398.9	S-II	Signal from computer to activate LOX step pressurization.	The LOX and LH_2 pressurization regulators are locked open at this time.
399.0	S-II	Signal from computer to activate LH_2 step pressurization.	
448.3	S-II	Signal from computer to arm S-II LOX depletion sensors.	
448.4	S-II	Signal from computer to arm S-II LH_2 depletion sensors.	
TBD	S-IVB	Signal from computer to open S-IVB prevalves.	The time and method for opening the S-IVB prevalves will be determined at a later date.
521.9	S-II	Signal to cut off J-2 engines.	The computer time base is reset at this time. Simultaneous shutdown of all five J-2 engines is initiated by any two of five propellant depletion sensors, (located 5 in LOX tank and 5 in LH_2 tank), sensing the shutoff level of either the LOX or LH_2 propellant tanks.
522.0	S-IVB	Signal from computer to turn off 305W instrument heaters.	The 305W instrument heaters are required to maintain a minimum temperature of -18.3°C (-65°F) in the flight instrumentation packages when the S-IVB engine is inoperative.
522.1	S-IVB	Signal from computer to trigger S-IVB ullage rockets (2).	The effective burning time of the S-IVB ullage rockets is approximately 4 seconds. The ullage rockets must burn ullage rockets must burn until enough thrust is present in the J-2 engine to maintain propellants seating (approximately $3\ ^{+0.5}_{-0}$ seconds).
522.2	S-II/ S-IVB	Signal from computer to: (a) Fire separation device (b) Fire retrorockets (8).	The time shown represents the time which the J-2 engine should be at 10 percent thrust. This time will be updated as more firm data becomes available on the J-2 thrust decay. Circuit delays of approximately 10 to 15 ms are built in to the separation circuitry so that retrorocket ignition occurs after separation device ignition to prevent possible unseating of the S-IVB stage propellants.

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
522.275	S-II/ S-IVB	Separation structure completely severed.	Occurs approximately 0.075 second after separation signal from the computer. First possible S-IVB axial motion relative to S-II.
522.3	S-IVB	Signal from computer to turn on 45 W instrument heaters.	The 45 W instrument heaters are required to maintain a minimum temperature of -18.3°C (-65°F) in the flight instrumentation packages when the S-IVB engine is operative.
522.325	S-II	Signal to close LH_2 and LOX prevalves.	Engine shutoff signal indicates a timer which upon expiration will close the S-II prevalves. The minimum time between engine shutoff and prevalve closing signal is 0.425 second.
522.335	S-II	Retrorocket thrust buildup begins.	Occurs approximately 0.135 second after separation signal from the computer. Successful separation can be accomplished with one retrorocket malfunctioning. The effective burn time of the retrorockets is 1.5 seconds.
522.4	S-IVB	Signal from computer to activate S-IVB roll control system.	This signal enables the auxiliary propulsion system to control roll.
523.1	S-IVB	Signal from computer to shut off fuel chilldown pump.	
523.2	S-IVB	Signal from computer to shut off LOX chilldown pump.	
523.4	S-IVB	Signal from computer to close LOX and LH_2 recirculation pump discharge valves.	
523.6	S-IVB	Signal from computer to give engine ready bypass.	This signal is effective only on unmanned flights. This signal prevents the engine from being cut off by any of the malfunction cutoff modes, which are: (a) Start tank depressurized (b) Mainstage not OK.
523.7	S-IVB	Signal from computer to initiate S-IVB engine start sequence.	This is the time when a minimum of 3.1 m (10 ft) clearance between S-IVB engine and separated aft interstage is reached with one retrorocket out. J-2 engine chilldown begins at this time. The J-2 engine contains a sequencer which sequences the necessary commands to the engine for starting. The engine start sequence shown here is based on ground prechill of the thrust chamber.
523.8	S-IVB	Signal from computer to bypass separation interlock in S-IVB engine start.	This interlock will be bypassed for unmanned flights only.

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
524.1	S-IVB	Signal from computer to enable LH_2 flight pressurization.	The LH_2 flight control pressure switch is enabled to control the LH_2 pressurization control solenoid valve at this time. The step pressurization solenoid valve is closed at this time and remains closed until the end of S-IVB first burn.
524.2	S-IVB	*Signal from engine sequencer to open start tank discharge valve.	This signal is initiated by a timer 0.5 second after initiating S-IVB engine start sequence. If the engine bell is not at the proper temperature at this time, the start tank discharge valve will not open and an additional 0.5 second is permitted for further chilldown. If the thermocouple signal indicating proper temperature is still not present at the end of this time, the thermocouple override signal is supplied.
524.7	S-IVB	Signal from computer to override thermocouple signal.	The start tank discharge valve will open at this time regardless of whether the thermocouple signal is present.
524.8	S-IVB	*Engine mainstage signal from the engine sequencer.	This signal occurs 0.6 second after start tank discharge signal. The engine mainstage control solenoid valve is energized at this time.
524.8	S-IVB	Signal from computer to initiate engine gimballing.	The switching occurs within the IU. This signal switches engine position control from the S-II to the S-IVB.
525.1	S-IVB	*J-2 engine at 10 percent thrust.	The J-2 engine reaches 10 percent thrust approximately 1.4 seconds after initiation of S-IVB engine start sequence.
526.0	S-IVB	Signal from computer to switch control of oxidizer pressurization valves.	Control of LOX tank pressure is switched from the main pressurization shutoff valve to the heat exchanger bypass valve. The main pressurization shutoff valve remains open until completion of first burn. Pressure switch controls LOX flight pressurization.
526.9	S-IVB	*J-2 engine at 90 percent thrust.	The J-2 engine reaches 90 percent thrust in approximately 3.2 seconds after initiation of engine start sequence.
528.2	S-IVB	Signal from computer to activate PU system.	
		*Indicates items will occur 0.5 second later if the thermocouple override signal is required.	

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
537.0	S-IVB	Signal from computer to jettison S-IVB ullage rockets.	
693.5	S-IVB	Signal to cut off J-2 engine.	J-2 engine cutoff time will be determined by guidance parameters. The time shown is approximate.
693.7	S-IVB	Signal from computer to deactivate engine control.	Engine control is deactivated in the IU. This signal disables engine gimballing.
693.8	S-IVB	Signal from computer to activate pitch and yaw control.	Pitch and yaw control is activated in the IU. This signal enables the APS to control pitch and yaw.
693.8	S-IVB	Signal from computer to turn on 312 Newton (70 pound) ullage engines.	The 312 Newton (70 pound) ullage engines are turned on to seat the propellants prior to continuous venting.
693.9	S-IVB	Signal from computer to switch auxiliary hydraulic pump to thermal mode.	A thermal switch is enabled to control the auxiliary hydraulic pump at this time. The thermal switch controls the running time of the hydraulic pump so that a predetermined maximum and minimum temperature of the hydraulic fluid is maintained.
694.0	S-IVB	Signal from computer to close LOX and LH_2 prevalves.	The prevalves are reopened in one minute. The main fuel and LOX valves must have sufficient time to close before the prevalves are closed. The minimum closing time of the LOX and LH_2 prevalves after engine cutoff is 0.425 second.
694.1	S-IVB	Signal from computer to reset auxiliary hydraulic pump flight mode command relay.	The flight mode command relay must be reset in order to have the auxiliary hydraulic pump in the coast mode.
694.2	S-IVB	Signal from computer to disable LH_2 flight pressurization.	This signal resets the first burn relay and disables the pressure switch controlling the LH_2 control solenoid valve.
694.3	S-IVB	Signal from computer to deactivate PU system.	
694.4	S-IVB	Signal from computer to close LOX pressurization main shutoff valves.	This signal sets the first burn relay which closes the main fuel shutoff valves.
694.6	S-IVB	Signal from computer to turn OFF 45 W engine instrument heaters.	
694.7	S-IVB	Signal from computer to turn ON 305 W engine instrument heaters.	
		*Indicates items will occur 0.5 second later if the thermocouple override signal is required.	

Table 4.3-3 Saturn V Flight Sequence, Phases 2 through 5 - Powered Flights and Orbital Coast (Cont)

Time From Lift-off	Stage	Event	Remarks
696.0	S-IVB	Signal from computer to switch out PU boiloff bias.	The PU boiloff bias is switched out before second burn so propellants will be burned at the proper mixture to obtain minimum residual.
696.1	S-IVB	Signal from computer to initiate engine purges.	The J-2 engine must be purged for 10 minutes after engine shutdown. Solenoid valve is opened to supply an engine cavity purge at this time. Pressure switch controls the engine purge solenoid valve.
700.5	S-IVB	Signal from computer to open LH_2 continuous vent valve.	
743.6	S-IVB	Signal from computer to shutdown 312 Newton (70 pound) ullage engines.	
754.0	S-IVB	Signal from computer to open LOX and LH_2 prevalves.	The LOX and LH_2 prevalves are reopened to prevent LOX and LH_2 from being trapped between the prevalves and the LOX and LH_2 main propellant valves for an extended period of time.
754.1	S-IVB	Signal from computer to open LOX and LH_2 recirculation pump discharge valves.	
1293.5	S-IVB	Signal from computer to terminate engine purges.	
S-IVB Orbital Coast ↓			S-IVB Orbital Coast ↓

Table 4.3-4 Saturn V Flight Sequence, Phases 6 and 7 - S-IVB Restart and Docking

Time From Restart	Stage	Event	Remarks
T-327.0	S-IVB	Signal to begin restart preparations.	Restart preparations are initiated by a signal from the ground. The ground signal will reset the computer time base and start automatic sequencing for S-IVB restart.
T-326.9	S-IVB	Signal from computer to turn on 312 Newton (70 pound) ullage engines.	The 312 Newton (70 pound) ullage engines are turned on to seat propellants for S-IVB restart.
T-326.8	S-IVB	Signal from computer to switch auxiliary hydraulic pumps to engine start mode.	The thermal switch controlling the auxiliary hydraulic pump is bypassed at this time and the auxiliary hydraulic pump runs continuously.

Table 4.3-4 Saturn V Flight Sequence, Phases 6 and 7 - S-IVB Restart and Docking (Cont)

Time From Restart	Stage	Event	Remarks
T-326.7	S-IVB	Signal from computer to reset auxiliary hydraulic pump coast-mode command relay.	This signal deactivates the thermal switch controlling the auxiliary hydraulic pump.
T-326.0	S-IVB	Signal from computer to close continuous venting valve.	
T-325.3	S-IVB	Signal from computer to close prevalves.	
T-325.2	S-IVB	Signal from computer to repressurize fuel tank.	This signal enables the LH_2 repressurization pressure switch to control the repressurization solenoid valve which supplies ambient helium for LH_2 repressurization.
T-324.8	S-IVB	Signal from computer to start LOX chilldown pump.	The LOX chilldown pump is started to condition the LOX system for restart.
T-322.0	S-IVB	Signal from computer to start LH_2 chilldown pump.	The fuel chilldown pump is started to condition the LH_2 system for restart.
T-22.0	S-IVB	Signal from computer to open LOX and LH_2 prevalves.	The LOX and LH_2 prevalves are opened at this time to insure against bubbles in the suction lines at engine start. The time shown is preliminary.
T-21.9	S-IVB	Signal from computer to repressurize LOX tank.	This signal enables the LOX repressurization pressure switch to control the repressurization solenoid valve which supplies ambient helium for LOX repressurization.
T-0.7	S-IVB	Signal from computer to disable LH_2 repressurization.	The LH_2 repressurization system is disabled at this time.
T-0.6	S-IVB	Signal from computer to shut off fuel chilldown pump.	
T-0.5	S-IVB	Signal from computer to shut off LOX chilldown pump.	
T-0.4	S-IVB	Signal from computer to close recirculation pump discharge valves.	
T-0.3	S-IVB	Signal from computer to disable LOX repressurization.	The LOX repressurization system is disabled at this time.
T-0.2	S-IVB	Signal from computer to turn OFF 305 W engine instrument heater.	The 305 W instrument heaters are required to maintain a minimum temperature of -18.3°C (-65°F) in the flight instrumentation packages when the S-IVB engine is inoperative.
T-0.1	S-IVB	Signal from computer to turn ON 45 W engine instrument heater.	The 45 W instrument heaters are required to maintain a minimum temperature of -18.3°C (-65°F) in the flight instrumentation packages when the S-IVB engine is inoperative.

Table 4.3-4 Saturn V Flight Sequence, Phases 6 and 7 - S-IVB Restart and Docking (Cont)

Time From Restart	Stage	Event	Remarks
TBD	S-IVB	Signal from computer to enable main LOX pressurization shutoff valve.	The LOX pressurization switch controls the LOX pressurization main shutoff valve and the LOX pressurization main shutoff valve is opened any time the LOX tank ullage pressure is low.
T-0	S-IVB	Signal from computer to initiate engine start sequence.	J-2 engine chilldown begins at this time. The J-2 engine contains a sequencer which sequences the necessary commands to the engine for starting.
T + 0.1	S-IVB	Signal from computer to give engine ready bypass.	This interlock will be bypassed for unmanned flights only. This signal prevents the engine from being cut off by any of the malfunction cutoff modes which are: (a) Start tank depressurized (b) Mainstage not OK.
T + 0.4	S-IVB	Signal from computer to deactivate the APS pitch and yaw control channels.	Pitch and yaw control is disabled in the IU. This signal disables the APS for pitch and yaw control.
T + 0.5	S-IVB	**Signal from engine sequencer to open start tank discharge valve.	This signal is initiated by a timer 0.5 second after initiating S-IVB engine start sequence. If the engine bell is not at the proper temperature at this time, the start tank discharge valve will not open and an additional 0.5 second is permitted for further chilldown. If the thermocouple signal indicating proper temperature is still not present at the end of this time, the thermocouple override signal is supplied.
T + 0.5	S-IVB	Signal from computer to enable J-2 engine gimballing.	J-2 engine's gimballing is enabled in the IU.
T + 1.0	S-IVB	Signal from computer to override thermocouple signal.	The start tank discharge valve will open at this time regardless of whether the thermocouple signal is present. If the override signal is required, events marked ** will occur 0.5 second later than shown.
T + 1.1	S-IVB	**Engine mainstage signal from the engine sequencer.	The signal occurs 0.6 second after start tank discharge signal. The engine mainstage control solenoid is energized at this time.
		**These events occur 0.5 second later than shown if the thermocouple override signal initiates the opening of the start tank discharge valve.	

Table 4.3-4 Saturn V Flight Sequence, Phases 6 and 7 - S-IVB Restart and Docking (Cont)

Time From Restart	Stage	Event	Remarks
T + 1.4	S-IVB	**J-2 engine at 10 percent thrust.	The J-2 engine reaches 10 percent thrust approximately 1.4 seconds after S-IVB engine start sequence is initiated.
T + 2.3	S-IVB	Signal from computer to switch control of oxidizer pressurization valves.	The control of LOX tank pressure is switched from the main shutoff valves to the bypass valve.
T + 3.0	S-IVB	Signal from computer to shut off 312 Newton (70 pound) ullage engine.	
T + 3.2	S-IVB	**J-2 engine at 90 percent thrust.	The J-2 engine reaches 90 percent thrust approximately 3.2 seconds after S-IVB engine start sequence is initiated.
T + 3.2	S-IVB	Signal from computer to set second burn command relay.	This signal enables LH_2 step pressure switch to control the LH_2 step pressurization solenoid valve during second burn of the S-IVB stage.
T + 5.5	S-IVB	Signal from computer to activate the PU system.	
TBD	S-IVB	Signal from computer to arm propellant depletion point level sensors.	Three LOX depletion sensors and three LH_2 depletion sensors are armed at this time. Actuation of any 2 of 3 depletion sensors in either propellant tank will initiate engine cutoff.
T + 313.1	S-IVB	Signal to cut off J-2 engine.	The time shown for S-IVB shutoff is nominal and will vary with the vehicle mission. If propellant depletion occurs before guidance parameters cut off the S-IVB engine, the engine will be shutdown by the propellant depletion sensors. Either method of cutoff should reset the computer time base.
T + 313.4	S-IVB	Signal from computer to deactivate main engine control.	Engine control is activated in the IU. This signal disables engine gimballing.
T + 313.5	S-IVB	Signal from computer to reactivate pitch and yaw control.	Pitch and yaw control is activated in the IU. This signal enables the APS to control pitch and yaw.
T + 313.6	S-IVB	Signal from computer to close LOX and LH_2 prevalves.	The main fuel and LOX valves must have sufficient time to close before the prevalves are closed. The minimum closing time of the LOX and LH_2 prevalves after engine cutoff is 0.425 second.
		**These events occur 0.5 second later than shown if the thermocouple override signal initiates the opening of the start tank discharge valve.	

Table 4.3-4 Saturn V Flight Sequence, Phases 6 and 7 - S-IVB Restart and Docking (Cont)

Time From Restart	Stage	Event	Remarks
T + 313.7	S-IVB	Signal from computer to shut off auxiliary hydraulic pump.	This signal will reset the auxiliary hydraulic pump flight mode command relay.
T + 313.8	S-IVB	Signal from computer to reset second-burn command relay.	This signal disables the LH_2 step pressure switch controlling the LH_2 step pressurization solenoid valve.
T + 313.9	S-IVB	Signal from computer to deactivate PU system.	
T + 314.0	S-IVB	Signal from computer to turn OFF 45 W instrument heater.	The temperature of the S-IVB heater package does not need to be controlled after this time.
T + 315.3	S-IVB	Signal from computer to shut off main LOX pressurization shutoff valves.	
TBD		Jettison forward section of IU/Apollo interstage adapter.	No details available at this time.
TBD		Command and Service Module (CSM) separation from Lunar Excursion Module/ IU/S-IVB and CSM turn around.	
TBD		CSM docking to LEM/IU/S-IVB.	
		NOTE: The major mission of the SA-501 after S-IVB second burn is CM/SM separation and CM reentry at 10,900 mps (36,000 fps). LOX and LH_2 venting capabilities should be available in event of mission redefinitions.	

CHAPTER 5

MEASURING AND TELEMETRY

TABLE OF CONTENTS

SECTION 5.1

INTRODUCTION

The combined measuring and telemetry system is essentially an independent operating subsystem within the overall Astrionics System.

The combined measuring and telemetry systems of the Saturn Launch Vehicles measure physical quantities and signals onboard the vehicle and transmit the data to ground stations. The complexity of the launch vehicle and its missions dictate a large number of measurements. The data transmitted by the measuring and telemetry systems supply information for the following operations:

- Automatic preflight checkout of the vehicle.
- Monitoring of vehicle performance during powered flight.
- Postflight evaluation of vehicle performance.
- Monitoring and checkout of the vehicle during orbital flight.
- Verification of commands received in the vehicle from ground stations.

Figure 5.1-1 illustrates the signal flow through the system. The transducers convert the physical quantities to be measured (e.g., pressure, temperature, etc.) into electrical signals. These transducer signals are modified by signal conditioning devices into voltages suitable as inputs to the telemetry system. The measuring distributor feeds the conditioned transducer signals to the telemetry system. In the telemetry system the signals are modulated on RF

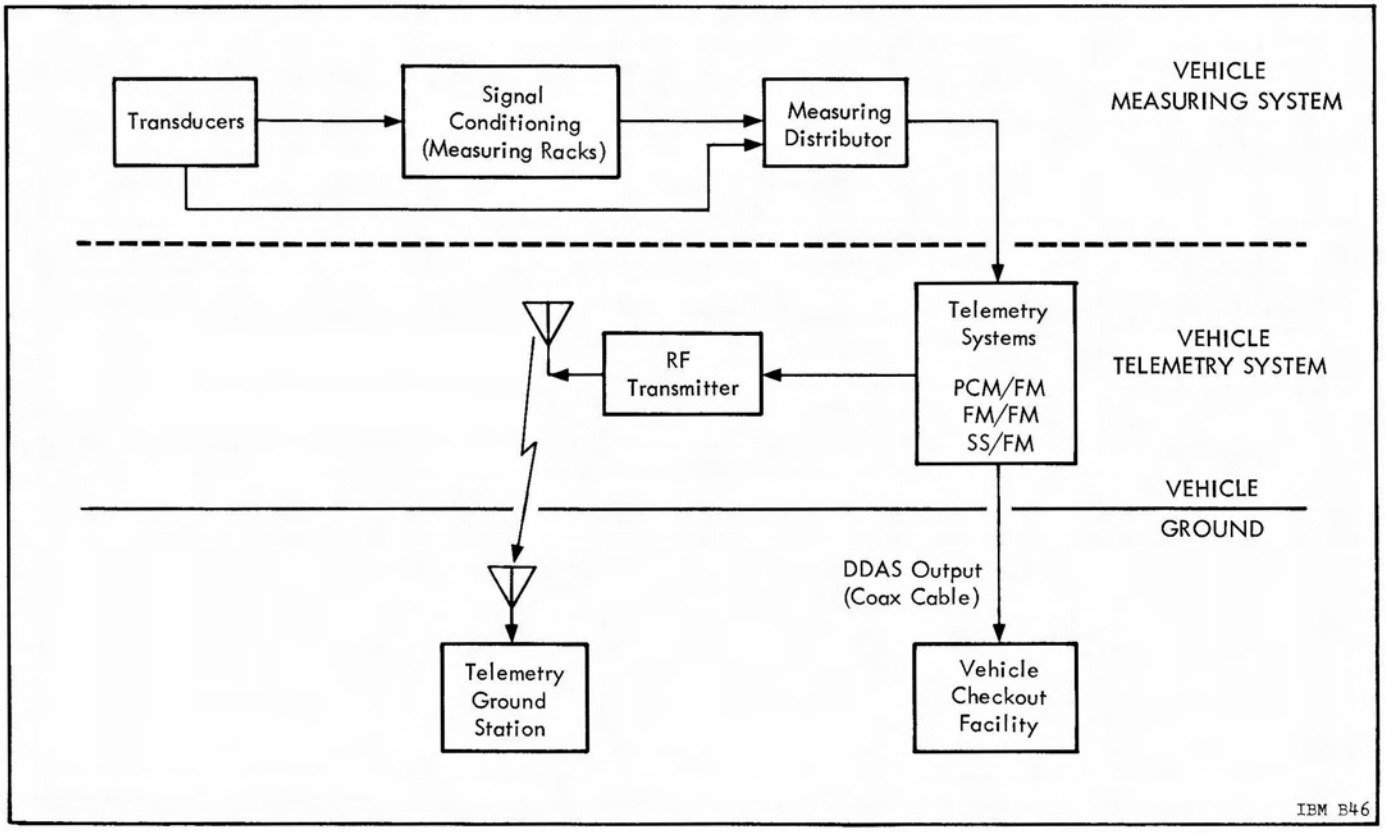


Figure 5.1-1 Measuring and Telemetry System

carriers and transmitted during flight to the telemetry ground stations. Before launch, the measuring and telemetry systems send digital data by coaxial cable from each stage of the vehicle to the checkout facility. The digital information is used for automatic checkout of the vehicle on the launch pad. In this mode of operation the telemetry system is called the digital data acquisition system. Figure 5.1-1 also indicates the division between the measuring system and the telemetry system.

Each stage of the launch vehicle has an independent measuring and telemetry system, DDAS output, and RF transmission. The telemetry system of the S-IVB Stage is also connected to the telemetry system in the IU for the purpose of digital data acquisition and alternate mode transmission. For monitoring of digital data, the IU telemetry system has an interface with the LVDC through the LVDA.

To simplify vehicle checkout, data handling, etc., standardization is practiced wherever feasible. A remote automatic checkout system is standardized on each stage to provide automatic checkout of measurements from ground equipment. This system greatly minimizes checkout time.

SECTION 5.2

MEASURING SYSTEM

5.2.1 GENERAL

The measuring system includes transducers, measuring racks (which contain the signal conditioning modules), measuring distributors, measuring rack selectors, and measuring voltage supplies. The measuring system converts the signal or quantity to be measured into an electrical signal that is acceptable to the telemetry system. According to this definition, the measuring system ends at the input to the telemetry system (at the subcarrier oscillator, multiplexer, etc.). Figure 5.2-1 illustrates typical components of the measuring system. The measurements in the launch vehicle cover the areas of:

Propulsion	Guidance and control
Structure	Environment
Flight mechanics	

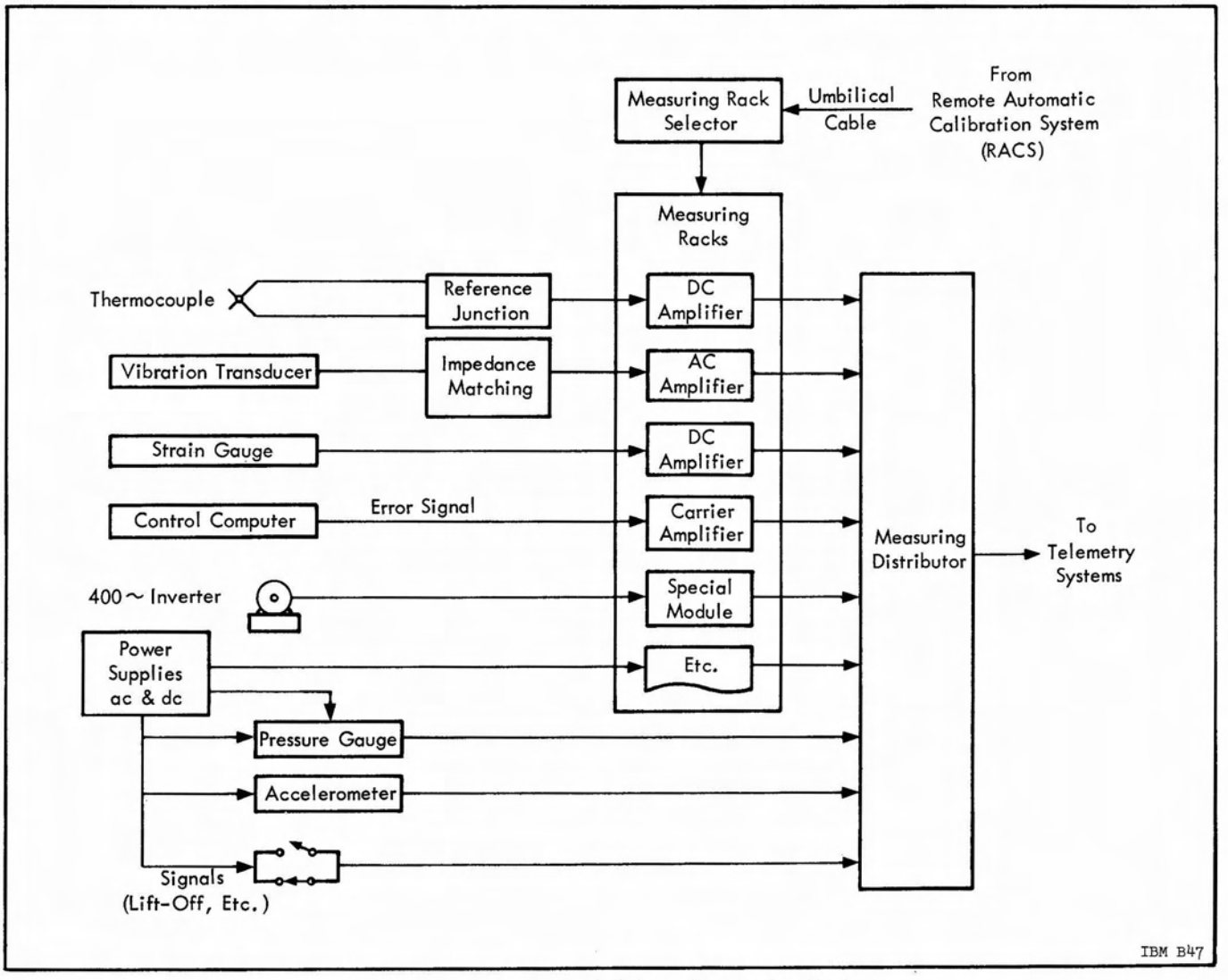


Figure 5.2-1 Typical Saturn Measuring System

Physical quantities to be measured, such as, pressure, temperature, and vibrations must be transformed by transducers into electrical signals for transmission by telemetry. Measurements of electrical signals (voltages, currents, and frequencies) originating in onboard equipment are used for monitoring the performance of this equipment and the sequence of flight events (e. g., stage separation, engine cutoff, and others). The signals to be measured exist in analog and digital form. Measurements of electrical signals do not require transducers.

The number of measurements made in the various stages of Saturn IB and V Launch Vehicles are listed in Table 5.2-1. A larger number of measurements is necessary for performance evaluation and testing of research and development vehicles, while for operational vehicles, this number is reduced considerably. Because of the large number of different measurements, no detailed list of measurements is given. Table 5.2-2 indicates some of the quantities measured in the S-IC Stage, the S-IVB Stage, and the Instrument Unit of the Saturn V Research and Development and Operation Vehicles.

Certain measurements will be used as inputs to the emergency detection system (see Chapter 4). Operational measurements are those measurements used for flight (mission) control. Operational measurements indicate the state of the vehicle and its systems and also provide trend information (beginning with the orbital flight phase). All operational measurements are transmitted over the PCM telemetry links of the S-IVB Stage and the IU. Typical operational measurements for the Saturn V Vehicles are given in Table 5.2-3.

The number and type of measurements given in the tables are best estimates and are subject to changes as the development of vehicles proceeds. This applies particularly to the figures for operational vehicles.

Table 5.2-1 Number of Measurements, Transducers, and Measuring Racks

SATURN IB						
Stage	Measurements R & D	Measurements Oper	Transducers R & D	Transducers Oper	Measuring Racks R & D	Measuring Racks Oper
S-IB	542	263	305	106	19	5
S-IV B	432	218	298	115	17*	7*
IU	278	134	92	45	9	5
Total Vehicle	1252	615	695	366	45	17
SATURN V						
Stage	Measurements R & D	Measurements Oper	Transducers R & D	Transducers Oper	Measuring Racks R & D	Measuring Racks Oper
S-IC	901	297	723	157	27	5
S-II	913	446	589	180	35	8
S-IV B	432	218	298	115	17*	7*
IU	278	134	92	45	9	5
Total Vehicle	2524	1077	1702	497	88	25

* Signal conditioning panels

5.2.2 TRANSDUCERS

Transducers are electromechanical measuring instruments which contain sensitive devices for converting mechanical quantities into electrical signals. Evaluation of vehicle performance and in-flight monitoring requires the measurement of a large variety of physical quantities onboard the vehicle. Therefore, many different types of transducers are used. Some typical transducers and the corresponding measurements are listed in Table 5.2-2. Because of the many types of transducers and measurements used in launch vehicles, no attempt is made to give a complete description of all transducers on each stage. The following measurement descriptions generally apply to the S-IB and S-IC Stages. The number of transducers used in each stage may be found in Table 5.2-1. Figure 5.2-2 illustrates several typical transducers.

BENDING MODE VIBRATION MEASUREMENTS (ALL STAGES)

Bending measurements are made using force-balance accelerometers. The principle of operation of the force-balance accelerometer is shown in Figure 5.2-3. These instruments operate as a sub-

Table 5.2-2 Typical Saturn V Measurements

Quantity Measured	Typical Transducer	Number of Measurements					
		S-IC		S-IVB		IU	
		R&D	Oper	R&D	Oper	R&D	Oper
Acoustic energy	Microphone	4	0	6	0	1	0
Temperature	Resistance thermometer thermocouple	257	61	163	50	56	30
Pressure	Vibration pressure transducer & other types	235	82	72	46	13	6
Vibration	Piezoelectric accelerometer	80	10	38	6	29	6
Propellant flow rate	Flowmeter	105	0	4	4	11	1
Liquid level	Level probe	17	8	6	6	—	—
Strain	Strain gauge	68	0	12	0	—	—
RPM (turbopump)	Tachometer	5	5	2	2	—	—
Acceleration	Force balance accelerometer	3	1	1	1	6	6
Voltage, current, and frequency	—	11	11	38	30	15	12
Signals	—	97	97	53	53	6	6
Guidance and Control Signals	—	—	—	—	—	58	45
RF & telemetry signals	—	—	—	—	—	28	6
Angular velocity	Rate gyro	—	—	—	—	35	3

Table 5.2-3
Typical Saturn V Operational Measurements

S-IVB Auxiliary Propulsion System

- Propellant level
- Helium supply pressure
- Propellant temperature

S-IVB Main Propulsion System

- Gas supply pressure
- Propellant valve positions
- Propellant masses
- Engine sequencing signals
- Tank pressure
- Propellant flow
- Thrust chamber pressure
- Hydraulic system pressure and fluid temperature

S-IVB/IU Electrical System

- Battery voltages and currents
- Bus voltages and currents
- Inverter voltages

S-IVB Attitude Control and Stabilization System

- Attitude control signals (pitch, yaw, roll)
- Angular velocity (pitch, yaw, roll)
- Engine actuators position
- Control computer temperature
- Servo amplifier signals
- Spacial amplifier signals
- Valve positions

Navigation, Guidance, and Digital Signal

- Steering commands (pitch, yaw, roll)
- Space fixed velocity (3 components)
- Space fixed displacement (3 components)
- Computer time
- Time to S-IVB second ignition and cutoff
- Accelerometer output (X, Y, Z)
- Gyro servo output (X, Y, Z)
- Gimbal angles (pitch, yaw, roll)
- Launch Vehicle Digital Computer signals
- Temperatures of computer and platform components
- Air bearing supply pressure
- Switch Selector output

Environmental Control System

- Pressure and temperature of coolant at several places
- Cold plate temperature
- Gas supply pressure

Instrumentation and Communication System

- Power output of the PCM transmitter (S-IVB & IU)

miniature servosystem, which is responsive to linear acceleration along its sensitive axis. Due to inertia, the acceleration sensitive mass, commonly called the paddle wheel, moves relative to the position detector when acceleration is applied. The position-error detector and servoamplifier generate a feedback signal to the restoring mechanism. The electromechanical servoaction results in a balance between the input force proportional to the acceleration and the feedback force proportional to the current in the restoring coil. The restoring current, or the voltage it develops across a series resistor, provides the output of the accelerometer, and is a precise measurement of acceleration.

The advantage of the force-balance accelerometer over earlier potentiometer type accelerometers is that friction is almost negligible. The force-balance accelerometer will sense both extremely slow vibrations and continuous acceleration in a single direction. Their measuring range is 0.5g. The same instruments are employed to sense lateral acceleration along the pitch and yaw axes in the IU. Similar measurements are also made to determine the bending or flapping actions of the vehicle fins. The instruments used to sense this movement have a range of ±0.1g.

FLIGHT MECHANICS MEASUREMENTS

Longitudinal acceleration measurements are made to measure the thrust decay of engines. These measurements are made with the same type of accelerometers that are used for strain and vibration measurements. Longitudinal acceleration measurements to determine thrust and thrust decay of the S-IVB Stage are made in the IU.

Angular velocity measurements are made using Rate Gyros (see Chapter 3). The instrument is accurate within a range of ±10 degrees per second. In case of a catastrophic situation, the vehicle also carries Rate Gyros to measure angular movement in excess of 100 degrees per second along the pitch and yaw axis.

Propulsion system measurements are made by pressure transducers, flowmeters, tachometers, and liquid level sensors. A brief functional description for each is given in the following paragraphs.

PRESSURE MEASUREMENTS

Pressure measurements are made by two different methods: potentiometric and strain gage.

The potentiometric transducer is basically a wirewound potentiometer with the wiper mechanically connected to a pressure controlled diaphragm as illustrated in Figure 5.2-4. The output voltage is obtained by applying 5 volts to the potentiometer. The magnitude of the output will vary from 0 to 5 volts, depending upon the position of the wiper. Since the output voltage is within the limit required by the sub-carrier oscillator, no signal conditioning is required. Approximately 70 per cent of the total pressure measurements are made with the potentiometric type transducer.

On the S-IB Stage most of the potentiometric type pressure transducers may be calibrated while on board the vehicle by using the calibration valve that is associated with each transducer. The calibration valve, connected between the transducer and the source of pressure being measured, may be coupled to a calibration line that is connected through a quick disconnect coupling to a controlled pressure source. When the calibration line is connected to the valve, the transducer sensor is mechanically positioned to sense the controlled pressure. The transducer automatically returns to sense the system pressure when the calibration line is removed. All other type pressure transducers are calibrated electrically.

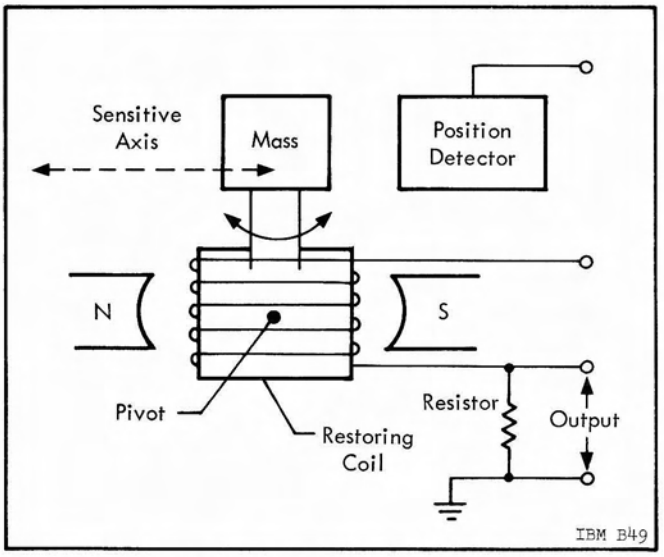


Figure 5.2-3 Force-balance Accelerometer Block Diagram

In addition to the potentiometric pressure transducer, pressure measurements are made with unbonded strain gages (Figure 5.2-5). Each strain gage transducer consists of four individual strain gages mechanically connected to a pressure sensitive diaphragm and arranged in such a manner that compression on two of the gages results in tension on the

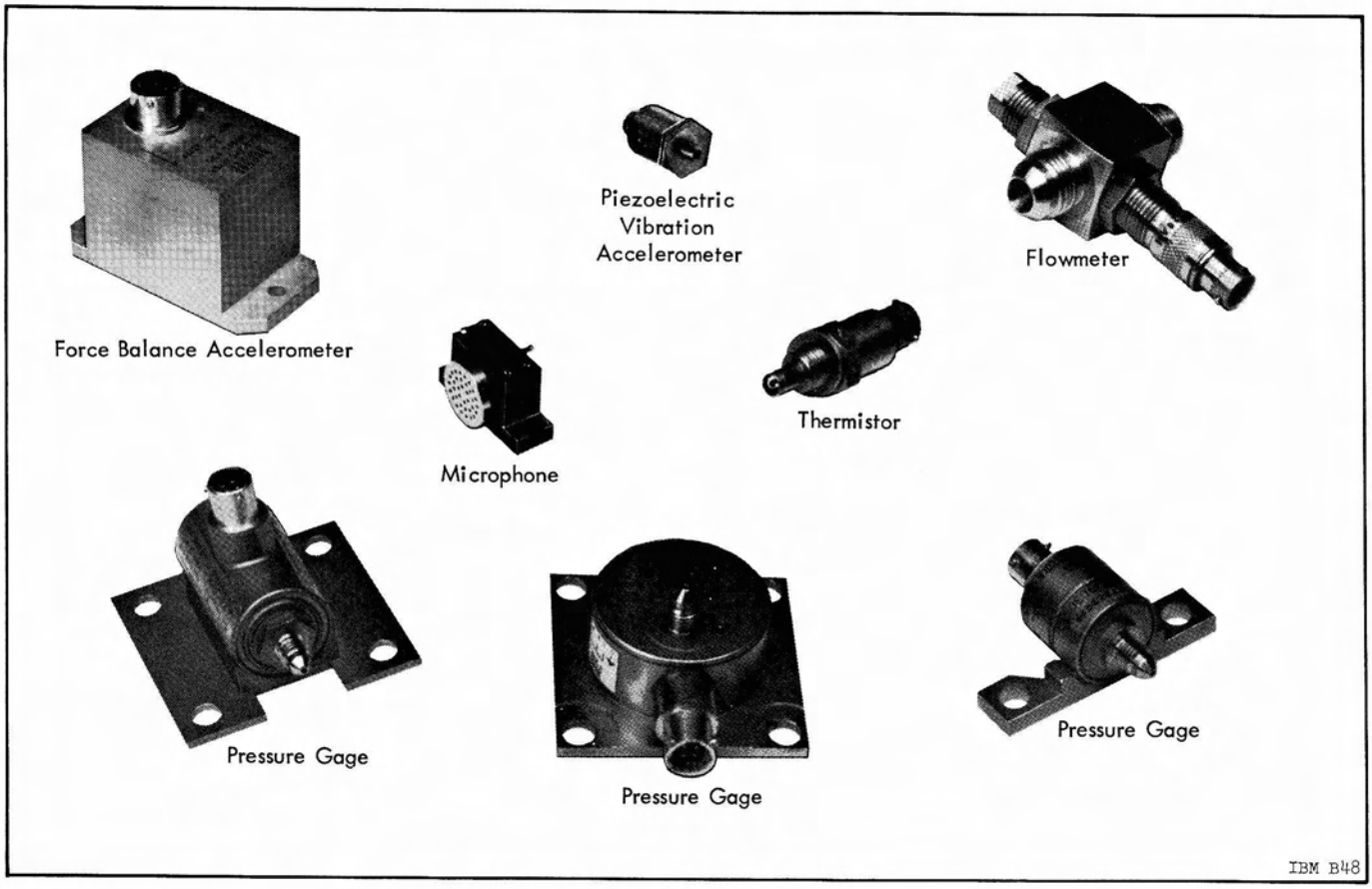


Figure 5.2-2 Typical Transducers

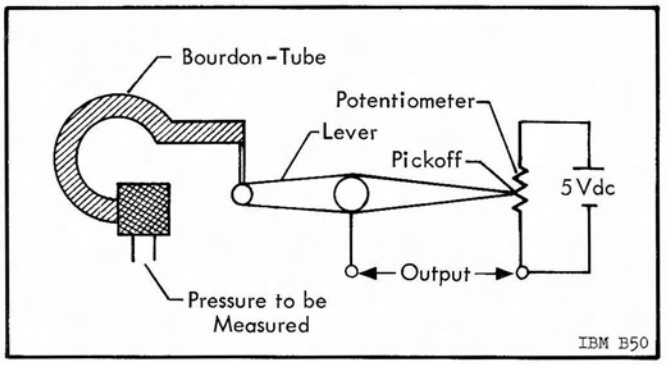


Figure 5.2-4 Bourdon-tube Potentiometer Type Pressure Transducer

other two. This action, in effect, results in an output when the strain gage transducer is excited by an external voltage. The output voltage of the strain gage transducer is approximately 40 millivolts at full pressure; therefore, the signal must be fed into a signal conditioner (dc amplifier) before it can be applied to the subcarrier oscillator. In some cases, the signal conditioning is incorporated in the transducer package.

RPM MEASUREMENTS (S-IB STAGE ONLY)

This measurement utilizes a variable reluctance type of tachometer mounted on the turbine. As the turbine turns, the varying reluctance of a magnetic path generates an ac voltage. The frequency of the output voltage is proportional to the rpm of the turbine. This frequency is too high for the bandwidth of the available telemetry channels; therefore, signal conditioning is required to divide the frequency by 32 to make the output signal compatible with available telemetry channels.

The signal conditioner is a magnetic frequency divider which uses the rectangular hysteresis characteristics of a saturable core.

LIQUID LEVEL MEASUREMENTS (S-IB STAGE ONLY)

The liquid level of the propellant is measured by two different methods: the discrete and the continuous method. The discrete method (Figure 5.2-6) utilizes a photo-electric cell to obtain signal output. The sensor consists of a light source, photo-electric cell, and a prism. Because the liquid diffuses the light rays, no output is obtained until the level of the liquid drops below the prisms. As the level of the liquid drops below the prism, light rays from the light source are reflected back to the photo-electric cell by the prism faces, which are at 45-degree angles to the light rays. Fifteen sensors are located along the length of the tank. When the output from one sensor is detected, it is possible to determine the amount of propellant (fuel or lox) that was consumed in the time interval that lapsed between outputs from this sensor and one that was previously initiated.

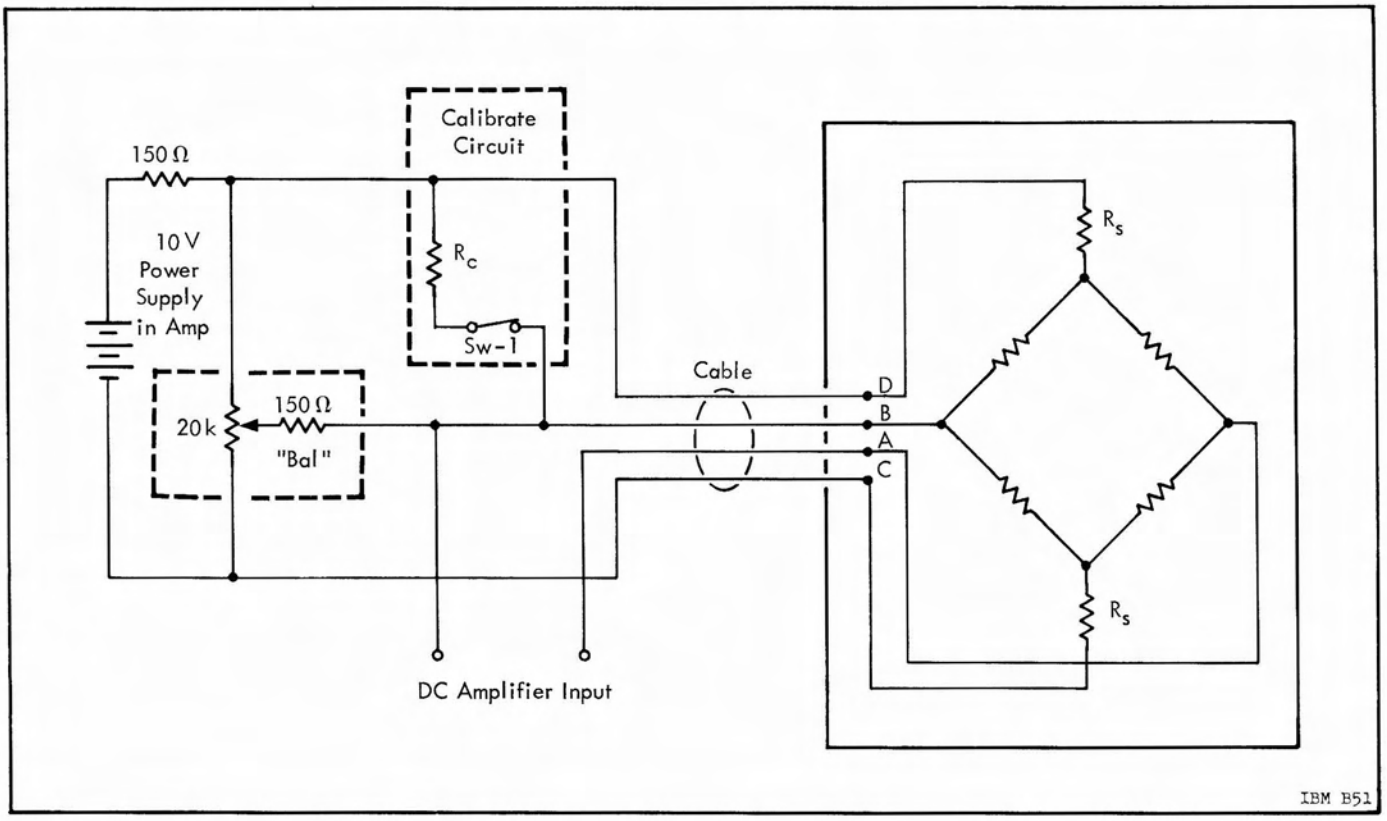


Figure 5.2-5 Strain-gage Type Pressure Transducer

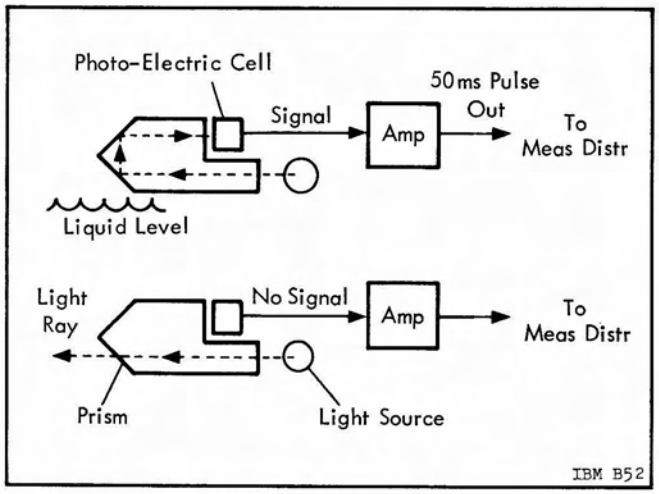


Figure 5.2-6 Liquid Level, Discrete, Functional Diagram

The continuous method of measuring liquid level is used in the lower portion of the propellant tank to determine the amount of propellants remaining after engine cutoff. Principles of operation of the continuous method are illustrated in Figure 5.2-7. The sensor consists of two tandem capacitors with the dielectric being the propellant. The top capacitor (C_S) is approximately 40 inches in length and exhibits a capacitance proportional to the height of the liquid and the dielectric constant of the liquid. The bottom capacitor (C_r) is approximately 3 inches in length and is submerged in propellant when a measurement is made. The capacitance of C_r is proportional to the dielectric constant of the liquid.

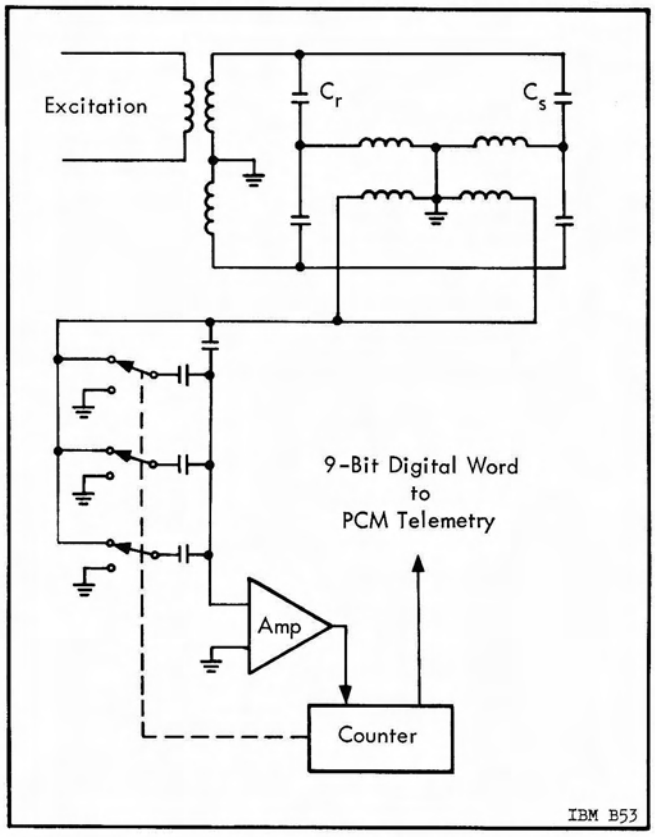


Figure 5.2-7 Liquid Level Sensor Electrical Schematic

Each capacitor is connected in a bridge circuit. The outputs of the two bridge circuits are connected as the excitation to a third bridge circuit which is always kept in balance by an electronic servosystem. The feedback elements of the servosystem are nine binary weighted capacitors controlled by a counter. The counter provides a parallel binary output for telemetry.

FLOW RATE MEASUREMENTS

Flowmeters are used to determine the rate of propellant flow to an engine. Basic principles of operation of the flowmeter are illustrated in Figure 5.2-8. The flowmeter is inserted directly in the liquid line and determines the volumetric fluid flow. Turbine blades are mounted on a hub which is imbedded with two permanent magnets. The blades are set so that the force of liquid flow causes the blades and the hub containing the magnets to rotate. On the periphery of the device is an E-core pickup with a number of wire turns. As the permanent magnets rotate, a sinusoidal voltage is generated in the core and its frequency is directly proportional to the flow rate.

TEMPERATURE AND RADIATION MEASUREMENTS

The principal temperature and radiation measurements are in the following areas:

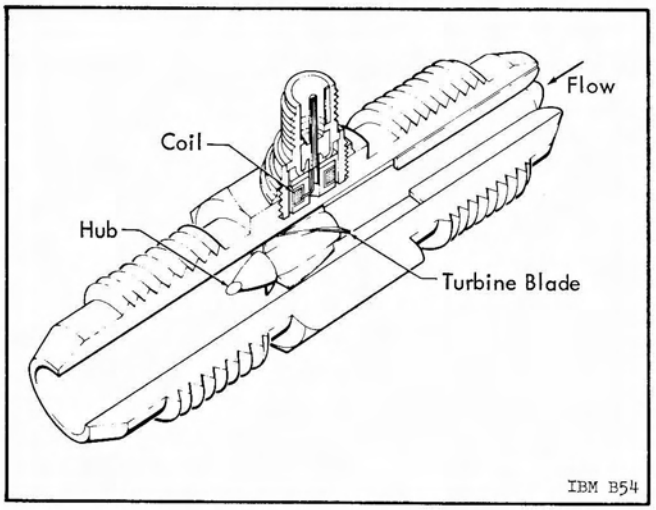


Figure 5.2-8 Basic Principles of a Flowmeter

- Cryogenic temperature measurements
- Heat flux (radiation and convective)
- Temperature measurements
- Fire detection temperature measurements
- General environmental temperature measurements

Cryogenic Measurements. An important factor in engine operating efficiency is the density of the oxidizer and the fuel. Temperature measurements are performed at critical points in these systems during flight. The operating efficiency of the engines can be determined from these and other measurements.

Cryogenic measurements are performed by means of resistance thermometers located in the fuel and lox tanks and in the plumbing for both of these systems. These positive temperature-coefficient resistors are fabricated of high purity platinum and require precise calibration techniques.

The maximum temperature range of these devices is from -200°C to +300°C (-328°F to +572°F). Data reduction is accomplished through a straightforward temperature versus resistance method. As in the other temperature measurements, dc amplifiers are employed to increase the output signal level to the required 0 to 5-volt telemetry input level.

Heat Flux (Thermal Radiation) Measurements. Calorimeters are located at strategic points on the engine heat shield to measure thermal radiation and thus permit a precise calculation of the minimum insulation weight allowable at these points.

One type of calorimeter measures both thermal radiation and convective heat transfer. The heating rate is determined from the temperature versus time characteristics of the copper slug.

Another type of calorimeter utilized in some measurements on the Saturn Vehicle is the "thin film" or "membrane" calorimeter. This calorimeter employs a thin disc of constantan welded to a copper heat sink. An insulated copper lead is attached to the center of the disc and another insulated copper lead is attached to the copper heat sink. The temperature differential between the center of the disc and the circumference of the disc produces the emf output which is telemetered to the ground. The emf output of the membrane calorimeter is a linear function of the incident heating rate with the slope of the output curve being determined by the physical size of the constantan disc.

Fire Detection Measurements (S-IB and S-IC Stages Only). The prelaunch fire detection system is operative during the period prior to vehicle lift-off. When the air temperature, measured at critical points, rises at a rate beyond a specified value, an alarm signal is initiated in the blockhouse and an automatic engine cutoff occurs.

A series of thermocouples, arranged in loops with several thermocouples in each loop, are used. The thermocouples are located in back of the heat shield and in the engine compartment. The rate of rise of the temperature of the air is measured in the immediate vicinity of the thermocouple, rather than the radiated heat from some point remote from the measuring device. The system does not define the exact location because of the series loop configuration.

General Temperature Measurements. Surface temperature measurements are made with thermocouples, thermistors, and resistance thermometers. Thermocouples are normally used when the measuring range is 150°C (302°F) or greater, and resistance thermometers and thermistors are used for ranges of less than 150°C. The resistance thermometers are extremely accurate positive temperature coefficient resistors of which the resistance thermometer type is typical. Thermistors are semiconducting devices which exhibit a high-negative-temperature coefficient of resistivity. Ambient air measurements down to 10°C (50°F) are also performed with thermistors.

Thermocouples and Zone Boxes. Three types of thermocouples are used on the vehicles. In the circuit consisting of 2 metals, an emf will be produced at the measuring junction if a temperature difference exists between the measuring and the reference junctions. The 3 types in use are: chromel/alumel, iron/constantan, and platinum/platinum 10 percent rhodium.

Thermocouples provide measurements of surface heat, fuel temperature, ambient air temperatures, and are used as fire detection gages.

In a laboratory, the reference junction is usually maintained at 0°C (32°F). For vehicular purposes, such a temperature limitation is impractical; therefore, an alternate method has been selected. Changes in reference junction temperature during flight are compensated for electrically by means of a bridge circuit with a resistance thermometer in one leg. A typical

bridge circuit with zone box is shown in Figure 5.2-9. The reference junction is contained within the zone box. The zone box is the junction between the vehicle network wiring and the thermocouple leads. A resistance thermometer is in thermal contact with the reference junction. The resistance thermometer has a known positive temperature coefficient. Since the resistance thermometer controls the resistance of one leg of the bridge, the output emf of the bridge circuit will follow the temperature induced emf output of the thermocouple (reference junction). The bridge circuit is so calibrated that it will cancel any emf produced by the reference junction as a result of an increase or decrease in temperature. The dc amplifier increases the output signal level to the required telemetry input level of 0 to 5 volts.

VIBRATION MEASUREMENTS

Vibration measurements are made to determine the structural strength and stability of the Saturn Vehicle. Vibration and stress sensors are mounted on the propellant tanks, turbopumps, engine mountings and engine combustion chamber, and at structural junction points of the vehicle. Two types of accelerometers are used as vibration sensors on board the vehicles; the piezoelectric and the strain gage types.

Piezoelectric Accelerometer. Because of its small size, light weight, and frequency response, the piezoelectric accelerometer is extensively used for flight vibration instrumentation. The frequency response of a typical piezoelectric accelerometer ranges from about 5 hertz to several kilohertz. For flight measurements, the useful frequency response is limited to the bandwidth of the telemetering channel. This type of accelerometer will not respond to static acceleration. The effects of vehicular acceleration are thus eliminated from the onboard measurements, and only local vibration is detected by the sensor.

The piezoelectric accelerometer (Figure 5.2-10 consists of a seismic mass which applies a force to a piezoelectric crystal, causing it to generate an electrical signal. The electrical output is proportional to the force applied to the crystal and is a true indication of dynamic acceleration or vibration. The high-impedance output of the device is coupled to a high-input-impedance emitter-follower stage to maintain adequate low-frequency response.

The emitter-follower can be integral to the accelerometer case, or it can be physically removed but joined electrically through a coaxial cable. Typical sensitivity is in the order of 10 mv/g. Temperature environment is the determining factor in the choice of crystal material to be used. A sufficiently

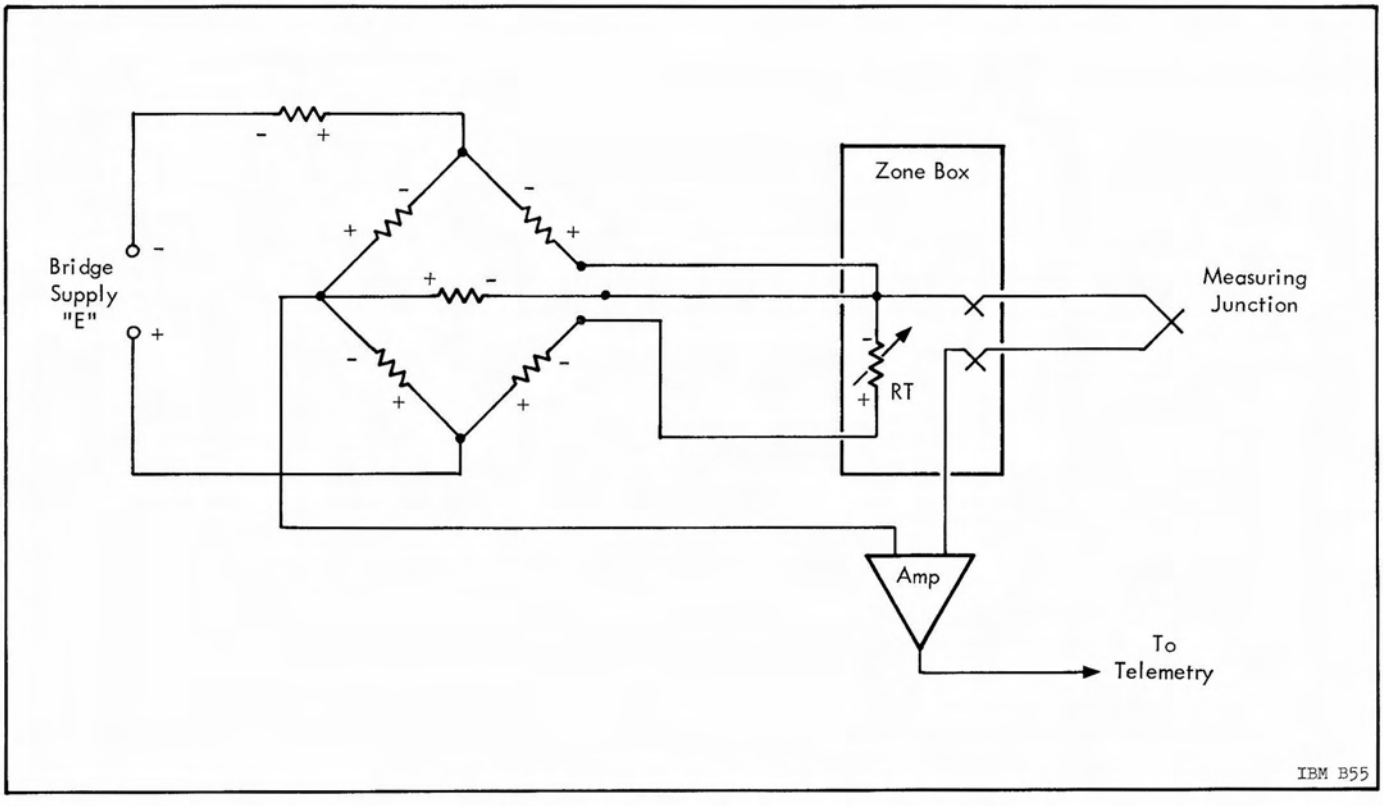


Figure 5.2-9 Typical Bridge Circuit

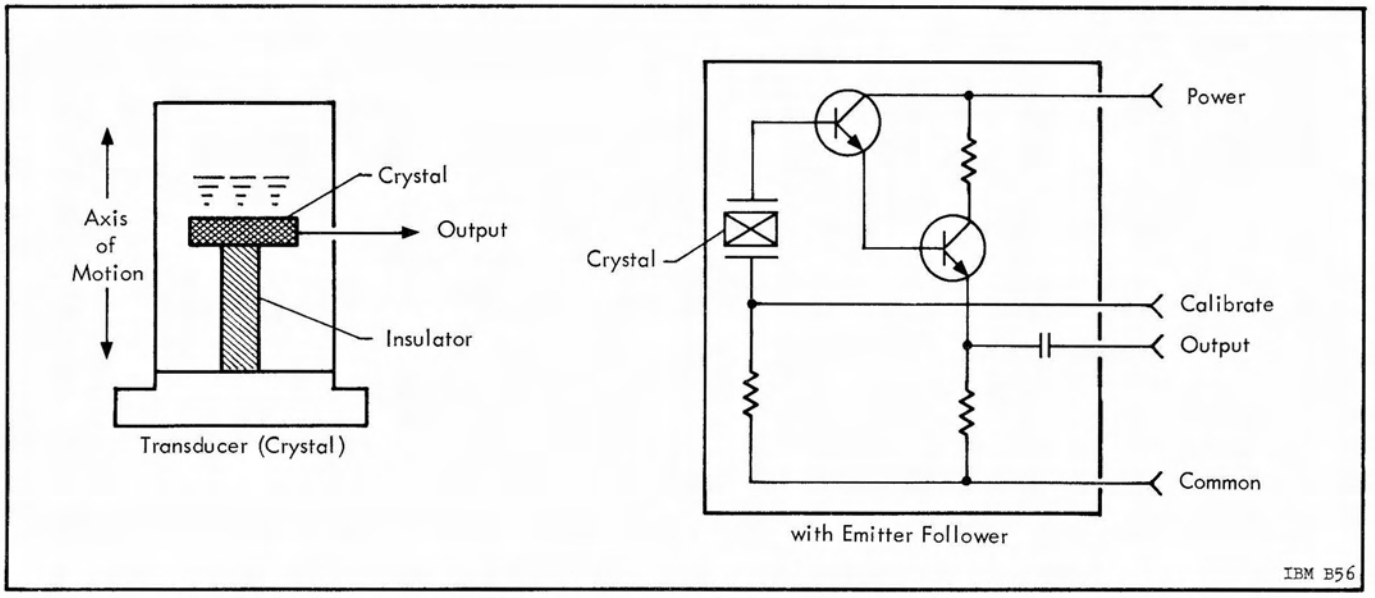


Figure 5.2-10 Piezoelectric Accelerometer and Emitter Follower

broad range of sensor types is available to permit vibration measurements to be made in almost any temperature environment. The accelerometers are capable of operating up to an acceleration level of several hundred g's and to a lower limit determined by the associated electronic circuits. In flight applications, the range is normally from ±3g to ±70g. Tests have indicated that the acoustic environment encountered on the vehicle will have negligible effect on accelerometer output. This is the sensor most frequently used for vibration measurements.

Strain Gage Accelerometer. The accelerometer (Figure 5.2-11) consists of a mass suspended from strain-sensitive wires connected to a Wheatstone bridge. When a force is applied to the mass, the resistances of the supporting wires change, thus unbalancing the bridge and causing an output voltage.

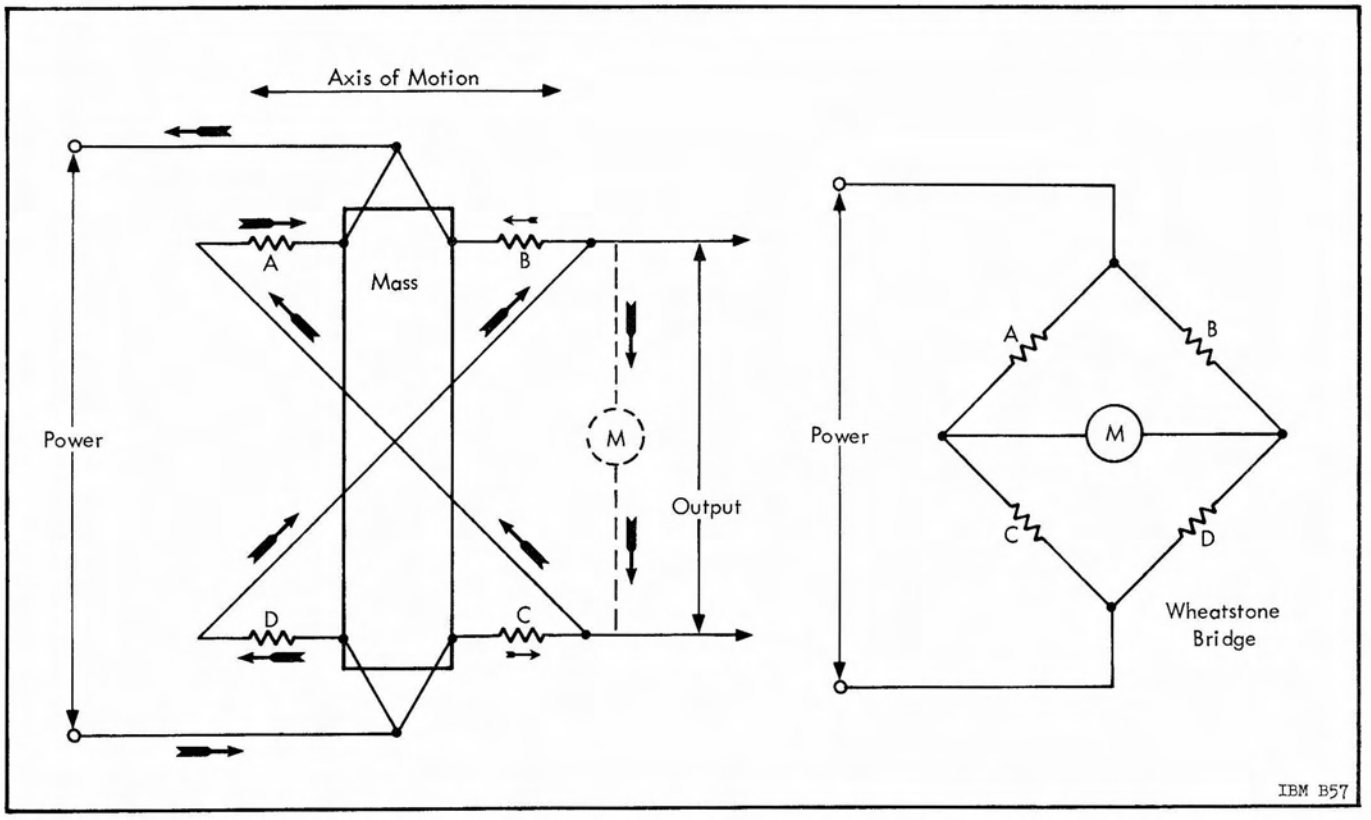


Figure 5.2-11 Strain-gage Accelerometer Block Diagram

The heavy arrows show the lower resistance circuit of an unbalanced bridge. The extent of the unbalance is indicated by the increase in voltage at the meter. In practice, a bias voltage is used to produce a 2.5-volt potential at the output of the amplifier when the mass is at rest. The bias prevents the output from going negative as the movements of the mass is in both directions. Furthermore, the bias confines the output voltage to the 0 to 15-volt range.

ACOUSTIC MEASUREMENTS

Microphone. A piezoelectric type microphone is used for flight acoustic measurements. One of the advantages of this microphone is that no shock mount is required. The microphone has a useful range of from 110 db to 190 db.

5.2.3 SIGNAL CONDITIONING

The following discussion on signal conditioning applies primarily to the Instrument Unit.

The signal conditioning system takes the signal to be measured and converts it to an analog signal that is acceptable to telemetry. The signal may be an electrical signal from the vehicle or it may be the output from a transducer. Certain transducers have output signals which do not require signal conditioning. These signals are fed directly to the Measuring Distributor.

A modular concept is used in the IU signal conditioning system. This consists of a number of measuring racks, each having 20 measuring channels plus 2 calibration channels. The modules which plug into the Measuring Rack consist of dc amplifiers, ac amplifiers, channel selectors (for calibration) and special modules. The amplifiers have the provisions for plug-in signal conditioning cards to obtain a very flexible measuring system with a minimum number of components.

The rack is a fabricated sheet metal structure with a tight fitting cover. It is not pressurized or hermetically sealed but has a gasket seal on the cover to protect the modules from foreign material. The internal electrical connections are made through a multilayer printed circuit board with flexible integral cable to the external connectors. The multilayer board is also the mechanical support for the measuring module connectors. A typical measuring rack of the type used in the IU is shown in Figure 5.2-12.

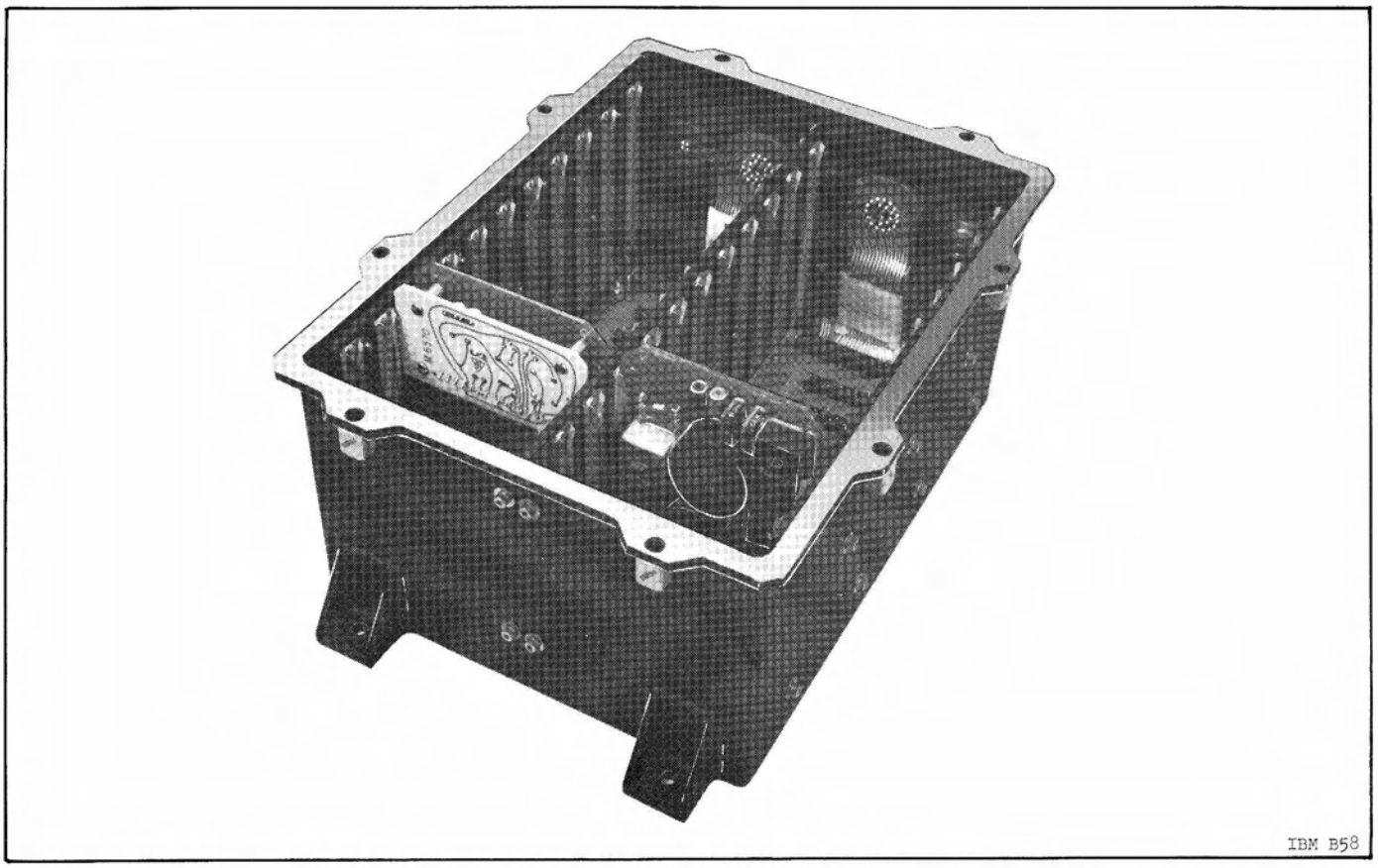


Figure 5.2-12 Typical Measuring Rack

DC AMPLIFIERS

There is only one type of dc amplifier used on the IU. By making use of a properly designed signal conditioning card, this one amplifier is used for measuring temperatures, pressures, currents, voltages, error signals, and other measurements.

The amplifier is a high-gain chopper amplifier with its input and output isolated from each other and ground. The amplifier has a fixed gain of 100. Variation in gain is controlled on the signal conditioning card. It contains a dual frequency response amplifier ranging from 0 to 20 hertz or 0 to 1000 hertz. The frequency response is determined by connecting jumper wires on terminals. The amplifier has an internal dc-to-dc converter and operates directly from the vehicle 28-volt supply.

The dc amplifier module contains a highly stable, isolated, and regulated power supply. This supply is used as a power source for strain gage transducers and temperature measurements and for a calibration voltage source in other measurements.

A limiting circuit is included in the amplifier to prevent overdriving the subcarrier oscillator of the telemetry system.

Two relays are provided for checkout and calibration of the amplifier and associated measuring system. These relays are operated remotely through the remote automatic checkout system.

AC AMPLIFIERS

Only one type of ac amplifier is used in the IU. The ac amplifier has the same type of signal conditioning card as the dc amplifier. It is used primarily for vibration and acoustic measurements.

The amplifier has a gain of 240 and a frequency response of 40 to 3000 hertz. Since practically all vibration and acoustic measurements are on SS/FM telemetry, the lower frequency response limit was designed to be 40 hertz. The output is transformer isolated from the input and ground.

The amplifier contains an internal dc-to-dc converter to supply an isolated power source for the amplifier and to provide an isolated power source for use with the vibration transducers and emitter followers.

The ac amplifier has the same type limiting circuits and calibration relays as the dc amplifier. Figure 5.2-13 illustrates an ac amplifier used in the IU.

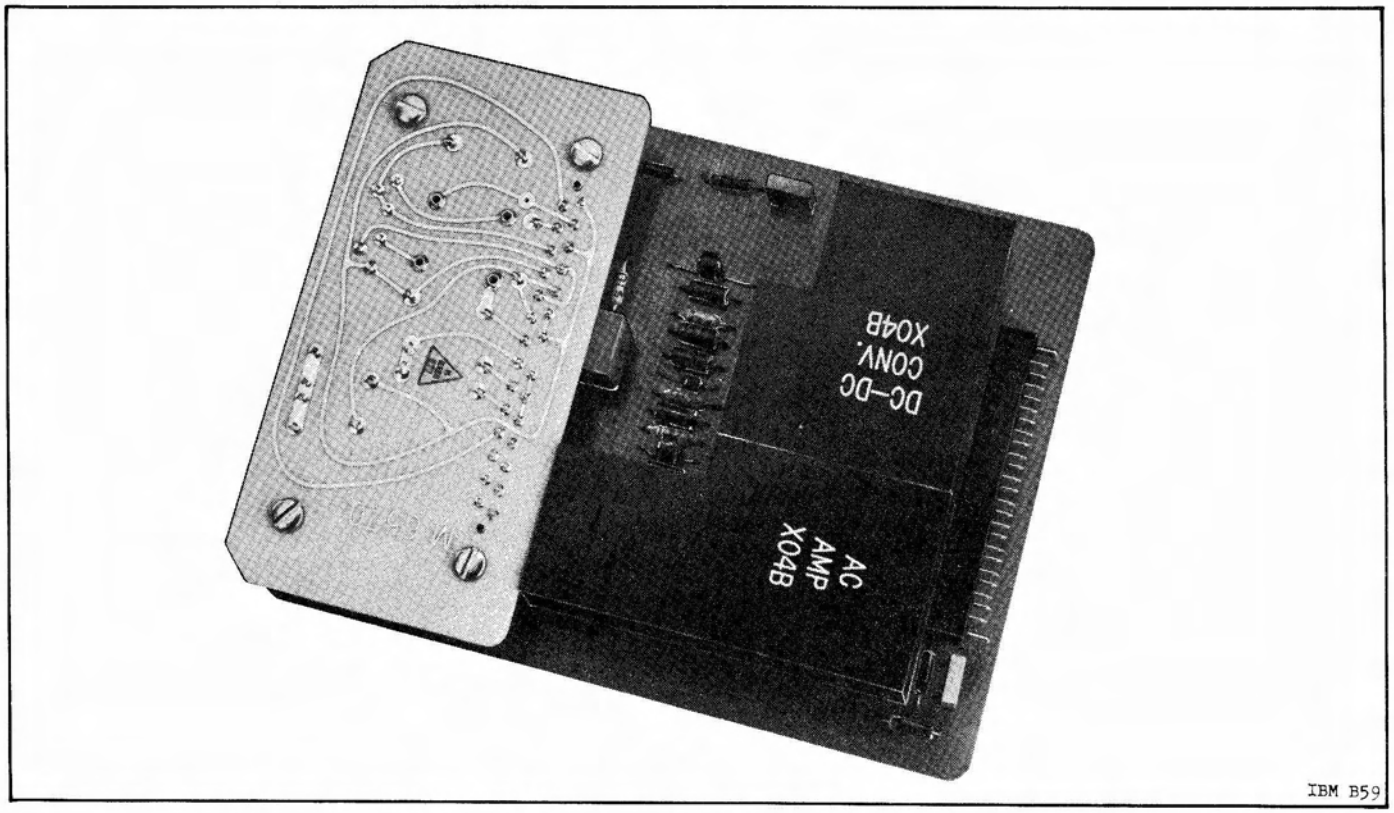


Figure 5.2-13 Illustration of an AC Amplifier

SPECIAL MODULES

There are several measurements that require signal conditioning that are not compatible with the ac or dc amplifier. Special signal conditioning modules are used for these measurements. Examples of these modules are: the dc converter used with flowmeters, the servo accelerometer unit used with the force balance accelerometers, and the frequency measuring unit used to accurately monitor the 400-hertz vehicle supply. Most of the special modules have relays for calibration and checkout.

SIGNAL CONDITIONING CARD

The signal conditioning card is a printed circuit card with a connector that mates with the signal conditioning card on the dc and ac amplifiers. The card provides the necessary flexibility to obtain the measurements required on the Saturn Vehicle with a small number of different type amplifiers. Thus, only one type of dc amplifier and one type of ac amplifier are used on practically all the measurements requiring signal conditioning. The signal conditioning card contains bridge completion resistors, calibration resistors, bias networks gain adjustment, etc.

A circuit diagram of a typical card for temperature measurements is shown in Figure 5.2-14. In this case, the transducer is a thermistor. Small range changes can be made by the span adjustment potentiometer. By changing resistors, the range can be changed by a large amount and several ranges of temperature can be measured by using one signal conditioning card. The system can be calibrated by using the remote automatic checkout system to operate the relays and thus shunt resistors R7 or R8 across the bridge.

Similar cards are used for error signals, currents, strain gage bridge transducers, and other measurements.

Signal conditioning in other vehicle stages accomplished in a similar way. Signal conditioning modules are mounted in measuring racks containing 20 modules each. In the S-IVB Stage, signal conditioning modules are mounted on panels distributed throughout the stage. The number of measuring racks in each stage is given in Table 5.2-1.

5.2.4 MEASURING DISTRIBUTOR

The measuring distributors accept the 0 to 5-volt output of the signal conditioning modules and route them to the proper telemetry channel. All measurements in the measuring system are connected to the distributor and are directed to their preassigned channel. The distributors provide versatility in changing channel assignments; changes are made by physically rearranging jumper wires within the measuring distributors. The versatility of the distributors eliminates extensive cable changes and allows channel changes to be made just prior to launch. More than one measuring distributor may be used depending on the number of measurements to be made and the physical location within the IU of the measurements to be made.

Switching functions connect different sets of measurements to the same telemetry channels during different flight periods. These switching functions, controlled by the Control Distributor, are performed in the Measuring Distributor. Switching functions, controlled from the ground via the umbilical cable, connect measurements not required during flight to digital data acquisition system channels for ground checkout and return the channels to flight measurements after checkout.

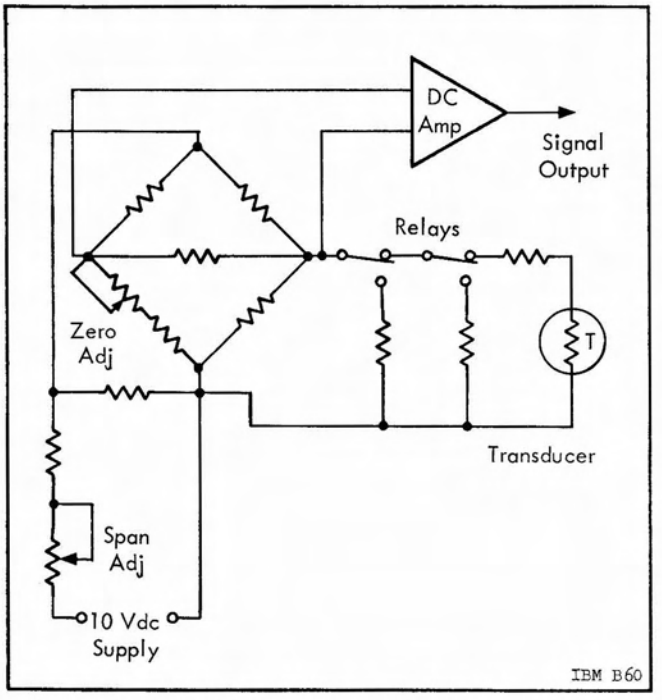


Figure 5.2-14 Typical Signal Conditioning Card for Temperature Measurements

SECTION 5.3

REMOTE AUTOMATIC CALIBRATION SYSTEM

The remote automatic calibration system permits a remote calibration of the measuring system prior to launch. During vehicle checkout, calibration of measurements is accomplished through the RACS and various corrections can be made by adjusting potentiometers on the modules. Prior to launch time, the RACS may be operated if the system drifts or deviates from the final adjustments. The data obtained is used to correct the flight data for more accurate measurements.

Each signal conditioning module contains 2 relays and the necessary circuit to simulate the transducer as well as the upper (HI) end and the lower (LO) end of the signal range for that particular measurement. The transducer is connected to the module in the RUN mode.

A binary-coded signal is sent from the GSE through the umbilical cable to the Measuring Rack Selector in the vehicle to select a particular measurement for calibration. Figure 5.3-1 shows the RACS of the IU. Each stage has a separate RACS. The signals are generated in the GSE either by a manual keyboard or from a computer program. These signals are decoded on the vehicle and distributed to the various Measuring Racks to operate the checkout relays.

The calibration signal consists of 13 bits in parallel. There are 6 bits for rack selection, 5 bits for channel selection, and 2 bits for mode selection. (One checkout relay is for the HI mode, or checkpoint, and the other is for the LO mode, or checkpoint.) The same code is used on all stages to provide a 31-rack capacity. The IU RACS is designed for 14 racks.

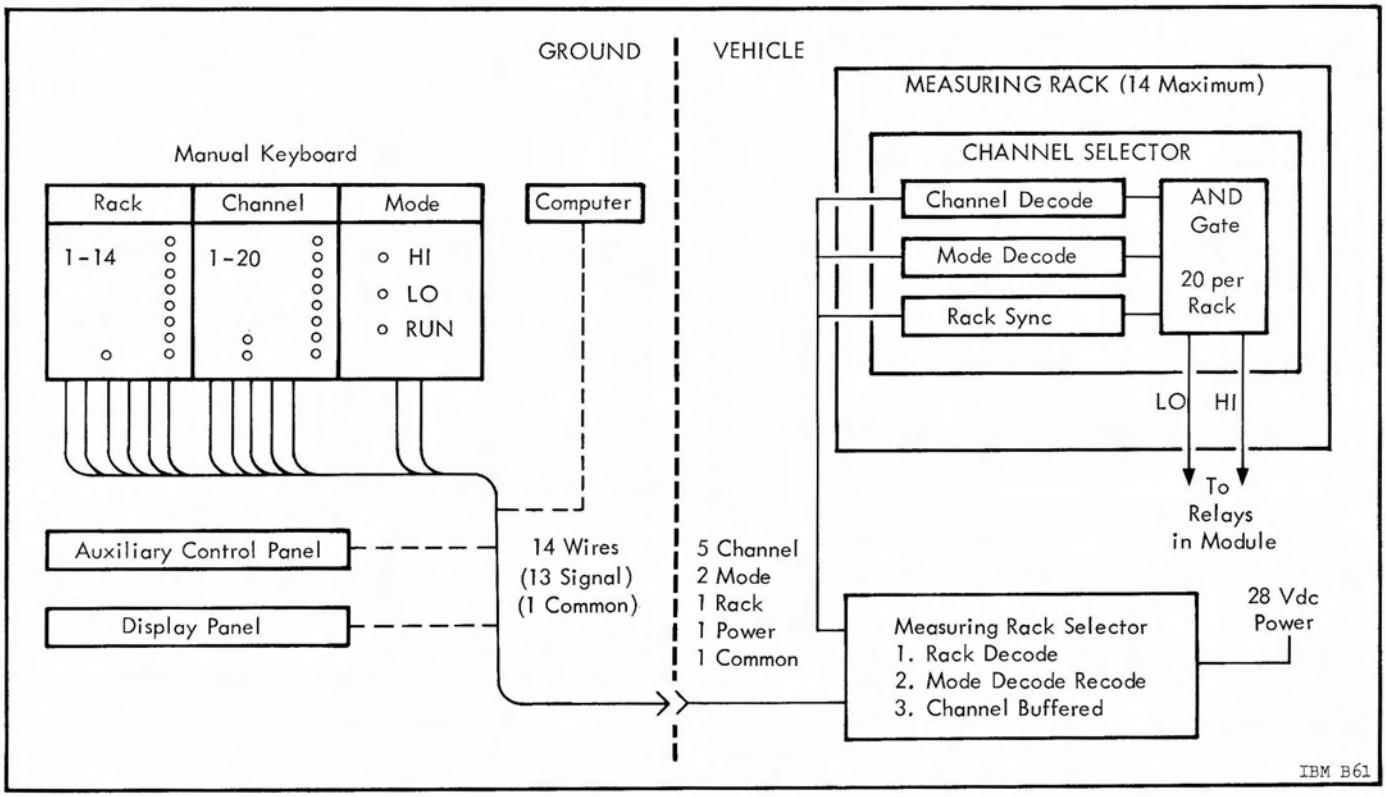


Figure 5.3-1 Block Diagram of RACS for the IU

On the vehicle, the code is received in the Measuring Rack Selector. The rack select code is decoded and the signal is addressed to the proper Measuring Rack. Buffer circuits for mode codes and channel codes are provided in the Measuring Rack Selector which acts as a distribution point to the various Measuring Racks. The signals go to the channel selector module in the selected Measuring Rack. Operation of the channel selector requires the following conditions:

Rack select signal present
Channel select signal present
Mode signal present (HI or LO)

There are two channel selectors in each Measuring Rack. One decodes channels 1 through 10 and the other decodes channels 11 through 20. The channel selector contains the necessary diode matrices and latch circuits to complete the operation of the RACS.

The channel select modules contain 20 AND gates. When the 3 conditions mentioned above are fulfilled, the addressed AND gate "latches in" and energizes the corresponding calibration relay in the signal conditioning module. This relay will remain energized until another signal is sent to change the mode.

In addition to HI and LO mode, there is a third mode of operation, called RUN mode, which is selected when both calibration relays are in an unenergized state. The RUN mode is the normal mode of operation with the transducer or input signal connected to the signal conditioning module. During calibration (following HI or LO mode), the RUN mode is achieved by sending the proper code to the vehicle. Since the RACS is used only before launch, it is wired in such a way that the power is removed at launch. Removal of the power causes all relays to switch to RUN mode. This eliminates the possibility of leaving any module in the checkout state (HI or LO).

Any number of channels can be selected individually, simultaneously, or in any sequence or combination (with any combination of a HI, LO, or RUN selection at the GSE keyboard). The GSE display panels are used to monitor the signal (code) sent to the vehicle (there is no code feedback from the vehicle). The calibration results are observed through the telemetry system and connected ground-checkout system.

Each of the signal conditioning modules has push buttons on the front of the module for manual operation of the calibration inside the vehicle.

SECTION 5.4

TELEMETRY

5.4.1 SATURN TELEMETRY SYSTEM

Each stage of the Saturn Vehicle carries an independent telemetry system. These systems modulate the signals from the measuring system onto RF carriers for transmission to ground stations. Three different modulation techniques are applied in the telemetry system of each stage:

- FM/FM telemetry applies frequency modulation/frequency modulation with Pulse Amplitude Modulation (PAM) and triple Frequency Modulation (FM^3) as auxiliary techniques
- SS/FM telemetry uses single sideband modulation/frequency modulation
- PCM/FM telemetry uses pulse code modulation

These different modulation techniques provide efficient transmission of the large number and variety of measuring data which has different requirements of bandwidth and accuracy (Table 5.4-1).

Low-response/low and medium-accuracy data may be sufficiently defined by sampling at a rate of 10 hertz, or less. In terms of frequency response this would be 2 or 3-hertz maximum variation. This category includes temperature, pressure, and other measurements where dynamic variations are not very likely or are not of particular interest.

Low-response/high-accuracy data requires accuracies of 1 percent or better. Examples are longitudinal acceleration and combustion chamber pressure measurements.

Medium-response/medium-accuracy data requires a 5 to 40-hertz response. Data of this category can be handled by sampling at 100 to 125 hertz per channel or less, or by FM/FM channels below the 3-kilohertz subcarrier using the standard deviation ratio of 5.

High-response/medium-accuracy data requires a 50 to 1000-hertz channel response. This type of data is readily handled by FM/FM subcarriers.

Wide-band data has a bandwidth of roughly 50 to 3000 hertz and normally no dc component of interest.

Table 5.4-1 Data Categories

Type	Frequency Response (hertz)	Accuracy Required (percent)
1. Low-response/low and medium-accuracy	2-3	2-5
2. Low-response/high-accuracy	2-3	1
3. Medium-response/medium-accuracy	5-40	2
4. High-response/medium-accuracy	50-1000	2
5. Wideband low-accuracy	50-3000	5
6. Event measurements	---	---
7. Digital measurements	---	---

Vibration data and sound intensity fall within this classification.

Event measurements constitute a special category. Interest in this data is limited to whether or not an event has occured and, if so, the time of occurrence with respect to a specified time resolution.

In addition, much data originates in digital form, e.g., signals from the LVDC.

The wide-band data-carrying capability of standard FM/FM telemetry is very poor. The FM/FM system has one channel with a frequency response of 0 to 1050 hertz at a subcarrier deviation ratio of 5; the other channels have decreasing frequency responses down to 6 hertz. The sum of all the channel bandwidths is only 4700 hertz. The bandwidth efficiency of a standard FM/FM system with subcarriers operating at a deviation ratio of 5 is about 1.6 percent. A corresponding figure for a PAM/FM system is about 3.5 percent; for a PCM/FM system, it is about 3.0 percent.

The necessity to transmit wide-band data (acoustic and vibration measurements) led to the use of SS/FM telemetry. An RF carrier is frequency modulated with single-sideband, amplitude-modulated carriers. The bandwidth efficiency of such a system is roughly 10 times greater than that of FM/FM. It is capable of transmitting 45 hertz of data over the same bandwidth used by the FM/FM link to transmit 4700 hertz of data.

A theoretical comparison of the signal/noise performance of the SS/FM with a standard FM/FM system is useful. Since single-sideband subcarriers do not possess wide-band gain, one would logically expect that SS/FM would perform less favorably in this respect than FM/FM, probably by a factor equal to $\sqrt{3}$ times the deviation ratio, which is the wide-band gain of the FM subcarrier. However, if the modulating signal of such a system is to be vibration data, other factors can more than compensate for the lack of wide-band gain in the subcarrier.

These compensating factors result from a prior knowledge of the nature and characteristics of vibration data. A Gaussian or normal curve is a good approximation of amplitude distribution characteristics of such data. Since the summation of Gaussian functions is a Gaussian function itself, the composite signal modulating the transmitter (in an SS/FM system carrying vibration data) could be expected to resemble a Gaussian function. The peak-to-peak amplitude of the data applied to an FM subcarrier must be limited to the band edges of the subcarrier channels, the deviation being ± 7.5 percent of center frequency, to prevent adjacent channel interference. Thus, when data possesses a high peak-to-rms ratio, the signal capacity of the channel is reduced below its signal capacity for a sine wave modulating signal (1.41 peak-to-rms ratio). Correspondingly, Gaussian data with a peak-to-rms ratio of 4.0 reduces rms data capability to 2.83.

No such inherent peak data restriction exists in the SS/FM system. The data peaks of the individual channels add in a random manner, resulting in an amplitude distribution of the composite signal similar to that of the data at the channel inputs and having a peak factor of approximately the same magnitude. Thus, with Gaussian-type characteristics and an identical number of channels, the SS/FM system will accommodate two or more times as much peak carrier deviation per channel as an FM/FM system.

Data which originates in digital form and data requiring high accuracy are transmitted through the PCM/FM system. The digital data transmission link is relatively insensitive to imperfections in the transmission channel. Below a threshold noise level, the accuracy is not appreciably affected by noise in the channel. Nonlinearity in the transmission channel is of little consequence. By a relatively simple and reliable operation, the serial digital data which contains noise and deteriorated rise time can be regenerated into its original noise-free form.

Also, digital data transmission is compatible with real-time data processing by digital computers at ground stations. A separate digital data output of the PCM/FM system is used for automatic preflight checkout of the launch vehicle. This is called the digital data acquisition system. The Mod 301 PCM/DDAS Assembly is also connected with the LVDC for checkout of the S-IVB/IU Stage in orbit. During flight, all operational data is transmitted over the PCM/FM link.

To increase the data handling capacity of telemetry systems, several data channels are multiplexed. Two types of multiplexing are utilized: frequency-division multiplexing and time-division multiplexing.

Frequency-division multiplexing is the process of simultaneous frequency sharing of one RF carrier transmission link by dividing the available bandwidth into a number of channels, each with a separate center

frequency. Spacing is provided between these channels to allow each channel to be frequency modulated or deviated about the center frequency. After modulation occurs, the subcarrier signals are combined linearly, and the resultant composite signal is used to frequency modulate an RF carrier. FM/FM and SS/FM are examples of this frequency division multiplexing.

Time-division multiplexing is the process of sequential sampling of two or more data sources and applying the data samples to a common output in a fixed sequence. The samples may or may not be separated by a "dead time" space. Usually some "marker" is made a part of the output signal to desigate the beginning or end of a sampling cycle. This is for identification and synchronization purposes at the data reduction point.

The Saturn telemetry systems make use of several types of time-division multiplexers. The Mod 270 Multiplexer Assembly is a time-division multiplexer for analog data. It is used in conjunction with the FM/FM telemetry system and the PCM/FM system. The Mod 245 Multiplexer Assembly provides time-division multiplexing for wide-band data and is used for SS/FM telemetry and FM/FM telemetry. The remote digital submultiplexers and digital multiplexers are used in connection with the Mod 301 PCM/DDAS Assembly. Remote analog submultiplexers are used for analog data connected to the Mod 270 Multiplexer Assembly.

The number of RF carriers allotted to each modulation technique is chosen to provide an appropriate balance of data transmission capability to handle the quantities and varieties of data originating on the stage. The telemetry equipment associated with each stage consists of a "building-block" arrangement, which may be connected in numerous combinations to satisfy specific measuring requirements. The number of carriers allocated to FM/FM, SS/FM, or PCM/FM and also the specific combination of building blocks vary from stage to stage and from vehicle to vehicle.

TYPICAL S-IVB/IU TELEMETRY SYSTEM

A typical R & D version of the S-IVB/IU telemetry system is shown in Figure 5.4-1. Figure 5.4-2 illustrates the operational version. In operational vehicles, the number of multiplexers and FM/FM systems will be reduced, and the SS/FM telemetry will be omitted. Flight (mission) control data will be sent in parallel to the IU PCM/FM and S-IVB PCM/FM systems as indicated in the figure. Therefore, in the event of a failure in one of the PCM systems (IU or S-IVB), the other PCM systems can be used to transmit the flight control data.

Table 5.4-2 lists the type and number of telemetry systems and multiplexers used in the stages of Saturn Vehicles. Because of the smaller quantity of measurements required in operational vehicles, the number of telemetry systems is also reduced. (Figures given for operational vehicles are "best guess" at the present time.)

From one to six time-division multiplexers are synchronized from a central timing source located in the PCM/DDAS Assembly. Each time-division multiplexer provides an output to the PCM/DDAS Assembly which combines the outputs into a single serial wavetrain. The individual analog samples are digitized and combined into a digital format which is transmitted via coaxial cable to the ground checkout equipment. This data is also transmitted via a PCM/FM carrier for in-flight monitoring.

Each of the time-division multiplexers has a second data output which is identical to the output provided to the PCM/DDAS Assembly except that it is conditioned for PAM transmission. These outputs may modulate a 70-kilohertz, voltage-controlled oscillator in FM/FM telemeter assemblies. This arrangement provides redundant transmission of some multiplexer outputs using both PAM and PCM techniques.

5.4.2 FM/FM TELEMETRY SYSTEM

The FM/FM telemetry system frequency multiplexes the input data. The conditioned signals derived from pressure, temperature, etc., modulate the frequency of the subcarrier oscillators. The combined output of several subcarrier oscillators is again frequency modulated on the RF carrier. Standard IRIG frequency channels are assigned. The data bandwidth capabilities of these channels are shown in Table 5.4-3. Slow-varying data is applied to the low-frequency channels; data with higher frequency variations, must be applied to the higher frequency channels. FM/FM systems are susceptible to various sources of noise and distortion (fluctuation noise, crosstalk, harmonic distortion of the individual subcarrier signals, subcarrier data feed-through, and distortion of individual subcarrier signals due to band-limiting filters), which affect the accuracy of the telemetered data.

Table 5.4-2 Telemetry Systems in the Various Saturn Vehicle Stages

Stage	Telemetry System	Number of Systems R&D	Number of Systems Oper	Number of Multiplexers R & D	Number of Multiplexers Oper	Transmitter Frequency	Transmitter Power
IU	FM/FM SS/FM PCM/FM	2 1 1	1 - 1	1x CIU 2x Mod 270 1x Mod 245 1x RDM Mod 410 1x RDSM	1x CIU 2x Mod 270 2x RDM Mod 410	Saturn IB: 225-260 MHz Saturn V: 225-260 MHz and 2200-2300 MHz	20 W
S-IVB	FM/FM SS/FM PCM/FM	3 1 1	1 - 1	4x Mod 270 1x Mod 245	2x Mod 270	225-260 MHz	20 W
S-II	FM/FM SS/FM PCM/FM	3 2 1	2 - 1	5x Mod 270 1x Mod 245 7x RASM 2x RDSM	2x Mod 270 2x RDSM 2x RASM	225-260 MHz	20 W
S-IC	FM/FM SS/FM PCM/FM	3 2 1	1 - 1	4x Mod 270 2x Mod 245 1x RDSM	1x RDSM 2x Mod 270	225-260 MHz	20 W
S-IB	FM/FM SS/FM PCM/FM	2 1 1	1 - 1	3x Mod 270 1x Mod 245 2x RDSM	2x Mod 270 1x RDSM	225-260 MHz	20 W

Note: CIU = Computer Interface Unit
RDSM = Remote Digital Submultiplexer
RASM = Remote Analog Submultiplexer
RDM = Remote Digital Multiplexer (Mod 410)

Each of the subcarrier oscillators of an FM/FM system may be preceded by another subcarrier group. Each of these "sub-subcarriers" would, in this case, be modulated by the actual measurement values. This technique is called FM/FM/FM, or FM^3. The technique trades bandwidth for additional channels; therefore, the frequency response of the channels is much lower. Since another modulation stage is used, the technique is less accurate than FM/FM.

A time-multiplexed signal may be fed into a subcarrier oscillator of an FM/FM system to increase the channel capacity. Time multiplexing consists of sequentially sampling a number of data signals with an electronic or mechanical commutator. The commutator output appears as a train of pulses of varying amplitude. This technique is known as Pulse-Amplitude Modulation (PAM/FM/FM).

The basic modulation scheme and principal components used (subcarrier oscillators, mixer, power amplifier, and transmitter) are essentially the same for each stage of the FM/FM system. Figure 5.4-3 shows a typical Saturn stage FM/FM system. Each channel receives a signal from the Measuring Distributor. This input signal modulates a voltage-controlled subcarrier oscillator. The frequency-modulated signals from the various subcarrier oscillators are combined in the mixer amplifier. The composite signal is frequency modulated on a radio-frequency carrier in the VHF band (225 to 260 megahertz) for transmission to the ground stations. The transmitter provides a signal power level of approximately 20 watts.

The available standard IRIG channels may be utilized in different ways. The system shown in Figure 5.4-3 uses 13 continuous data channels (channels 2 through 14). The input signals from the Measuring

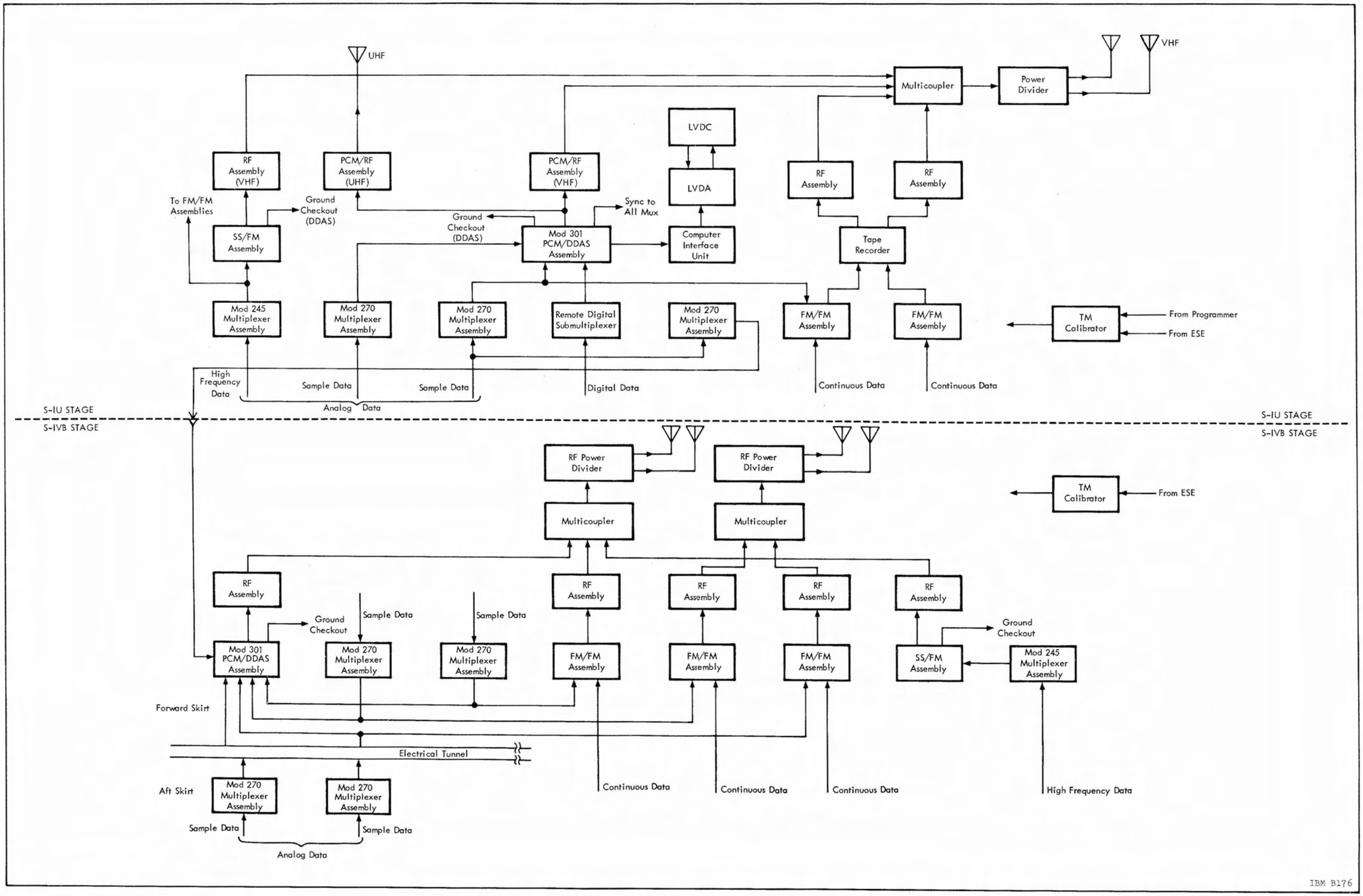


Figure 5.4-1 Typical S-IVB/IU Telemetry System (R & D Version)

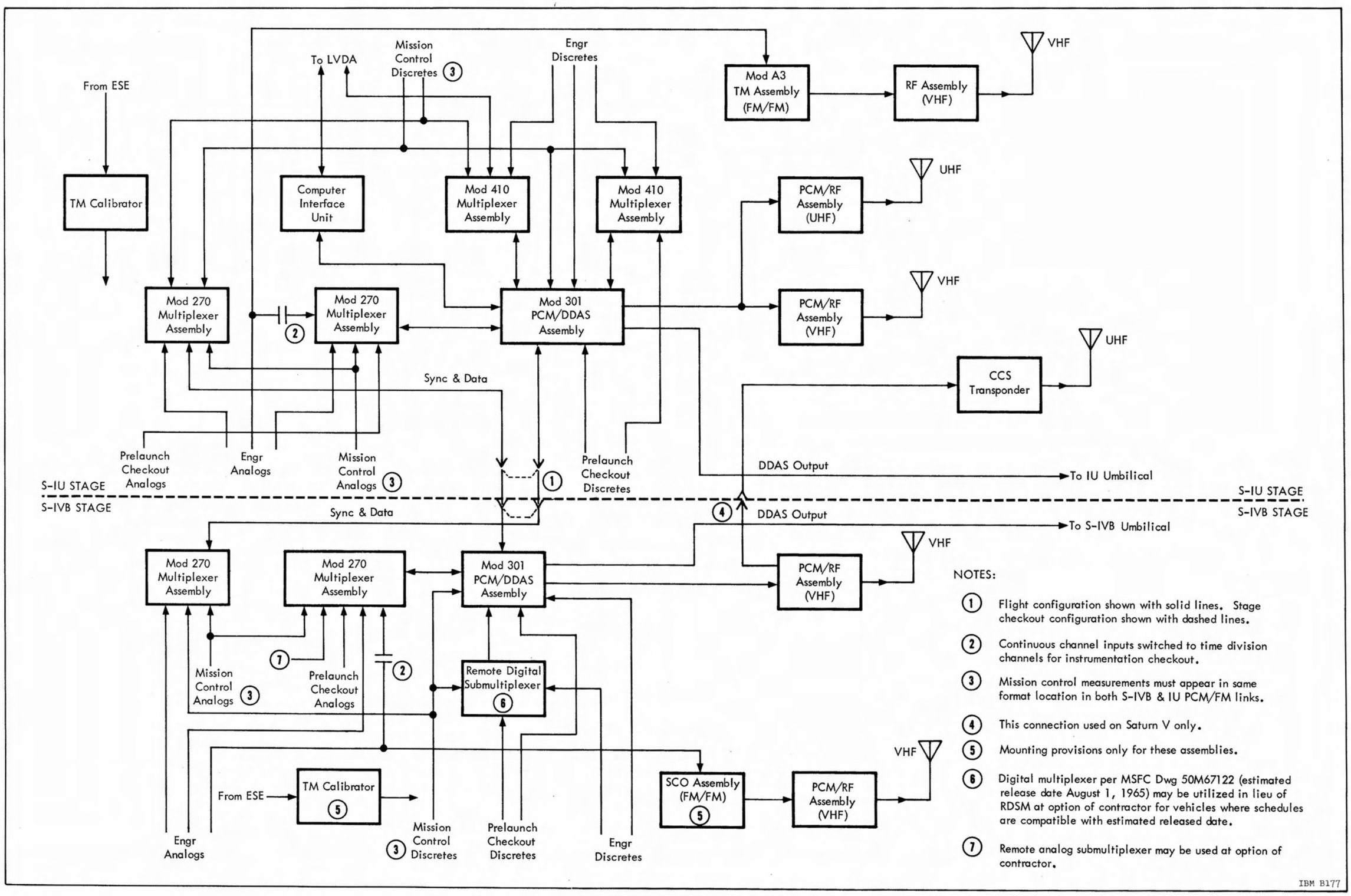


Figure 5.4-2 Typical S-IVB/IU Telemetry System (Operational Version)

Table 5.4-3 IRIG Subcarrier Channels (± 7.5% Channels)

Channel	Center Frequencies (kHz/s)	Lower Limit (kHz/s)	Upper Limit (kHz/s)	Nominal Frequency Response (Hz/s)	Nominal Rise Time (ms)	Maximum Frequency Response (Hz/s)	Minimum Rise Time (ms)
1	0.40	0.370	0.430	6	58	30	11.7
2	0.56	0.518	0.602	8	42	42	8.33
3	0.73	0.675	0.785	11	32	55	6.40
4	0.96	0.888	1.032	14	24	72	4.86
5	1.30	1.202	1.398	20	18	98	3.60
6	1.70	1.572	1.828	25	14	128	2.74
7	2.30	2.127	2.473	35	10	173	2.03
8	3.00	2.775	3.225	45	7.8	225	1.56
9	3.90	3.607	4.193	59	6.0	293	1.20
10	5.40	4.995	5.805	81	4.3	405	0.864
11	7.35	6.799	7.901	110	3.2	551	0.635
12	10.50	9.712	11.288	160	2.2	788	0.444
13	14.50	13.412	15.588	220	1.6	1,088	0.322
14	22.00	20.350	23.650	330	1.1	1,650	0.212
15	30.00	27.750	32.250	450	0.78	2,250	0.156
16	40.00	37.000	43.000	600	0.58	3,000	0.117
17	52.50	48.562	56.438	790	0.44	3,938	0.089
18	70.00	64.750	75.250	1,050	0.33	5,250	0.067
19	93.00	86.025	99.975	1,400	0.25	6,975	0.050

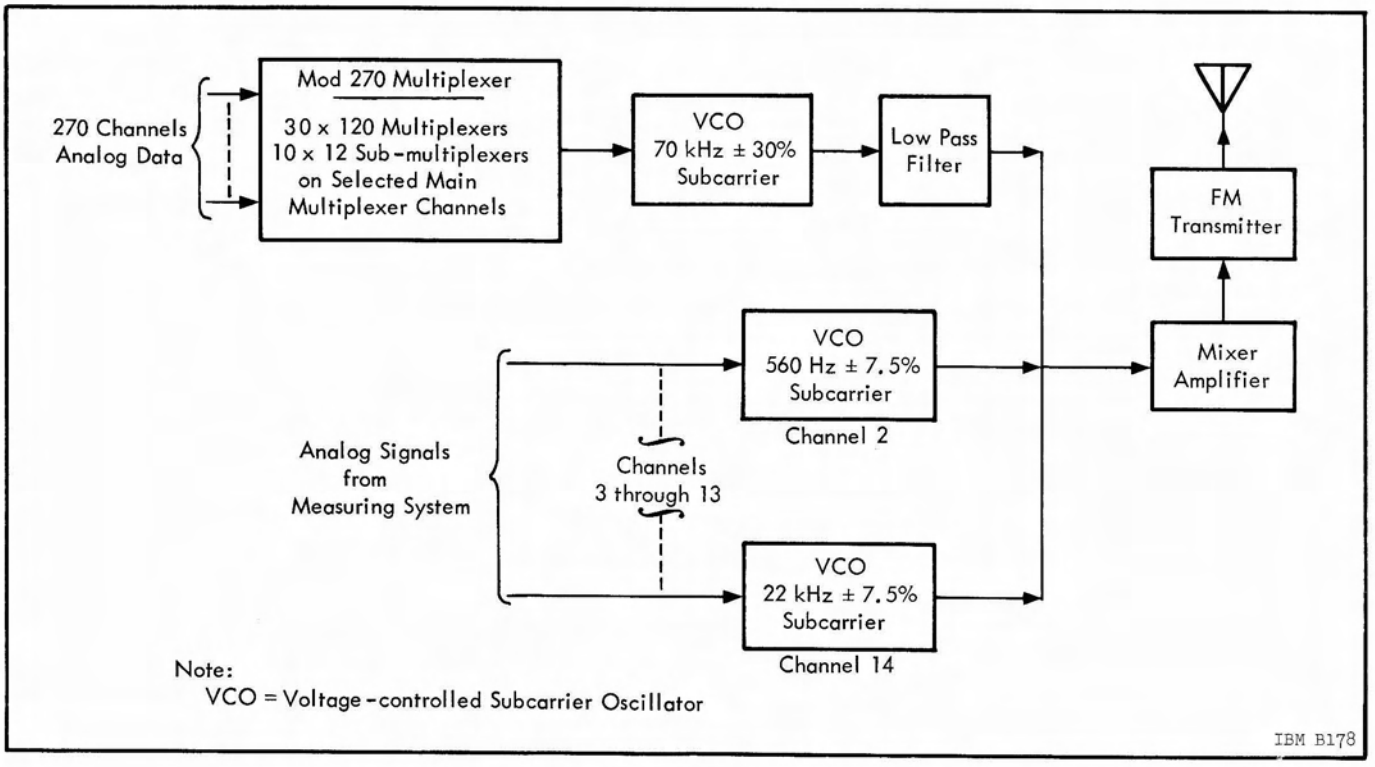


Figure 5.4-3 Block Diagram of Typical Saturn V FM/FM Telemetry System

Distributor are in the range of 0 to +5 volts dc (2 to 7 volts peak-to-peak ac when a bandpass filter is used in place of a channel or subchannel oscillator).

When used, triple FM (FM^3) is applied to the channels above channel 13. A subcarrier channel of 70 kilohertz (±30 percent) is used for time-multiplexed signals from the Mod 270 Multiplexer Assembly. When this PAM technique is applied, all IRIG channels above 30 kilohertz will not be used. The Mod 270 solid-state, time-division multiplexer operates at a rate of 3600 samples per second. It consists of 30 primary channels which are sampled 120 times per second. In addition, 10 submultiplexers may be used on selected main channels; each sampled at a rate of 12 per second. The multiplexer accepts input signals in the range of 0 to 5 volts dc and provides two PAM wave train outputs. One wave train modulates the 70-kilohertz, voltage-controlled subcarrier oscillator with a frequency deviation of ±30 percent (i. e., 49 to 91 kilohertz for an input signal from 0 to 5 volts dc). The second wave train is used for the PCM system.

The RF Assembly accepts single sideband FM and FM analog signals from the telemetry assemblies and provides the highly-stable, close-tolerance carrier frequency (±0. 01 percent). It further provides the capability of varying the carrier frequency in a manner (±1 percent of the best straight line approximation for 125-kilohertz deviation at modulation frequencies from 300 hertz to 100 kilohertz) proportional to the input signal amplitude, thereby providing an RF link from the measurement systems in the flight vehicle to the ground receiving station.

5.4.3 SS/FM TELEMETRY SYSTEM

The Saturn SS/FM telemetry system is designed specifically for transmission of the large volume of vibration data from the Saturn Vehicle. This system can transmit 15 channels, each having a response of 30 to 3000 hertz, for a total data bandwidth of approximately 45 kilohertz within the standard telemetry carrier bandwidth.

Each of the 15 data inputs is fed to a balanced modulator and heterodyned with a 455-kilohertz carrier (Figure 5. 4-4). The output of the modulator is fed to a mechanical bandpass filter (455 to 458 kilohertz) which passes only the upper sideband. The output of the filter is fed to a second balanced modulator where it is translated to the proper baseband frequency. The baseband position is determined by the carrier supplied from the frequency synthesizer. The two balanced modulators and the mechanical bandpass filter for each data channel make up the channel units. The channel units are identical for all channels.

The second modulator carriers are supplied to the channel unit from the frequency synthesizer and comb filters. These 15 subcarriers transpose the data to an assigned frequency between 4. 74 and 72 kilohertz. These are the lower sideband outputs of the second modulators.

Both sidebands of the second modulators go to the summing amplifier No. 1 and the 200-kilohertz low-pass filter where all upper sidebands of the second modulator are filtered out. Here a 75. 835-kilohertz pilot tone is summed into the channel unit outputs. The pilot tone provides a signal at the receiving station for demodulation of the 15 channels.

After leaving the 200-kilohertz low-pass filter, the composite signal is passed through a signal regulator. From the signal regulator, the composite signal is summed with the signal from the non-translated special service channel. The frequency response of this channel is 0 to 1200 hertz. Its normal use is to carry a 960-hertz signal provided by the Mod 245 Multiplexer Assembly for demultiplexing the signals at the receiver. The output of the summing amplifier No. 2 is used to frequency modulate an RF transmitter.

All the carrier signals and the pilot tone are generated internally in the airborne SS/FM assembly by a single 910. 025-kilohertz crystal oscillator. This signal is used to drive a flip flop which provides the 455. 012-kilohertz carrier signal and a frequency synthesizer provides all sub-carriers and the pilot tone from the comb filters.

To provide a 3-kilohertz information bandwidth and allow sufficient guardband, a channel spacing of 4. 74 kilohertz is used. This spacing is convenient to generate in the synthesizer and allows an adequate guardband of 1. 74 kilohertz. The 75. 83-kilohertz pilot tone falls just above the highest baseband frequency. It is used as a reference in the ground demodulation equipment to regenerate the basic 455 and 4. 74-kilohertz frequencies. Since the amplitude of the transmitted 75. 83-kilohertz pilot tone is regulated, it is also used as an automatic gain control.

The SS/FM Assembly is used in conjunction with a vibration multiplexer (Mod 245) to expand its data-handling capability by time-sharing specific data channels. SS/FM telemetry is not carried in operational vehicles.

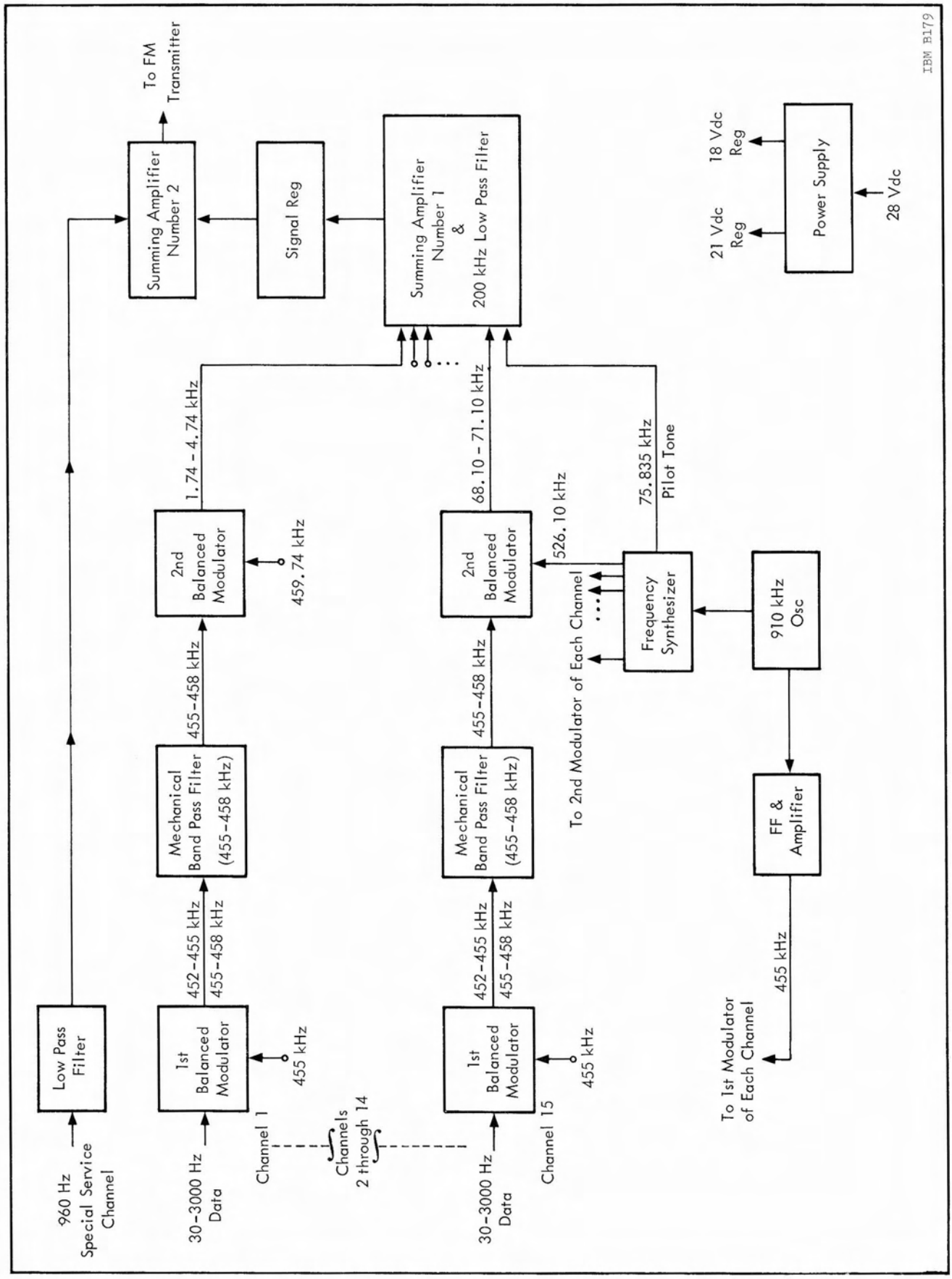


Figure 5.4-4 Block Diagram of Airborne SS Telemetry Assembly

5.4.4 PCM/DDAS TELEMETRY SYSTEM

The PCM/DDAS telemetry system serves a dual purpose in the Saturn Launch Vehicle. This system functions as a telemetry link for digital data (PCM/FM) and as a part of the DDAS. PCM/FM is required on the launch vehicle in order to obtain sufficient accuracy, with acceptable bandwidth efficiency, for digital data transmission from data sources such as the LVDC. The DDAS provides necessary measurement data to the LVDC. Before launch, it also provides measurements to the launch computer in the ground checkout stations (via coaxial cable).

To provide flexibility, the system is "built up" from several assemblies which may be combined as required in a particular stage application. The following assemblies may be used to "build up" a PCM/DDAS telemetry system:

- Mod 301 PCM/DDAS Assembly
- PCM RF Assembly
- Mod RDSM-1D Remote Digital Submultiplexer
- Mod 410 Remote Digital Multiplexer
- Mod 270 Multiplexer Assembly
- A remote analog submultiplexer which may be used with a Mod 270 Multiplexer Assembly
- Computer Interface Unit

MOD 301 PCM/DDAS ASSEMBLY

The Mod 301 PCM/DDAS Assembly is the central piece of equipment in both the telemetry link and the DDAS link. It provides the output signals for telemetry and automatic checkout.

The PCM/RF Assembly contains the signal conditioner, power amplifier, and RF transmitter for the telemetry link.

The Mod RDSM-1D Remote Digital Submultiplexer is used to connect digital data sources to the Mod 301 PCM/DDAS Assembly.

The Mod 410 Remote Digital Multiplexer is used in the IU to connect the LVDC to the Mod 301 PCM/DDAS Assembly.

The Mod 270 Multiplexer Assembly is used to connect analog data into the Mod 301 PCM/DDAS Assembly.

The remote analog submultiplexer may be used to submultiplex data being fed through the Mod 270 Multiplexer Assembly.

The Computer Interface Unit allows the LVDC, operating through the LVDA, to read selected measurement data which is being transmitted through the Mod 301 PCM/DDAS Assembly.

A brief functional description of the Mod 301 PCM/DDAS Assembly and the PCM/RF Assembly is given on the following pages. The multiplexers and the Computer Interface Unit are described in the following paragraphs.

The Mod 301 PCM/DDAS Assembly performs six major functions as follows:

- Scans the PAM wavetrains of several (1 to 6) Mod 270 PAM Multiplexer Assembles in a programmed sequence and combines these wavetrains into a single PAM wavetrain.
- Encodes the PAM samples in this wavetrain into 10-bit digital form.
- Accepts data in digital form and programs it into selected time slots in the output serial format.
- Generates the required frame and master frame identification codes, combines these codes with the digital and encoded analog data, and arranges the desired serial format for output.
- Provides a 600-kilohertz FM modulated carrier as the DDAS output, and an NRZ modulating output for the PCM RF Assembly.
- Provides the synchronization outputs necessary to synchronize the Mod 270 Multiplexer Assemblies and remote digital submultiplexers.

Figure 5.4-5 is a functional block diagram of the Mod 301 PCM/DDAS Assembly. It composed of the six functional subsystems listed below:

- PAM scanner (and associated program patch).
- Analog-to-digital converter.

- Digital multiplexing and formating logic.
- Clock programming and timing logic.
- DDAS voltage controlled oscillator.
- Power supplies.

PAM Scanner. The PAM scanner connects one or more Mod 270 Multiplexer Assembly outputs in a programmed sequence to the ADC input for digitizing. By means of the scanner program patch, any multiplexer arrangement compatible with the system application can be accomodated. Up to three multiplexer arrangements (modes) may be programmed at the scanner patch, and the automatic switching between modes is accomplished by applying external 28-volt dc commands.

The scanner gates are 4-transistor, back-to-back, balanced configurations which switch both legs of the PAM circuit of each PAM multiplexer. The transformer coupling of the switching logic input of the gates provides a favorable impedance condition for the PAM signals.

The PAM scanner and program patch are packaged on printed circuit cards which plug into the Mod 301 PCM/DDAS Assembly.

Analog-to-Digital Converter. The analog-to- digital converter encodes the PAM signals received through the PAM scanner by the successive approximation method. The digital output is fed in parallel form to a parallel storage register according to commands received from the programming and timing logic. Figure 5.4-6 shows a functional block diagram of the ADC. Its operation is non-synchronous (not synchronized with other parts of the system) and at a clock rate of approximately 250 kilohertz which is provided by a blocking oscillator.

Encoder command pulses at the system word rate are provided by the programming logic. When an encode command is received by the ADC, it begins an encode cycle at its own clock rate; this requires approximately 56 microseconds. At the end of the cycle, the ADC register switches have been set to the digital equivalent of the analog quantity present at the buffer input during the encode cycle. The logic levels from the register switches provide a parallel digital output until the next encode command arrives. The register switches are then reset and a new encode cycle follows.

Digital Multiplexing and Formating Logic (See Figure 5.4-7). The function of the digital multiplexing and

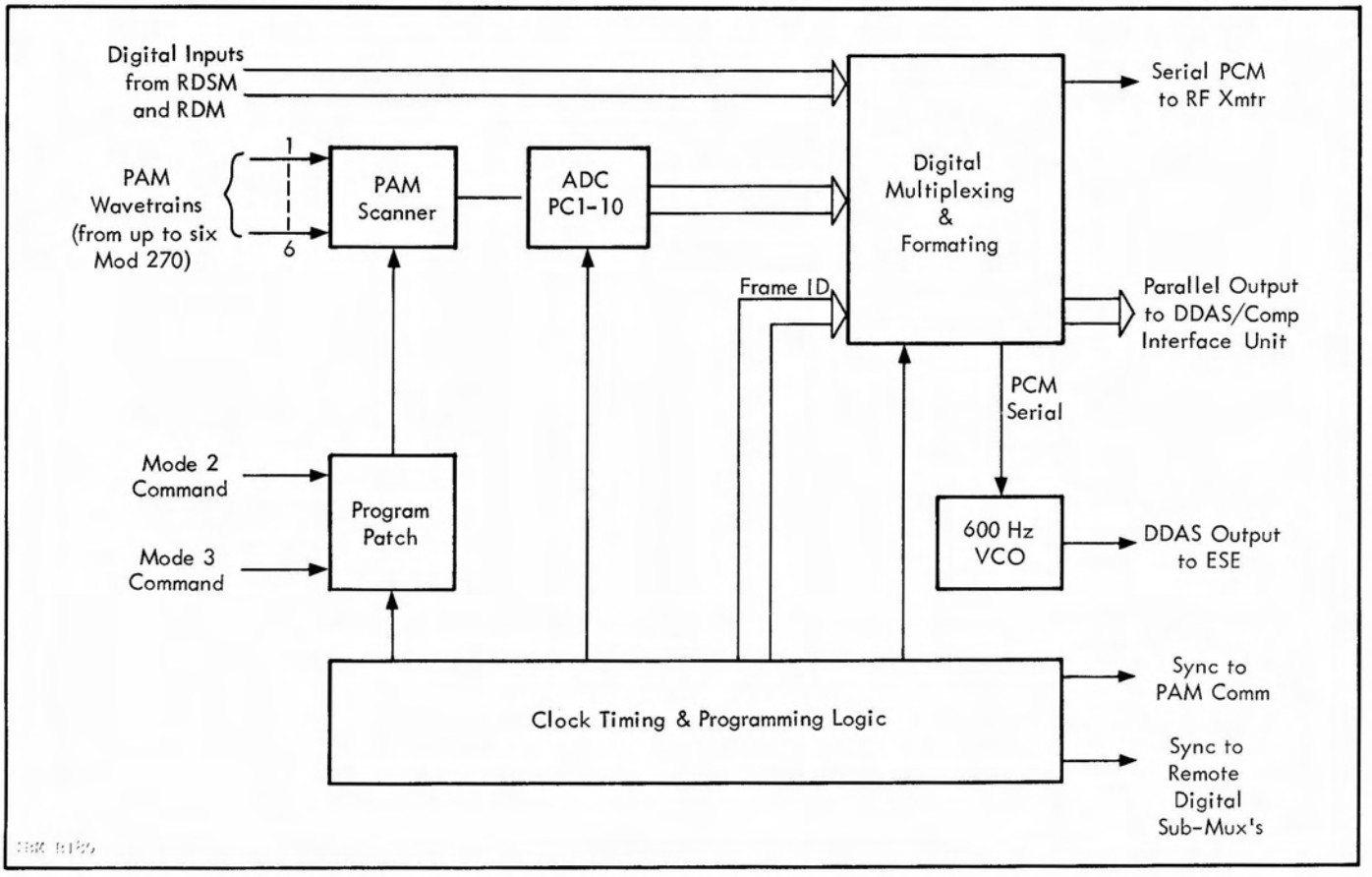


Figure 5.4-5 General Block Diagram - PCM/DDAS Assembly

formating logic is to combine the encoded data from the ADC, externally generated digital data, and frame (and master frame) identification words into the required output sequence. The specific time slot into which data is inserted is controlled by command pulses from the programming and timing logic. The 10-bit output of the ADC is transferred into the parallal storage register by each word rate clock pulse (so long as the encoder inhibit bus is unenergized). When the encoder inhibit bus in energized, the ten AND gates at the ADC output are disabled, and the ADC output is not transferred into the parallel storage register.

Up to ten 10-bit groups of digital data from external sources can be programmed into selected time slots at any of the four system sampling rates. The data is accepted in parallel. A zero-volt level represents a logical "0" and a positive level represents a logical "1". Inputs are buffered and then shifted into a magnetic core register before being transferred into the parallel storage register. The MCR provides temporary storage and dc isolation of the data source. Each MCR, along with its ten associated buffers and other circuits, is powered by an individual supply which is dc isolated. This permits monitoring of several digital data sources without interconnecting their dc commons.

A WRITE command to an MCR causes the 10 bits of data to be stored in the magnetic cores. The WRITE command is programmed (at the command program patch) to occur before the time for transfer of the data into the PSR. Typically, the command occurs during the previous word time, but it can be programmed to occur at any word time after the previous sample of the specific channel is read into the PSR. For example, several 10-bit data sets can be written into their MCR's simultaneously and then placed into specific time slots in the output format. This mode of operation is utilized in monitoring a 40-bit set of data from the LVDC.

The READ command to the MCR is timed to transfer the data into the output register during the least significant bit time of the previous word time. READ commands are also OR'd together to provide a function for inhibiting the transfer to ADC data through the encoder gate.

The digital input section has 10 channels. Each channel will accept a 10-bit input in parallel form. To increase the data handling capacity, the input section may be fed from 10-channel remote digital submultiplexers.

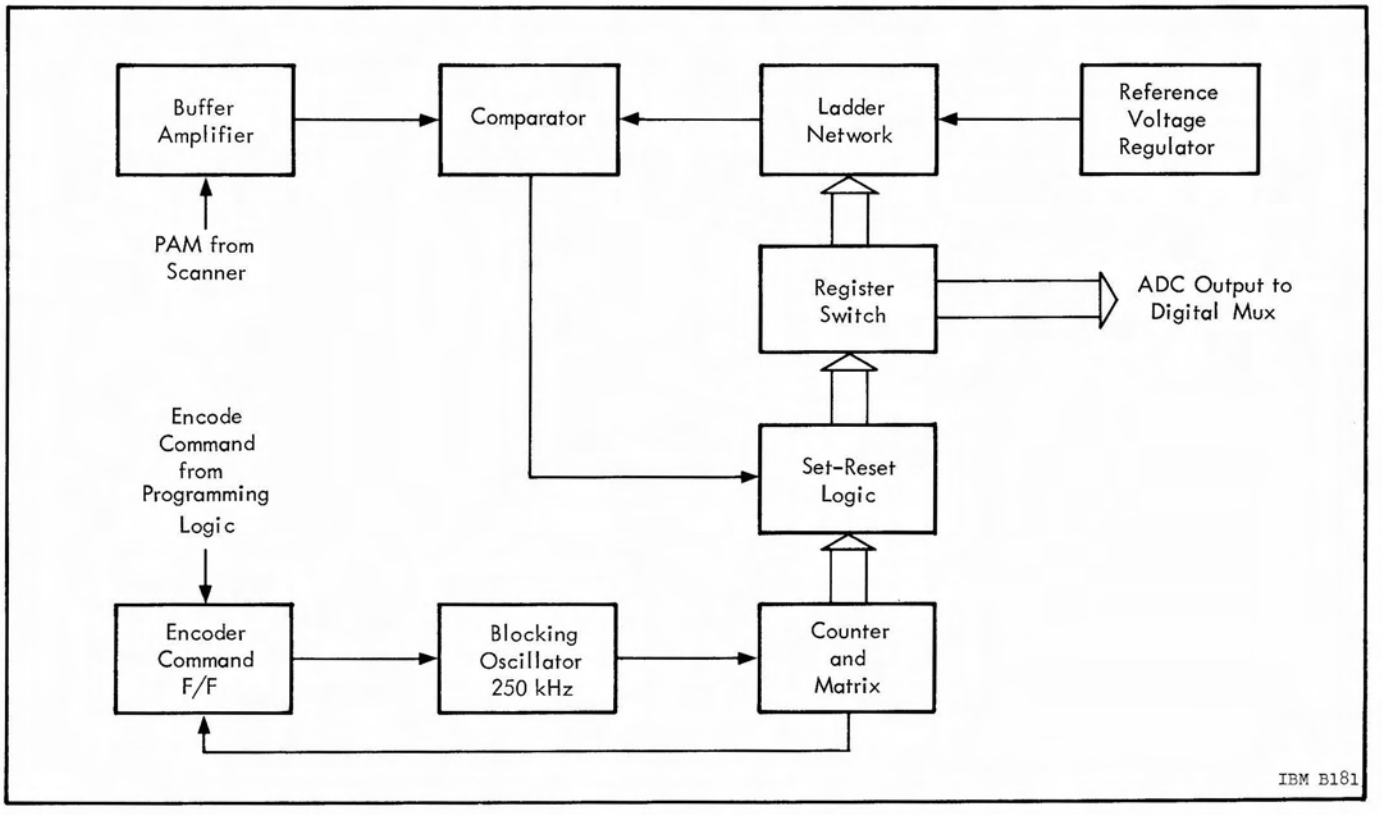


Figure 5.4-6 Analog-to-Digital Converter Block Diagram

The frame identification logic generates three unique code groups and inserts them consecutively during the last three word times of the PCM/DDAS frame. Once each 30th frame, the frame ID logic receives a signal from the frame ID reversal flip flop. This signal causes the frame ID logic to complement (reverse) all bits in the frame ID code of the 30th frame. This forms the master frame identification code. The code group is as follows:

Word 29B	1 0 1 1 0 1 1 1 1 0
Word 30A	1 0 1 0 0 0 1 0 0 1
Word 30B	1 1 0 0 0 0 0 1 1 0

The serializing logic shifts the contents of the PSR bit-by-bit into the NRZ flip flop thus forming the serial NRZ output. The states of the bits per word counter are decoded, combined with the PSR outputs, and clocked to provide set-reset pulses to the NRZ flip flop. The two complementary outputs of the NRZ flip flop are buffered and provided at an output connector for use as a modulating input to the PCM/RF Assembly. One side of the NRZ flip flop provides a modulating input to the DDAS/VCO.

Clock, Programming, and Timing Logic. (See Figure 5.4-8) The clock, programming, and timing logic provides the timing signals necessary for the Mod

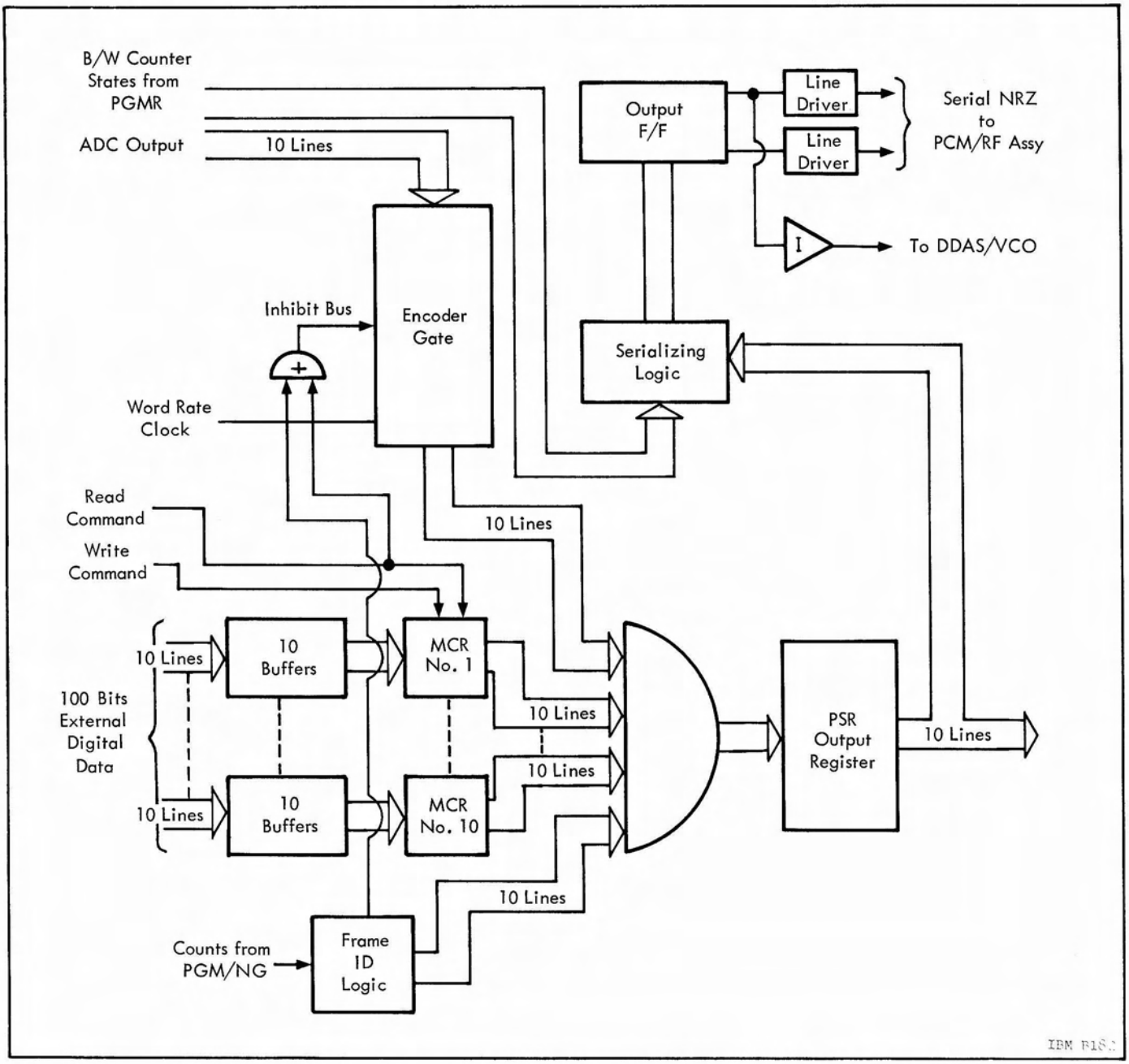


Figure 5.4-7 Digital Multiplexing and Formating Logic

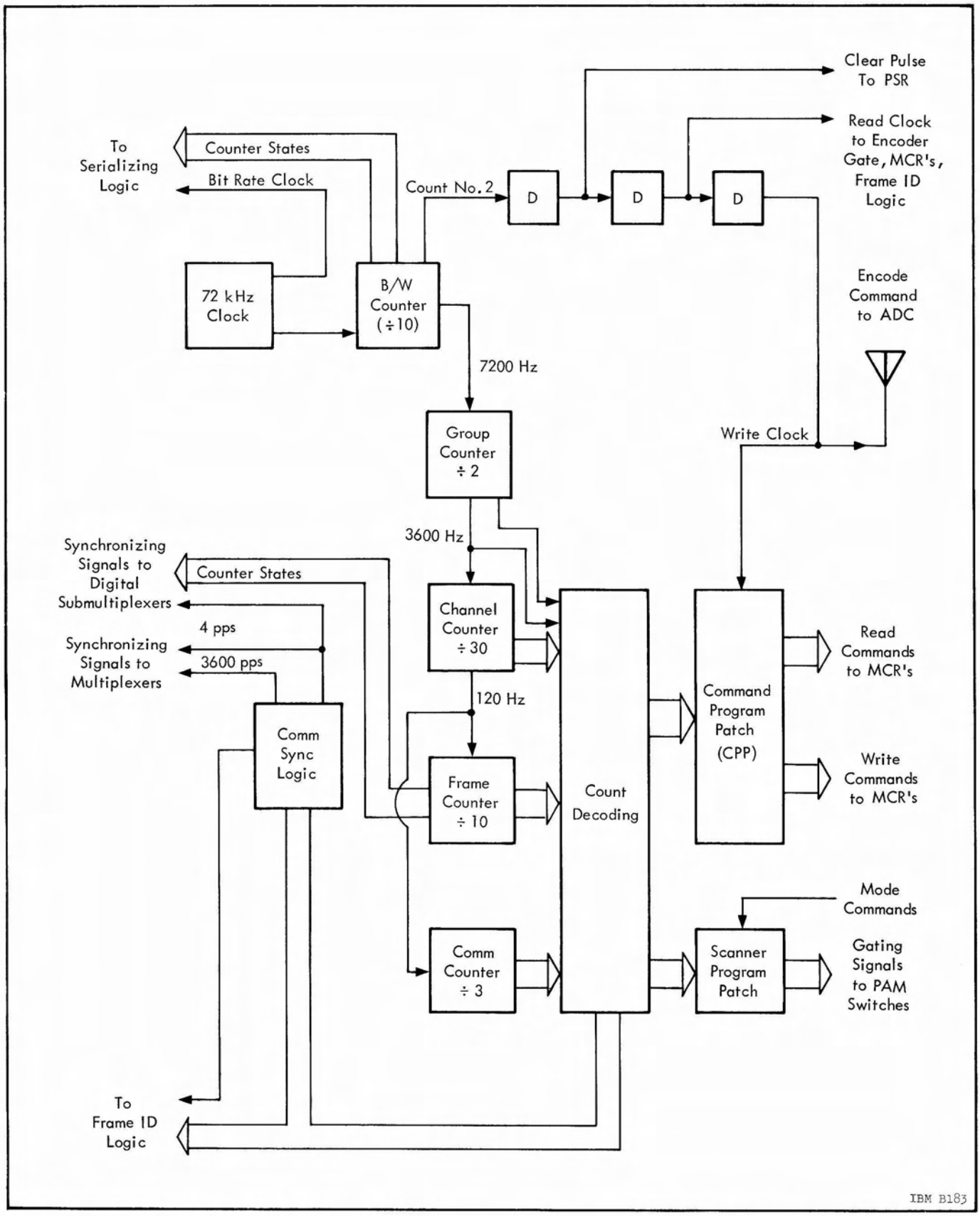


Figure 5.4-8 Clock Programming and Timing Logic Block Diagram

301 PCM/DDAS Assembly as will as signals required to synchronize logic in other telemetry assemblies.

One phase of the 72-kilohertz clock provides bit rate pulses to the serializing logic while the other phase steps the B/W counter. The outputs from each trigger of the B/W counter are decoded in the serializing logic and used to select stages of the PSR to form the serial bit train which controls the NRZ flip flop.

Count "2" of the B/W counter is decoded and initiates a series of three successive timing pulses which are 1.75 microseconds apart. The first (clear) pulse occurs approximately 2 microseconds after the least significant bit is transferred to the NRZ flip flop and resets all 10 stages of the PSR. The second pulse (READ clock) provides the correct timing phase for the transfer of data into the PSR from the ADC, the frame ID logic, or an MCR. The third pulse (WRITE clock) provides the proper phasing for writing external digital words into the MCR's. This pulse also signals the ADC to proceed with digitizing the succeeding analog signal.

The reset pulse of the B/W counter steps the group counter. This pulse occurs during the 2^2 bit time because of offset in the serializing logic. This allows settling time for the analog data inputs, (which are gated by the scanner in synchronism with the group counter) before the ADC begins digitizing. The group counter is a divide-by-two counter (one flip flop).

The reset pulse of the group counter steps the channel counter at a rate of 3600 pps. This consists of a divide-by-five counter and a divide-by-six counter which together form a divide-by-thirty counter.

The reset of the channel counter steps the divide-by-ten frame counter and the divide-by-three multiplexer counter. Both of these counters are stepped at the PCM/DDAS frame repetition rate of 120 times per second.

The 4 counters define each time slot in the PCM/DDAS format. The divide-by-two group counter provides the timing for the interlacing of two multiplexer groups. Each group is comprised of up to three Mod 270 Multiplexers which are controlled by the divide-by-three multiplexer counter. The divide-by-three multiplexer counter provides timing for the sharing of specific mainframe time slots. The divide-by-thirty channel counter steps in sychronism with the sampling action of the 30 by 120-channel analog gates (each sampled 120 times per second) in the Mod 270 Multiplexer Assemblies. The divide-by-ten frame counter steps in synchronism with the 10 by 12 submultiplexers (10 gates sampled 12 times per second).

The counts of each of the 4 counters are decoded and routed to the command program patch. A programming arrangement provides selection of READ and WRITE commands corresponding to specific time slots. These commands provide the timing signals to the MCR's necessary to place external digital data inputs into a specific format. Decoded outputs of the group counter and multiplexer counter are also routed to the scanner program patch, which provides selection of the multiplexer scanning sequence. Up to three multiplexer-scanning sequences may be programmed on the scanner program patch. A specific sequence is selectable by an externally generated mode command. The mode commands are 28-volt dc signals from GSE, the vehicle command, or other sources appropriate to the application. (Note: Mode 1 does not require application of an external mode command voltage.)

The control logic also generates 3 sets of waveforms used for synchronizing logic in other assemblies to the clock and frame rates of the Mod 301 PCM/DDAS Assembly. Two sets of waveforms provide the correct waveform shape, frequency, and phase for synchronizing Mod 270 Time Division Multiplexers. The two waveform sets are identical except for the offset in phase necessary for interlacing group A and group B multiplexers. Each set consists of a 3600-hertz square wave and a 278-microsecond pulse with a repetition rate of 4 times per second.

The third waveform set consists of an output from each stage of the divide-by-ten frame counter and a 3600-hertz square wave. This set of waveforms is utilized to synchronize remote digital submultiplexer assemblies.

DDAS Voltage Controlled Oscillator. The DDAS/VCO provides an FM modulated carrier (600 kilohertz) for transmission of the PCM/DDAS signal (via coaxial cable) to DDAS receiving equipment.

A 600-hertz transistor multivibrator is bias modulated by the serial NRZ data. An amplifier preceding the multivibrator presents an impedance of approximately 50 kilohms to the NRZ data input and also provides a non-linear modulating characteristic which makes the frequency deviation relatively insensitive to variations in the input data logic levels. A frequency deviation of approximately ± 35 kilohertz is used.

A common-collector buffer stage drives a filter which is designed to remove harmonics from the multivibrator output. This output stage delivers a nominal 75 megawatts to a 100-ohm load.

Power Supplies. There are six separate power supplies used in the Mod 301 PCM/DDAS Assembly.

A 28 Vdc-to-28 Vdc converter regulates the primary 28 Vdc power to the assembly and isolates the digital return in the Mod 301 PCM/DDAS Assembly from the vehicle 28 Vdc return line. It supplies 28 Vdc ± 1 percent at a nominal 25 watts output to the remaining power supplies in the system.

The 6 Vdc card accepts + 28 volts from the converter and provides + 6 Vdc at 250 mA, and - 6 Vdc at 50 mA. The + 6 Vdc output provides collector voltage to the programming, timing, and scanning portions of the Mod 301 PCM/DDAS Assembly. The - 6 Vdc output provides base bias voltage to the same circuits.

The +18 Vdc and +5 Vdc card accepts, regulates, and converts 28 Vdc to +18 Vdc and +5 Vdc. All circuit returns on this card are common. These voltages are used in the non-critical and digital circuits in the ADC (encoder) section of the assembly.

The -9 Vdc supply card provides bias voltage for the encoder section of the Mod 301 PCM/DDAS Assembly.

The +15 Vdc regulated supply obtains its input voltage from the +18 Vdc supply. The +15 Vdc is used as the reference voltage from which the comparison voltage is derived for the ladder network in the encoder.

The + 12 Vdc supply is a simple Zener-resistor divider. It is used to provide bias voltage for the circuits on command program patch B.

PCM/RF ASSEMBLY

The PCM/RF Assembly contains the modulator and the RF transmitter for the PCM/FM telemetry link. Figure 5.4-9 shows a block diagram of this assembly.

The assembly consists of a frequency-shift keyer, a premodulation filter, a hybrid 3-watt FM transmitter, and a single-stage RF power amplifier. These components are powered by a solid-state regulated power supply. They are mounted to system chassis.

The input signal applied to the assembly is a 72,000 bits per second-NRZ digital signal from the Mod 301 PCM/DDAS assembly. The signal amplitude ranges from 6 to 10 volts peak to peak; rise and fall times are from 0.5 to 3.0 microseconds. Input sine wave signals of 4 volts peak to peak and zero to 100 kilohertz will not modulate the transmitter.

Premodulation filtering of the digital signal restricts sideband components outside a band of plus or minus 250 kilohertz around the carrier center frequency to 68 db below the level of the unmodulated carrier. The RF power output is 15 watts. The center frequency of the RF carrier is selectable to any frequency between 225 and 260 megahertz with center frequency stability and accuracy within 0.01 percent. A positive voltage excursion of the PCM/RF Assembly input signal produces an increase in carrier frequency.

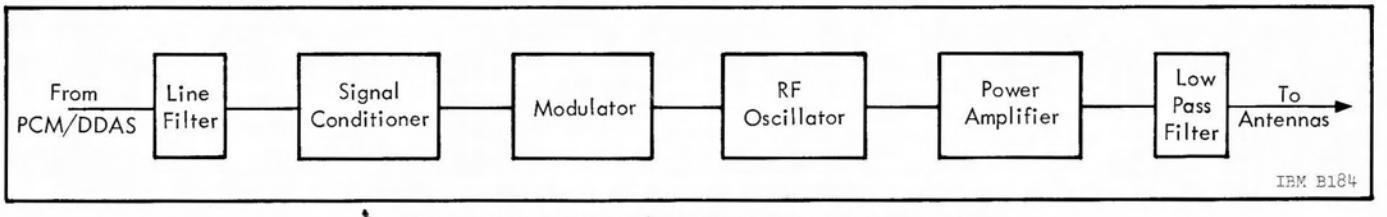


Figure 5.4-9 PCM/RF Assembly Block Diagram

SECTION 5.5

MULTIPLEXERS

5.5.1 MOD 270 MULTIPLEXER

The Mod 270 Multiplexer Assembly (time division) is basically a 30 by 120 multiplexer (30 channels, each sampled 120 times per second). It accepts voltage inputs in the range of 0 to 5 volts (high level data) and provides two PAM wavetrain outputs, one (with pedestal) for input to a 70-kilohertz ±30 percent FM/FM subcarrier and a second (without pedestal) for the PCM/DDAS Assembly. A block diagram of the Mod 270 Multiplexer Assembly is shown in Figure 5. 5-1.

A time-division multiplexer consists of three major parts: a set of switches or gates for each output channel, a timing device (logic generator), and a power supply.

The gates, acting as electronic switches, sequentially connect the data inputs to the multiplexer output on commands from the timing circuits.

The timing, or logic, circuits provide the signals which open and close the data gates at the desired times and in the desired sequence.

Multiplexers are normally located in proximity to data sources in order to minimize cabling weight. Each multiplexer houses sampling gates for up to 234 data channels. By means of flexible plug-in modules, variations in numbers of channels and sample rates may be accomplished within the multiplexers. These multiplexers also accept pre-sampling filters where required for specific measurements. Remotely located submultiplexer assemblies may also be used to increase the capacity of each individual multiplexer to 270 channels.

Twenty-seven of the thirty primary channels are data channels while the remaining three are utilized for amplitude references and PAM frame identification. Ten-channel gate modules, which plug into the assembly, may be used to submultiplex primary channels 1 through 23. Each of these 10 sub-channels then provides a sampling rate of 12 times per second. Any number of the 23 channels may be submultiplexed or utilized as 120-sample-per-second channels. When used at the primary sample rate, a submultiplexer "dummy" card (or a pre-sampling filter if required) is inserted in place of the submultiplexer module. The four remaining primary data channels (24, 25, 26, 27) are utilized as 120-sample-per-second channels. Each of the 27 primary data channels may be submultiplexed external to the basic assembly.

A zero amplitude reference is inserted on channel 28 of the output wavetrains except in the frame corresponding to sub-channel 10 (where a 5-volt amplitude reference is inserted to provide master frame identification). Channels 29 and 30 carry a 5-volt reference level and are bridged together to form PAM frame identification. Except for the channel 29-30 bridge, all channels are inserted as 50 percent duty cycle pulses on both output wavetrains. A zero pedestal of 1. 2 volts is added to the wavetrain output applied to the 70-kilohertz VCO of the PAM/FM/FM telemetry system. The output wavetrains have a pulse rate of 3600 pps.

CALIBRATOR

A calibration generator, located in the assembly, provides in-flight calibration capability. Calibration is initiated by an external command which in the Saturn telemetry system is provided by the TM Calibrator (Mod II). When a calibrate command is received, the calibration generator delays its sequence until the beginning of the following master frame. It then applies a sequence of five calibration voltages to all data channels (channels 28, 29, and 30 are unaffected by the calibration). The calibration voltage levels are in order: 0, 25, 50, 75, and 100 percent of full-scale data voltage. Each voltage level is sustained for one master frame (80 milliseconds), requiring approximately 400 milliseconds for the complete sequence. Section 5. 6 discribes the calibration function in greater detail.

SYNCHRONIZATION

Internal logic functions of the Mod 270 Multiplexer Assembly operate from its internal 3600-hertz multivibrator clock. However, the sample and frame rates can be synchronized to external pulses of the correct frequency and waveform. In the Saturn telemetry system, these synchronizing signals are provided by the Mod 301 PCM/DDAS Assembly. The synchronizing waveforms consist of a 3600-hertz square wave and a 4 pps pulse approximately 278 microseconds in duration occurring during channel one of each 30th frame.

The Mod 270 Multiplexer Assembly also provides synchronizing signals as outputs. These are identical to the waveforms previously described, except the frame sync pulse has a repetition rate of 12 pps instead of 4 pps. See Figure 5. 5-2. These synchronization outputs are normally utilized to control remote submultiplexer packages.

SUBMULTIPLEXER

The submultiplexers are composed of selection gates that subdivide the main multiplexer channels. Ten submultiplexer channels are connected to each

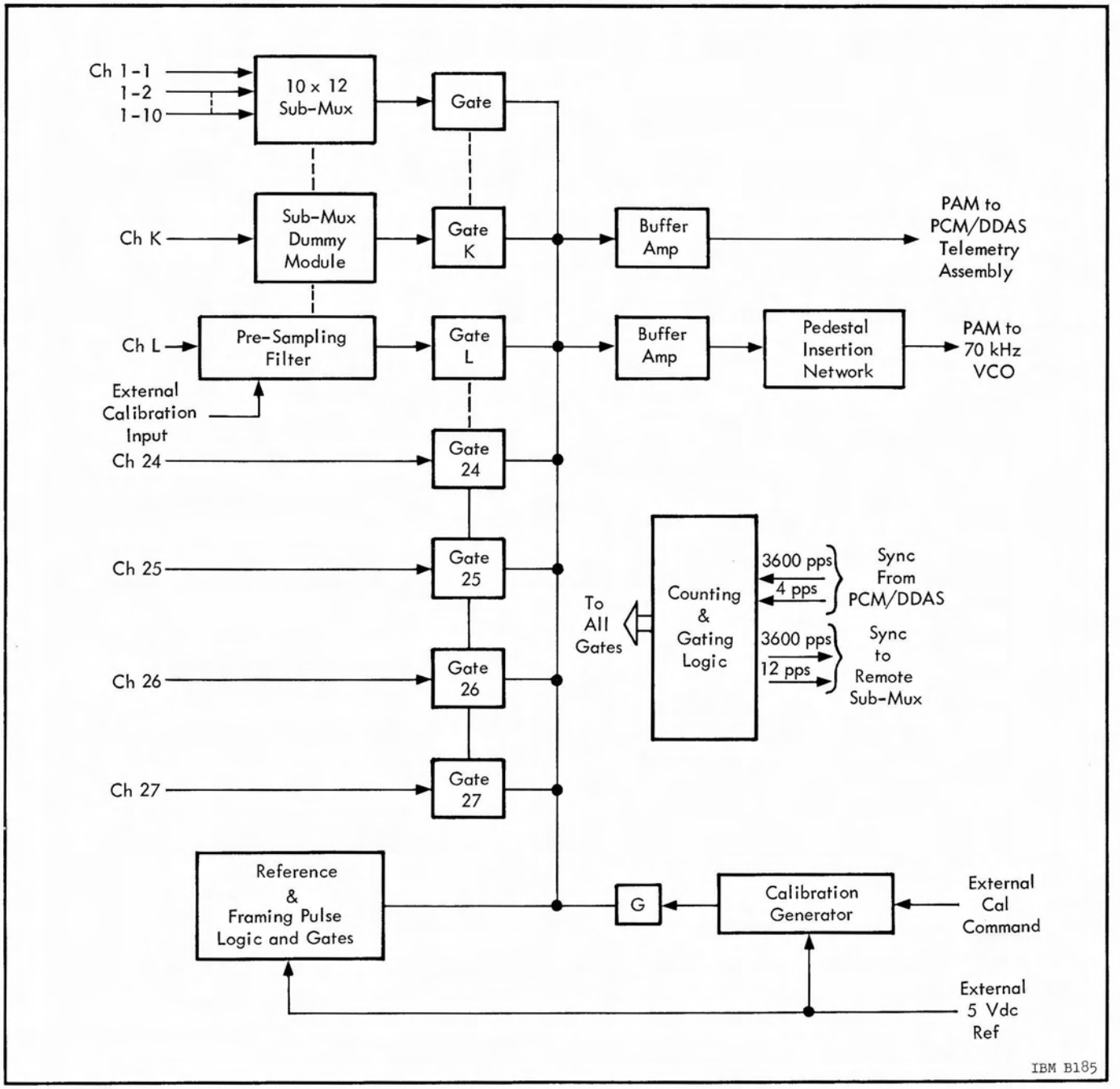


Figure 5. 5-1 Mod 270 Multiplexer Block Diagram

main multiplexer channel, thus reducing the sampling rate from 120 per second to 12 per second.

Each gate functions in the following manner: The input side of a gate is tied to the data to be sampled, and the output side is tied to the main multiplexer channel. The normally open gate closes upon application of a current pulse to the transformer to allow information to pass through to the main multiplexer. This current pulse is obtained by grounding one side of the transformer and connecting the other side to the decoded output of the "T" counter.

The gates are connected in columns of ten, and all outputs of a particular column are connected to one main multiplexer channel input.

The submultiplexer "dummy" card is used when a sampling rate of 120 times per second is required. This card, used in place of the submultiplexer card, provides a direct path from the data being sampled to the main multiplexer board. An RC load mounted on this board (the same as on all submultiplexer cards) prevents data spikes from being passed through.

The characteristics of the Mod 270 Multiplexer Assembly are given in Table 5.5-1.

Table 5.5-1 Mod 270 Multiplexer Assembly Performance Characteristics

Characteristic	Specification
Time Stability	
Clock rate	3600 Hz + 2%
Duty cycle	139 us ±5%
Linearity (best straight line)	± 0.1%
Accuracy	
Output of amplifier (without pedestal)	± 0.1%
Output of amplifier (with pedestal)	± 0.5%
Pedestal Stability	1.2 V ± 50 mV
Reverse Current (all channels at 5 V except channel under test which is short circuited)	2 uA (max)
Input Impedance of Channel (excluding 100k input terminating resistor)	5 mego (min)
Output No. 1 (without pedestal)	100 Ω (max)
Output No. 2 (with pedestal)	2k (max)

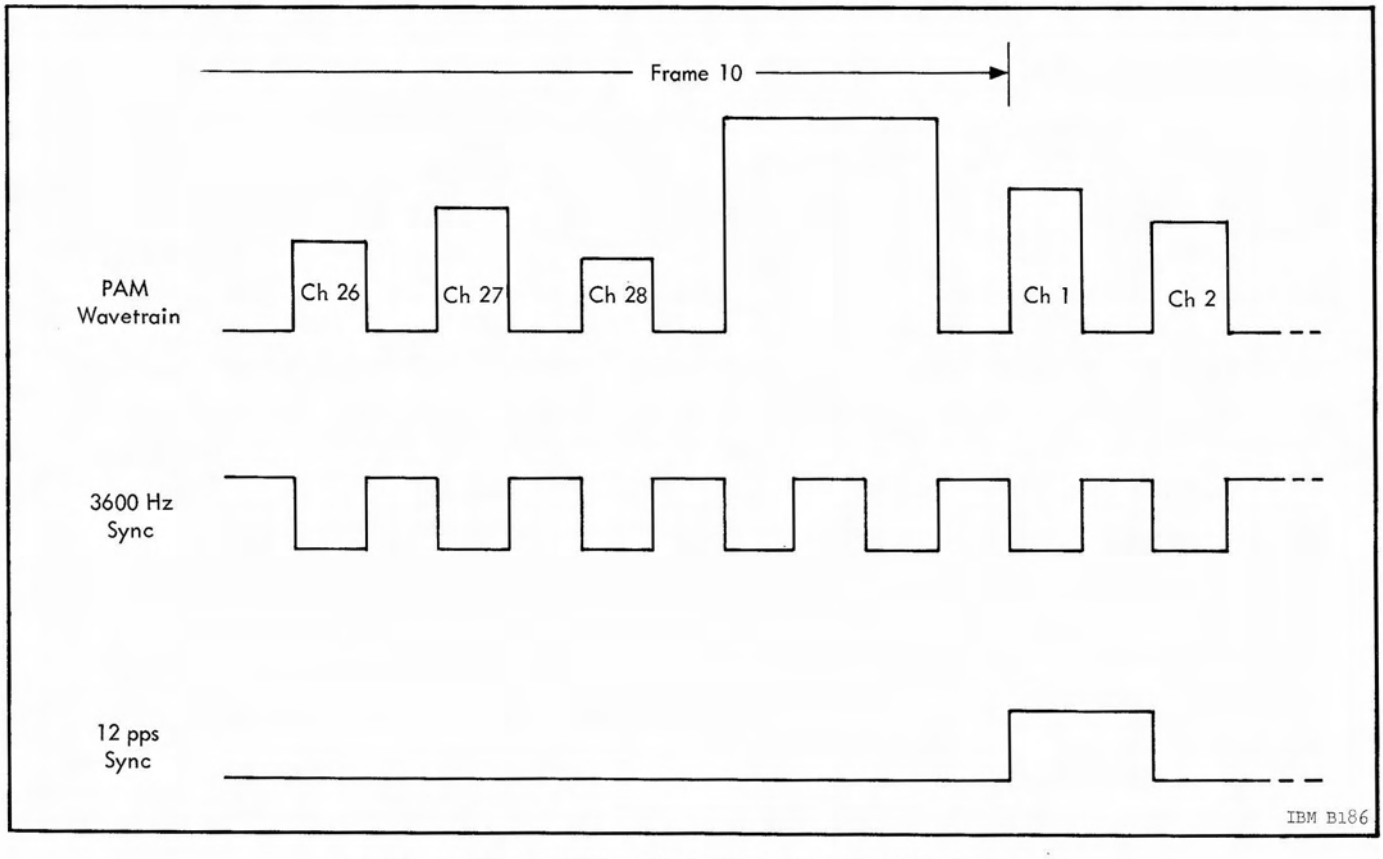


Figure 5.5-2 Mod 270 Multiplexer Assembly Waveforms

5.5.2 REMOTE DIGITAL SUBMULTIPLEXER (MOD RDSM–1D)

The Remote Digital Submultiplexer provides additional digital data handling capability to the PCM telemetry system. A maximum of 100 inputs are provided (see Figure 5. 5-3). These inputs are sampled sequentially in groups of 10 and then applied to an output register with 10 outputs. The inputs may be utilized individually or in groups to form digital words. The RDSM handles digital or discrete information only; i. e., its inputs and outputs are set voltage levels which represent either ON-OFF conditions or binary numbers.

The PCM programmer located in the Mod 301 PCM/DDAS Assembly controls the sequential sampling action of the RDSM. The control signal consists of a 4-bit binary word which arrives in parallel format and represents timing information.

The RDSM provides a high degree of flexibility of application by use of isolated input gates and isolated power supplies. The unit has two isolated power supplies; regulated 20 Vdc and +5 Vdc gate-collector supply. The regulated 20 Vdc is derived from the 28 Vdc vehicle supply by a dc-to-dc converter. The +5 Vdc gate supply is developed on each gate card by rectifying and filtering the 3600 pps clock signal from the PCM programmer.

Figure 5. 5-4 presents the logic symbols and defines the logic elements. The binary inputs to word gates are 0 ± 0. 5 volt for a logical "0" input and 7 + 3 volts for a logical "1" input (In a Type IV RDSM, a logical "1" input is 28^{+4}_{-10} Vdc). The binary outputs from the RDSM and the PCM programmer are the same, 0 ± 0. 5 volt and 5 ± 1 volts.

An auxiliary card is available with the RDSM. It may be added to the unit to adapt it to a specific input. This auxiliary card is a divide-by-six (+6) card which has an output signal that is used to cycle the liquid level measuring system.

5.5.3 REMOTE DIGITAL MULTIPLEXER (MOD 410)

This assembly will be utilized in the Instrument Unit to take the 40-bit (parallel) words from the LVDC and provide 10-bit words at the output to feed the LVDC words into the Mod 301 PCM/DDAS Assembly for transmission to the ground. (See Figure 5. 5-5.)

A more detailed diagram is given in Figure 5. 5-6. There are 40 data input bits from the LVDA which are fed into the MCR cards for storage and subsequent insertion into the proper time slots of the system format. These time slots will be determined by the command program patch. From the Mod 301 PCM/DDAS Assembly multiplexer, there are two sync pulse inputs to the 410 timing logic; a 3. 6-kilohertz group sync pulse, and a 4-hertz master frame sync pulse. Delay circuits in the timing logic provide the correct sequencing of the write, clear, and read commands. The timing logic also steps the 3, 5, 6, and 10 counters. The outputs of the counters are decoded by the command program patches A and B to provide assembly timing which is sufficient to accurately define the occurrence of time slots in the system format.

5.5.4 VIBRATION MULTIPLEXER

The Mod 245 Multiplexer Assembly is a time-division multiplexer which is used in conjunction with the SS/FM Assembly multiplexer and the FM/FM multiplexer link. This unit can sample a maximum

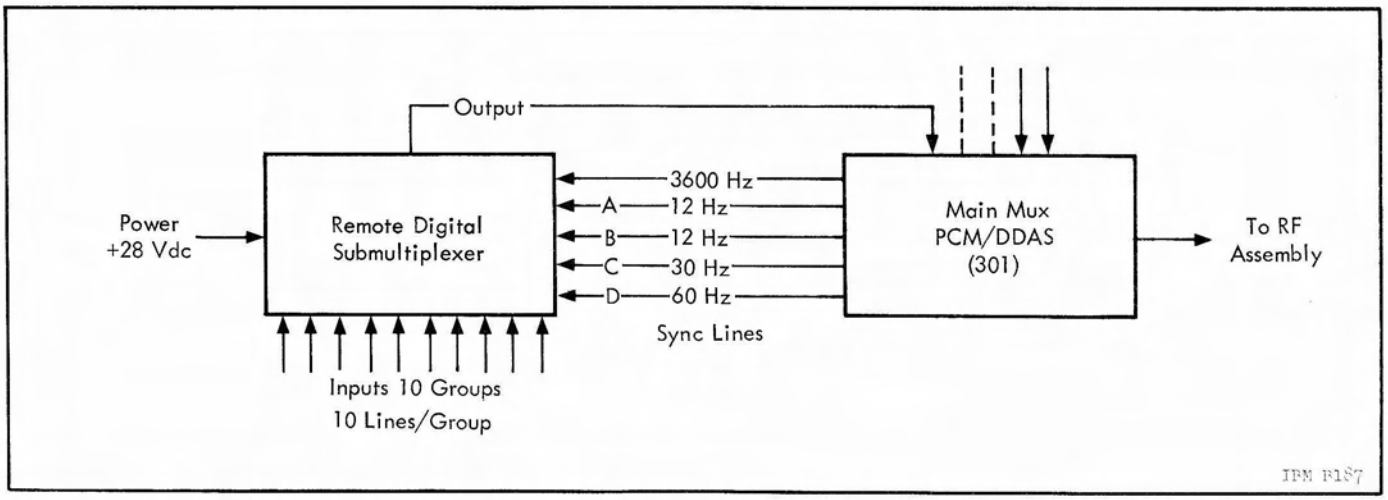


Figure 5. 5-3 Block Diagram of RDSM Inputs and Outputs

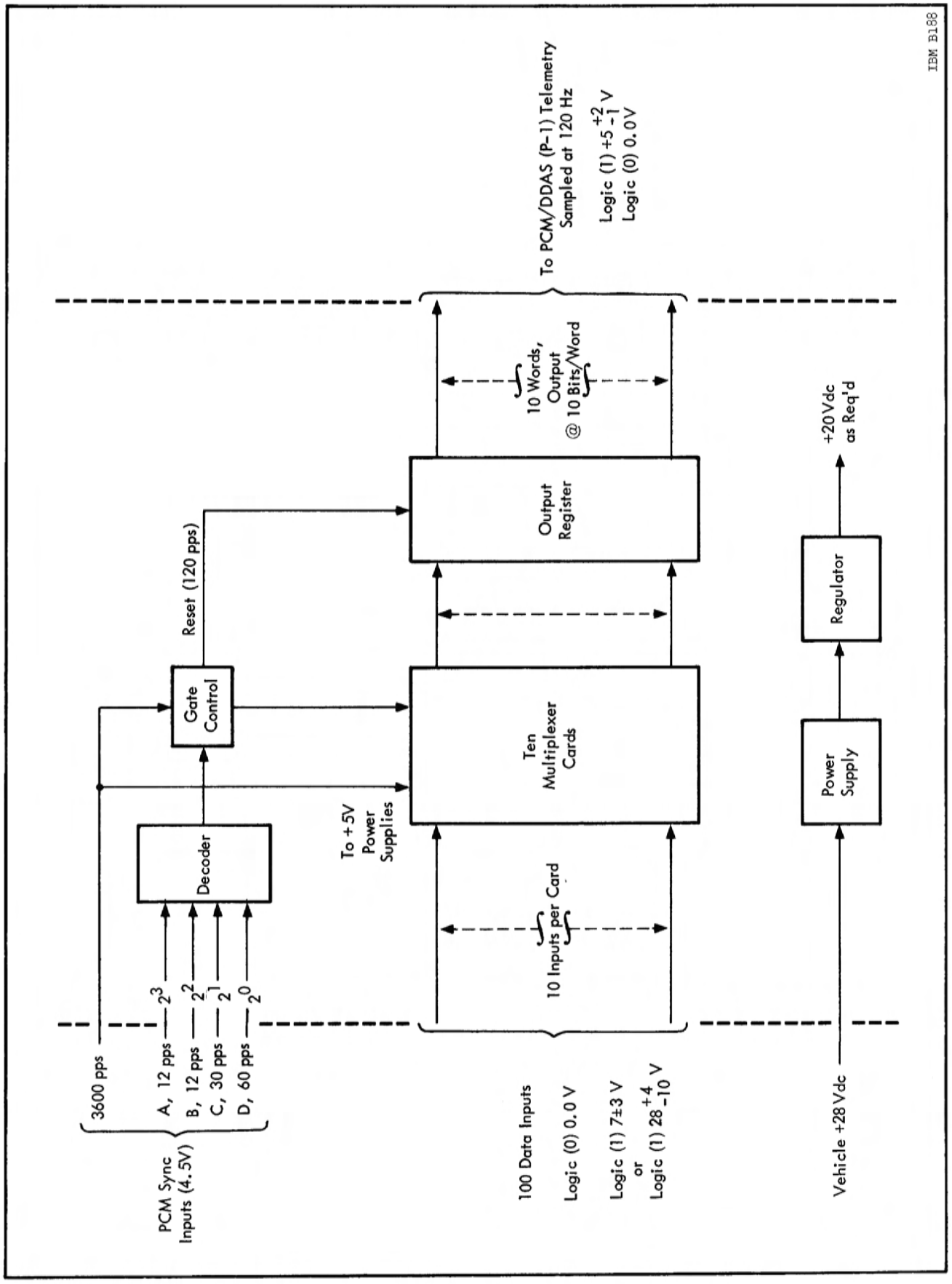


Figure 5.5-4 Remote Digital Submultiplexer Simplified Block Diagram

of 80 data channels and provide 16 channels of output data 15 of which feed the SS/FM Assembly multiplexer and 1 channel feeds the FM/FM multiplexer. It is primarily used for multiplexing wideband vibration data.

The Mod 245 Multiplexer Assembly, Figure 5. 5-7, consists of 20 plug-in subassemblies. Of these 20 subassemblies, 4 are common subassemblies (1 logic and timing unit, 1 regulator unit, 1 inverter unit, and 1 driver and voltage-controlled oscillator unit). The remaining 16 subassemblies are multiplexer units.

The multiplexer units are made up of 3 types. They are as follows:

- Two multiplexed channels with a sample period of 5. 7 seconds each.
- Four multiplexed channels with a sample period of 2. 9 seconds each.
- Five multiplexed channels with a sample period of 2. 3 seconds each.

The 3 types of multiplexer units all use 12-second sampling cycles. The different sample times are separated by "dead time". The sampling cycles are separated by longer periods of "dead time". Frequency response of the input is 0 to 5000 hertz. Input impedance is a constant 100 kilohms. Input signal level can be 0 to +5 volts peak to peak, or 0 to +5 volts dc. Output impedance is 1 kilohm at 0 to 5000 hertz.

A dummy unit is used for continuous data. Other than a marker, no timing is required.

Additional timing information is also transmitted using a 960 ± 70-hertz voltage controlled oscillator for data reduction purposes. This is fed into the special service channel in the SS/FM Assembly.

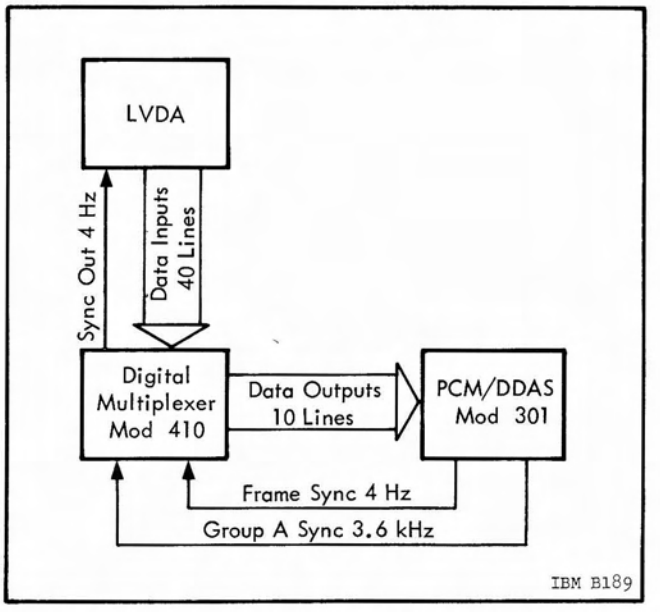


Figure 5. 5-5 Inputs and Outputs of Mod 410 Multiplexer

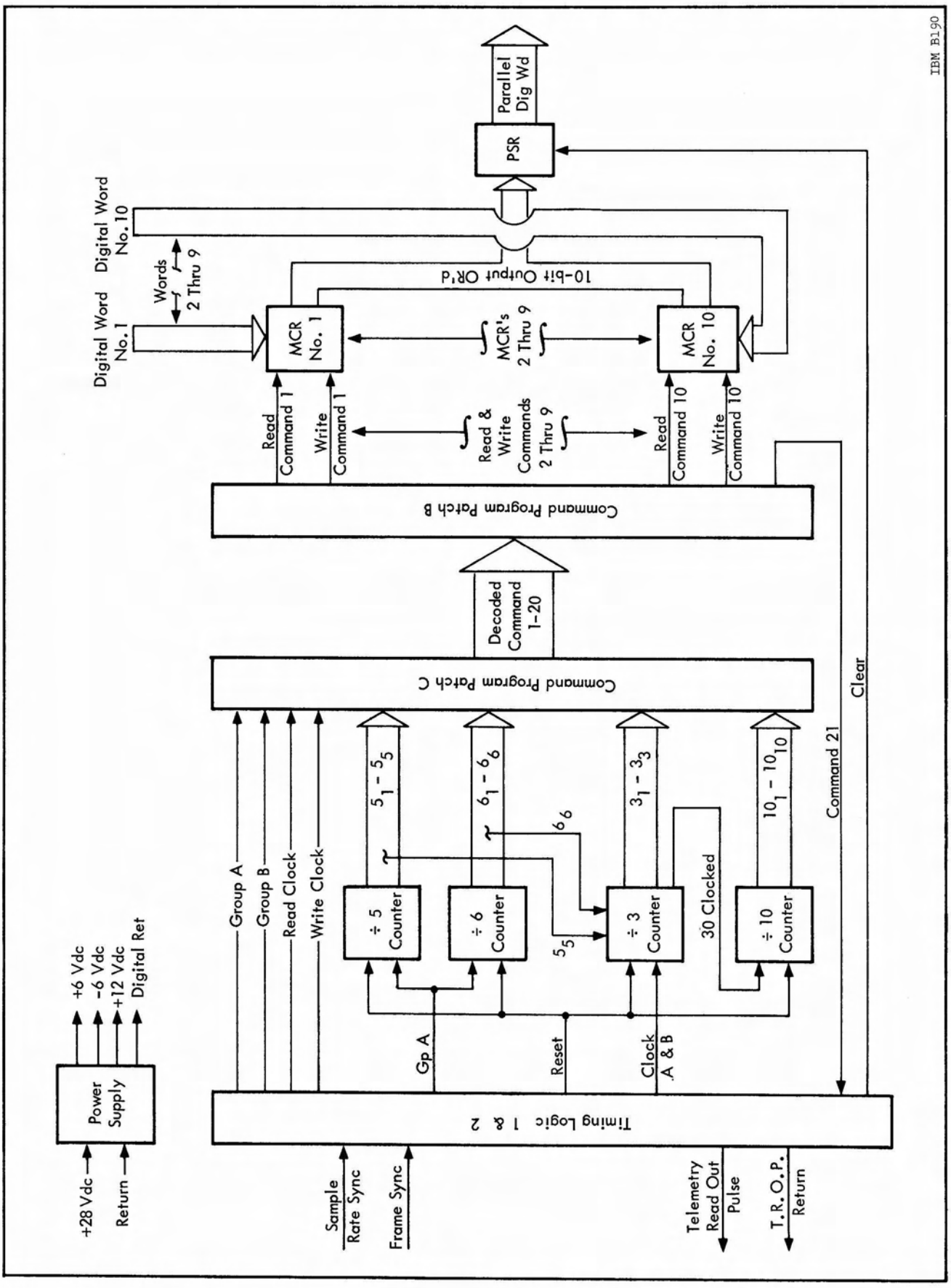


Figure 5.5-6 Block Diagram of Mod 410 Multiplexer

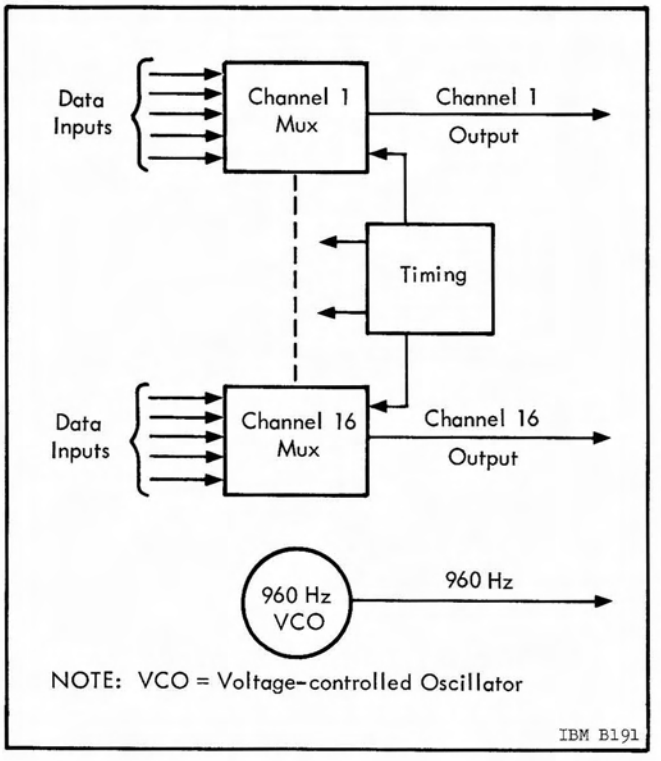


Figure 5. 5-7 Block Diagram of Mod 245 Multiplexer

SECTION 5.6

TELEMETRY CALIBRATION SUBSYSTEM

The purpose of the telemetry calibration subsystem is to assist in determination of telemetry equipment accuracy. This is done by furnishing selected telemetry equipment with known, precise inputs in place of the normally broadcast measurement signals. The normally broadcast signals are compared to the calibrated broadcast signals to obtain the exact degree of telemetry equipment accuracy.

TM calibration is used during flight and prelaunch checkout. During flight, the TM calibration is controlled by the LVDC program. For prelaunch checkout, TM calibration is controlled by the electrical support equipment in the control center.

Two units and special circuitry in other units provide TM calibration. The two units are the TM Calibrator (Mod II) (calibrator) and the TM Calibrator Control Unit (controller). Special circuits to accept calibration inputs are located in analog multiplexers, telemeter oscillator assemblies, and single sideband telemeters that are to be calibrated.

The calibrator and controller function together to furnish and control the calibration inputs to the telemetry components. The calibrator selects the calibration signal level and selects the component to be calibrated. The controller furnishes regulated power to the calibrator and also serves as an interface unit to route and isolate all signals to and from the calibrator.

The calibrator-controller assembly furnishes 6 outputs for calibration of analog multiplexers or telemeter oscillator assemblies and 3 outputs to calibrate single sideband telemeters. Each of the units to be calibrated contain circuitry to accept the calibration command and to apply the calibrated signals to their individual data channels. While up to 9 units can be calibrated by the calibrator-controller assembly, the full capability may not be used. For clarity of explanation, this description of subsystem operation assumes that full capability is used.

To increase system flexibility, all inputs and outputs of the calibrator-controller assembly are routed through a Measuring Distributor. This allows the inputs and outputs to be patched to selected telemetry equipment without modification to launch vehicle wiring.

The functions of the subsystem are greatly expanded during prelaunch checkout. Any of several preflight calibrations may be selected in addition to the normal inflight calibration.

GENERAL SUBSYSTEM FUNCTION

The subsystem is operated in either the inflight mode or the prelaunch mode. During inflight mode, the telemetry equipment is calibrated by preset signals in a preset sequence when commanded to do so by the LVDC program. During prelaunch mode, the LVDC command may be simulated and variable calibration signals may be furnished to the telemetry equipment.

Inflight Mode. During flight, upon receiving a single 28 Vdc pulse command from the LVDC, the calibrator-controller assembly will:

- Furnish six 28 Vdc commands that can be used to enable oscillator assemblies to receive calibration signals or initiate a calibration sequence in an analog multiplexer.
- Furnish one 0 to 5 Vdc calibration signal (in 1.25-volt steps) to be sent to the oscillator assemblies being calibrated.
- Furnish three 28 Vdc commands that can be used to enable single sideband telemeters to receive calibration signals.
- Furnish three 1700-hertz calibration signals to be sent to the single sideband telemeters being calibrated.

The subsystem uses 28 Vdc from the vehicle power supply and 5 Vdc from the 5 Volt Measuring Voltage Supply. The 5 Vdc is used for the precise 0 to 5 Vdc calibration signal sent to the oscillator assemblies. The 28 Vdc is regulated by the controller and used for operating power for the calibrator and the 28 Vdc enable signals sent to calibrate the oscillator assemblies, multiplexers, and single sideband telemeters.

The inflight calibration start command originates in the LVDC (see Figure 5. 6-1) and is routed through the Switch Selector to the calibrator-controller assembly.

The clock starts a voltage divider and stepper circuit which produces a precise 0 to 5 Vdc, stepped-voltage output. This sequentially stepped output goes from 0. 00 to 1. 25 to 2. 50 to 3. 75 to 5. 00 and back to 0. 00 in a period of 700 ± 25 milliseconds. The stepped voltage runs through 6 sequences and is fed to the calibration bus for distribution to oscillator assemblies. Each time the stepped voltage finishes a sequence, the output selector circuit advances to select the next oscillator assembly or multiplexer to be calibrated.

When an oscillator assembly is selected for calibration, the 28 Vdc signal from the calibrator-controller assembly energizes a relay circuit in the oscillator assembly. This relay inhibits the normal measurement data for 700 milliseconds and substitutes the stepped calibration voltage present at the calibration bus. When another unit is selected for calibration, the relay returns to its original position and normal measurement data is once more allowed to flow to the oscillator channels.

When a multiplexer is selected for calibration, the 28 Vdc signal from the output selector starts an automatic circuit in the multiplexer. This automatic circuit inhibits the normal measurement data input and substitutes an internally generated, stepped 0 to 5 volt signal like the signal generated by the calibrator-controller assembly. When a multiplexer receives the calibrate command, the calibration sequence is delayed until the start of the next multiplexer master frame. Each voltage step is held for one master frame. This requires five master frames or approximately 400 milliseconds for a complete calibration sequence. The multiplexer then returns the normal measurement data to its data channels.

While the multiplexers and oscillator assemblies are being calibrated, the calibrator-controller assembly also selects and calibrates three single sideband telemeters. The calibrator-controller assembly produces a 1700-hertz, 1-volt peak-to-peak calibration signal. The single sideband telemeters are selected and calibrated with the 1700-hertz signal similar to the method used for the selection and calibration of the oscillator assemblies. A calibration sequence for a single sideband telemeter lasts the time necessary for 2 multiplexers or oscillator assemblies to be calibrated; that is, 1400 ± 50 milliseconds. Normal measurement data is then allowed to return to the data channels of the single sideband telemeter.

Prelaunch Mode. During prelaunch mode, while being controlled from the control centers the subsystem can:

- Simulate the inflight calibration start command from the LVDC.
- Transfer the calibration bus to ESE control and supply an ESE supplied calibration signal.
- Select all three single sideband telemeters for calibration and supply an ESE generated calibration signal.
- Connect the data input of all oscillator assemblies to the calibration bus.
- Control the output of the calibrator-controller assembly to allow any step of the 0 to 5 Vdc calibration signal to be applied to the calibration bus.

The subsystem uses the same 28 Vdc and 5 Vdc power used in the inflight mode. During prelaunch mode, the 28 Vdc may be switched OFF, thus turning OFF the subsystem.

An inflight calibration start command simulation signal may be originated by the ESE. This signal is fed to an OR circuit in the calibrator-controller assembly and starts the same calibration sequence that is started by the inflight calibration start command from the LVDC.

The calibrator-controller assembly's signal to the calibration bus may be switched out and substituted by an input from the ESE. This input is generally a 100-hertz signal with the primary purpose of calibrating the oscillator assembly channels that carry frequency-intelligent measurement data.

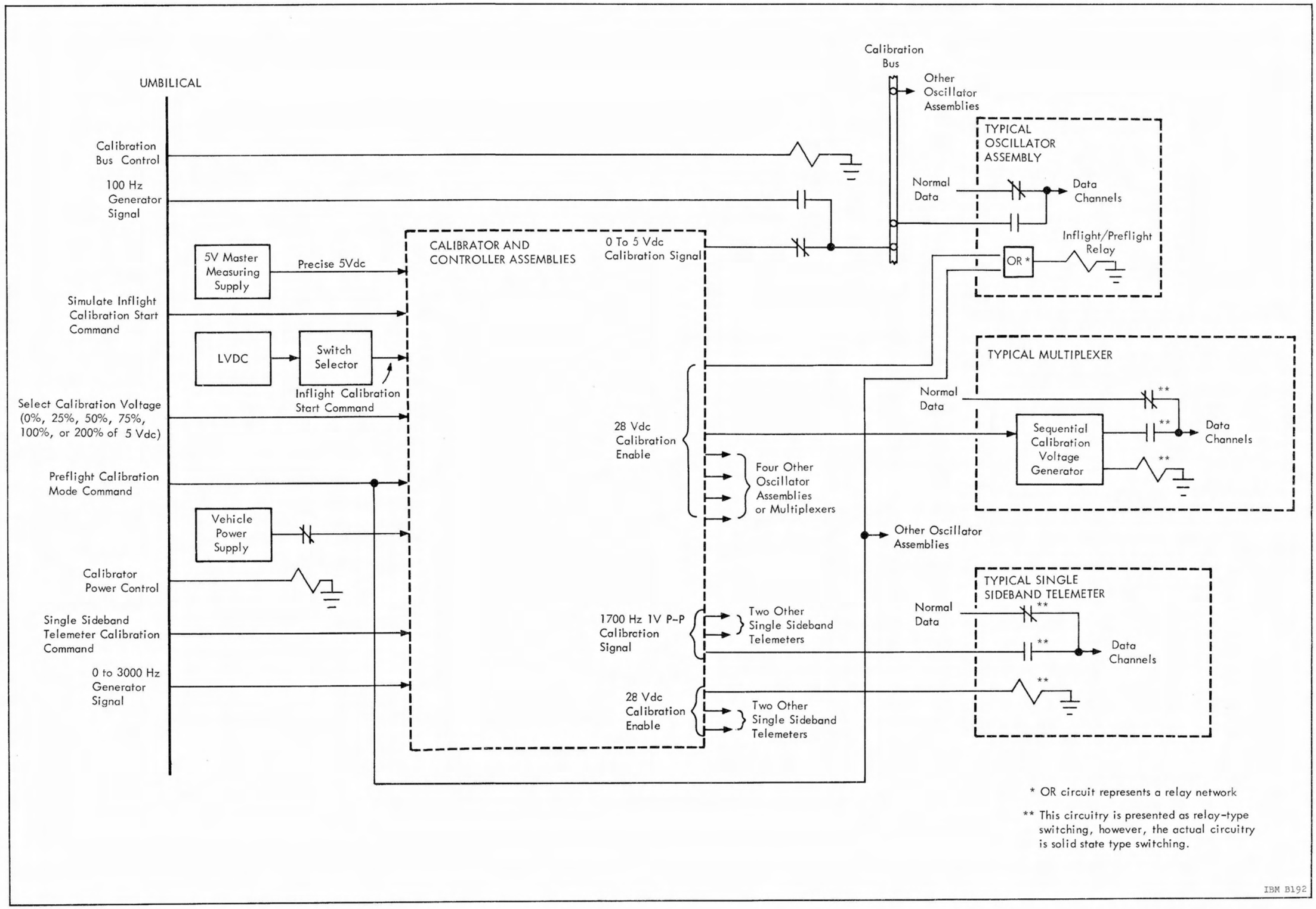


Figure 5.6-1 Typical Telemetry Calibration Subsystem

A command from the ESE can cause all three single sideband telemeters to be switched to the calibration bus in the calibrator-controller assembly. A 0 to 3000-hertz calibration signal is then applied to the bus from the ESE.

Application of a preflight calibration mode command causes the data inputs of all oscillator assemblies to be switched to the calibration bus. This command also allows the 0 to 5 Vdc calibration voltage from the calibrator-controller assembly to be completely controlled from the ESE.

After the preflight calibration mode command has been sent, the 0 to 5 Vdc output is under the complete control of the ESE. The ESE may select any of six possible signals to be supplied by the calibrator-controller assembly to the calibration bus. Any of the five voltage steps or a continually stepping voltage may be selected. Each of these 6 signals may be applied to the calibration bus for as long as desired.

CALIBRATOR-CONTROLLER ASSEMBLY FUNCTION

The calibrator-controller assembly contains three main functional circuits (see Figure 5.6-2). Although the 3 circuits are interdependent, they have separate outputs. The output selection circuit selects the component to be calibrated and sends a 28 Vdc calibrate enable signal to that component. The voltage stepper circuit generates and selects the calibration voltage to be sent to the oscillator assemblies. The single sideband telemeter calibration circuit generates the inflight calibration signal and selects whether this signal or an ESE generated signal will be applied to the single sideband telemeters.

A start calibration sequence is initiated by a 28 Vdc pulse from the LVDC through K2 or from the ESE through K1. The start command causes the first components subject to calibration to be selected and enables the rest of the components to be selected sequentially each time the calibration voltage completes a stepped sequence.

At any given instant, the only possible output of the unity gain amplifier to the oscillator assembly calibration bus is 1 of the 5 "steps" of calibration signal (0.00 Vdc, 1.25 Vdc, 2.50 Vdc, 3.75 Vdc, or 5.00 Vdc). A feedback from the unity gain amplifier output is fed to the voltage comparator where the feedback is compared to the voltage comparator's input command. If the voltages are the same, nothing happens. If the voltages are different, the comparator causes the output of the unity gain amplifier to change "steps" until it matches the comparator's input command. If the input command exceeds 5 Vdc, (200 percent input), the circuit will continuously step through the five possible levels since it cannot match the input command. During the inflight mode, 28 Vdc is constantly applied to the input of the voltage comparator through K3, causing a continuously stepping voltage. One complete stepping sequence is 700 milliseconds long.

A 1700-hertz calibration signal is constantly generated by the calibrator. Each time any signal sideband telemeter is selected for calibration, this 1700-hertz signal is furnished to all single sideband telemeters through the contacts of K5. During prelaunch mode all three single sideband telemeters may be simultaneously selected for calibration through K4. If this is done, a 0 to 3000-hertz calibration signal is furnished to the calibrator for distribution to the single sideband telemeters.

Output Selection Circuit Function. A start calibration command enables the output relay drivers and sets the control flip flop. The control flip flop advances the 7-point sequencer generator to step 1, enables the 7-point sequencer generator input gate to accept signals from the 5-point sequencer generator, and enables the clock input gate in the 5-point sequencer generator. In step 1, the 7-point sequencer generator causes the relay matrix and gate to issue calibrate command 1 through the enabled relay driver. This supplies a calibrate enable command to one oscillator assembly or multiplexer and one single sideband telemeter. Each time the voltage stepper circuit completes a 0 to 5 Vdc sequence, it sends a signal through the 7-point sequencer generator input gate to advance the sequencer generator input gate to select the next calibrate command to be issued.

Voltage Stepper Circuit Function. If the comparator is commanded to change the output voltage, it detects the difference between its input command level and the voltage output of the unity gain amplifier. If there is a difference, the comparator sends a signal to enable the 5-point sequence generator gate, another signal to enable the clock input gate, and another signal through the conditioning stage to advance the 5-point sequence generator to the first step. With the clock input gate enabled, the clock issues pulses at 140-millisecond intervals. Each clock pulse advances the 5-point sequence generator to select the next voltage level. Each time the 5-point sequence generator passes the 5-volt level, it commands the 7-point sequence generator is issue the next calibration command. The 5-point sequence generator sends

a command through the calibration matrix to the signal divider to produce the desired 0 to 5-volt level. The signal divider uses the precise 5 Vdc from the 5 Volt Measuring Voltage Supply as a supply voltage to be divided as necessary. The output is fed through the unity gain amplifier to the oscillator assembly calibrate bus. This output is also fed back to the comparator, and as long as the output does not equal the commanded voltage, the comparator will cause the circuit to continue stepping through the 0 to 5 Vdc range.

Single Sideband Telemeter Calibration Circuit Function. A 1700-hertz, 1-volt peak-to-peak calibration signal is constantly generated by an oscillator circuit and furnished to the normally open contacts of K5. Whenever the output selection circuit selects a single sideband telemeter for calibration, K5 is closed allowing the calibration voltage to be applied to all three single sideband telemeters. During prelaunch mode, the ESE can select all three single sideband telemeters for calibration without using the output selection circuit. When this is done, a 0 to 3000-hertz calibration signal may be furnished from the ESE to calibrate the single sideband telemeters.

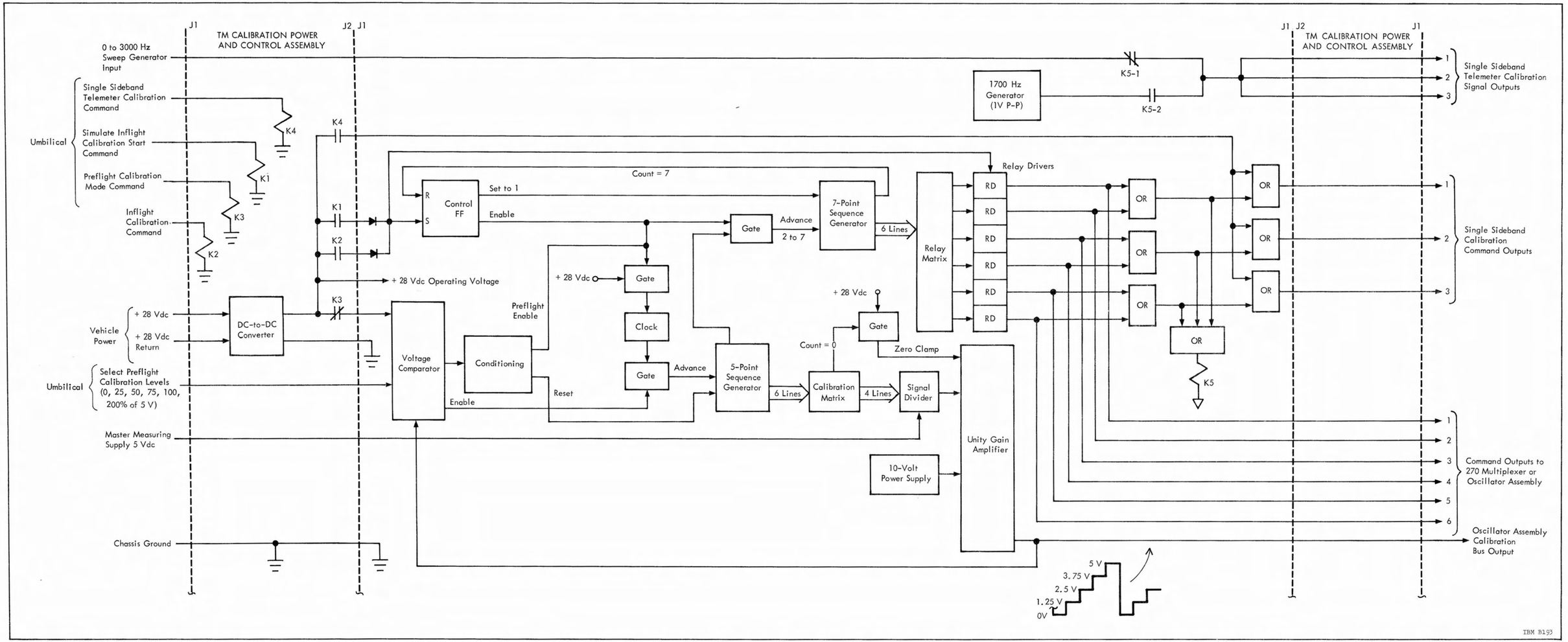


Figure 5.6-2 Telemetry Calibrator Assembly

SECTION 5.7

DIGITAL DATA ACQUISTION SYSTEM

DDAS is a function associated with Saturn V PCM telemetry and is utilized in both preflight and flight phases.

During preflight checkout, the telemetry system presents digital data over coaxial cables to one or more locations remote from the vehicle. These measurements are available to digital computers in real time through a special data-receiving facility interfaced with the computers. The data-receiving facility also provides outputs for display of selected channels in either digital or analog form for visually determining the status and readiness of vehicle subsystems and tape records the DDAS inputs for analysis at a later time.

During the launch, earth orbiting, and lunar-injection phases, there are times when information processed by the LVDC is desired at the ground station. Also, during periods when specific commands are being given through the IU command system to the LVDC, it will be necessary to transmit to ground the particular command prior to processing by the LVDC. Since the information to be telemetered is dependent on particular missions and has a random characteristic, provision will be made in the telemetry to accommodate these outputs. Specific PCM telemetry system channels are assigned to accommodate the LVDA 40-bit outputs. The assigned channels are sampled at a rate of 240 times per second.

The LVDA identifies valid data by the presence of a validity bit which has no significance to the telemetry but is transmitted as part of the data telemetered to the ground. The ground computer automatically determines the existence of valid data by recognizing the validity bit in a data word. The validity bit is present with the valid data for at least 4.5 milliseconds to ensure at least one transmission of the valid data.

During flight, the DDAS function is performed between the telemetry system, LVDA, and LVDC. Upon request, data in digital form is made available to the LVDC during flight and is used by the LVDC to perform vehicle checkout.

The telemetry system in the S-IVB/IU functions during launch, earth orbit, and lunar-injection phase of the mission. During these phases, periodic checks are required of the vehicle's performance or operating status. This is accomplished by inserting specific segments of the telemetered information into the computer.

During orbital checkout, which is initiated by a command signal to the LVDC via the IU command, the LVDC requires a real-time value of measurements, which are part of the total measurements being telemetered by the S-IVB/IU Stage telemetry system.

Selective transfer of measurement values from the S-IVB/IU Stage telemetry systems to the LVDA is accomplished through the DDAS/Computer Interface Assembly. This assembly contains the timing and comparison logic necessary to separate the selected channel from the IU PCM/DDAS format. A time division multiplexer, located in the S-IVB Stage, transfers S-IVB measurements needed for checkout and mission control to the IU PCM/DDAS Assembly.

The LVDA signifies the specific data channel to be transferred by means of a 12-bit channel address. Upon receipt of a "data-request" signal from the LVDA, the DDAS/Computer Interface Assembly initiates a transfer sequence which consists of:

- Awaiting the next appearance of the signified channel in the PCM/DDAS format
- Writing the data sample into a 10-bit holding register within the assembly
- Providing a "data-ready" signal to the LVDA indicating that the selected data is available

So long as the "data-request" signal remains at the request level, subsequent samples of the selected channels are transferred into the holding register as they appear in the format of the PCM/DDAS Assembly. When the LVDA returns the "data-request" signal to the standby level, the last value transferred remains in the holding register until another transfer sequence is initiated.

When the LVDA receives the "data-ready" signal, it branches to a sub-routine which operates to transfer the data from the telemetry output register to the LVDA. Synchronization between the telemetry system and the LVDA is accomplished in the following manner: Each time the telemetry receives an address from the LVDA, followed by a valid "data-request" signal, it recognizes this input as the initiation of a new data-seeking cycle as well as a signal to read in the data. Upon this recognition by telemetry, it first resets its output data register and then begins seeking the data requested by the LVDA. The LVDA and LVDC ensures that a new address with a valid read bit is not generated until data from the telemetry output register has been received in response to the previous address.

5.7.1 DDAS/ COMPUTER INTERFACE UNIT

A System interconnection diagram for the DDAS/Computer Interface Unit is illustrated in Figure 5. 7-1. Figure 5. 7-2 is a block diagram showing logic and circuit arrangements for the DDAS/Computer Interface Unit. Positive true logic levels and positive circuit triggering is assumed.

The buffer and dc isolation circuits provide the required input impedance to data and synchronizing signals from the PCM/DDAS. The circuits also contain magnetic coupling elements which provide isolation between the circuits of the PCM/DDAS and other circuits within the assembly. It should be noted that dc isolation is not required between the LVDA and the assembly logic circuits.

The timing and resetting logic circuits derive the common reset for the counter array and a clock of the correct phase for transfer of data into the holding register from the synchronization signals.

The counter array consists of three binary counters (A, B, and C) each having an internal reset which provides a recycle each 30, 10, and 3 counts, respectively. Each counter is also reset to a count of 1 by the common reset from the timing and resetting logic.

Counter A consists of 5 flip flops, arranged to provide a divide-by-thirty binary counter. Its input consists of the restored 3600 pps synchronization input to the assembly. At the end of count period 30, counter B is internally reset to a count of 1. The internal reset of counter A is also provided as an input to counters B and C.

Counter B consists of 4 flip flops configured as a divide-by-ten binary counter. Its input is triggered 120 times per second by the internal reset of counter A. At the end of count period 10, counter B is internally reset to a count of 1.

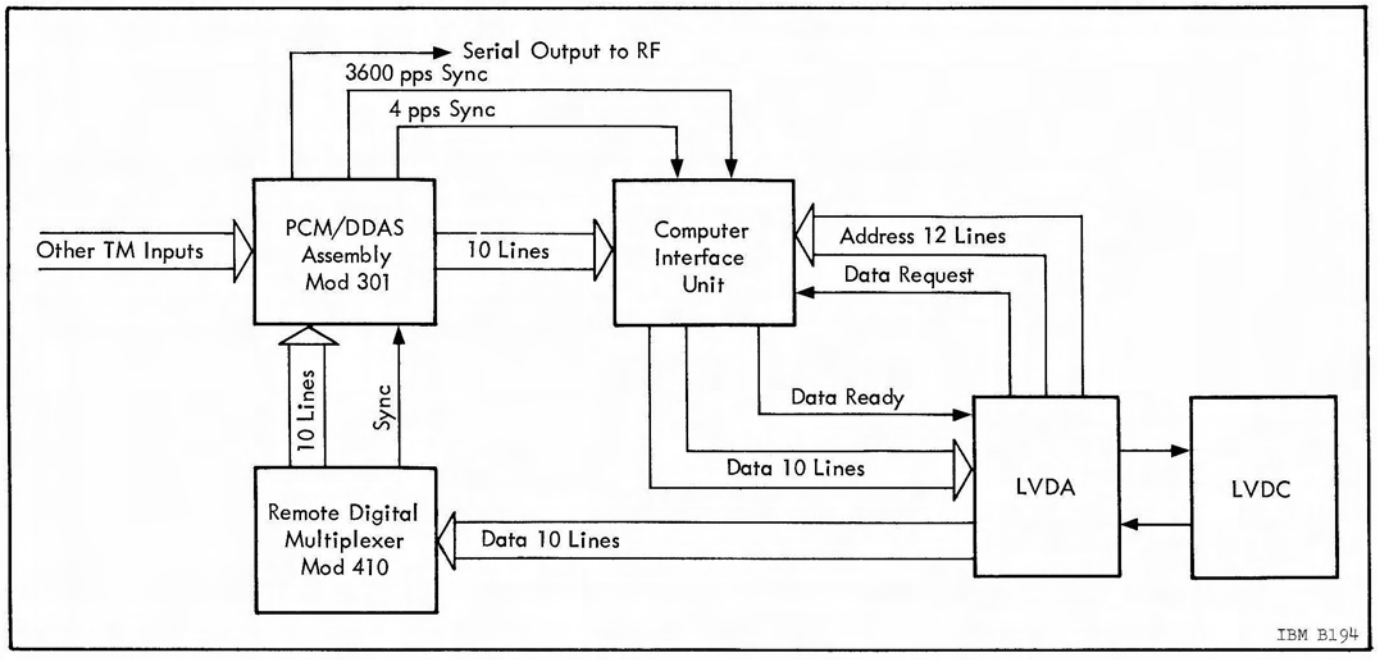


Figure 5. 7-1 Computer Interface Unit - System Interconnection Diagram

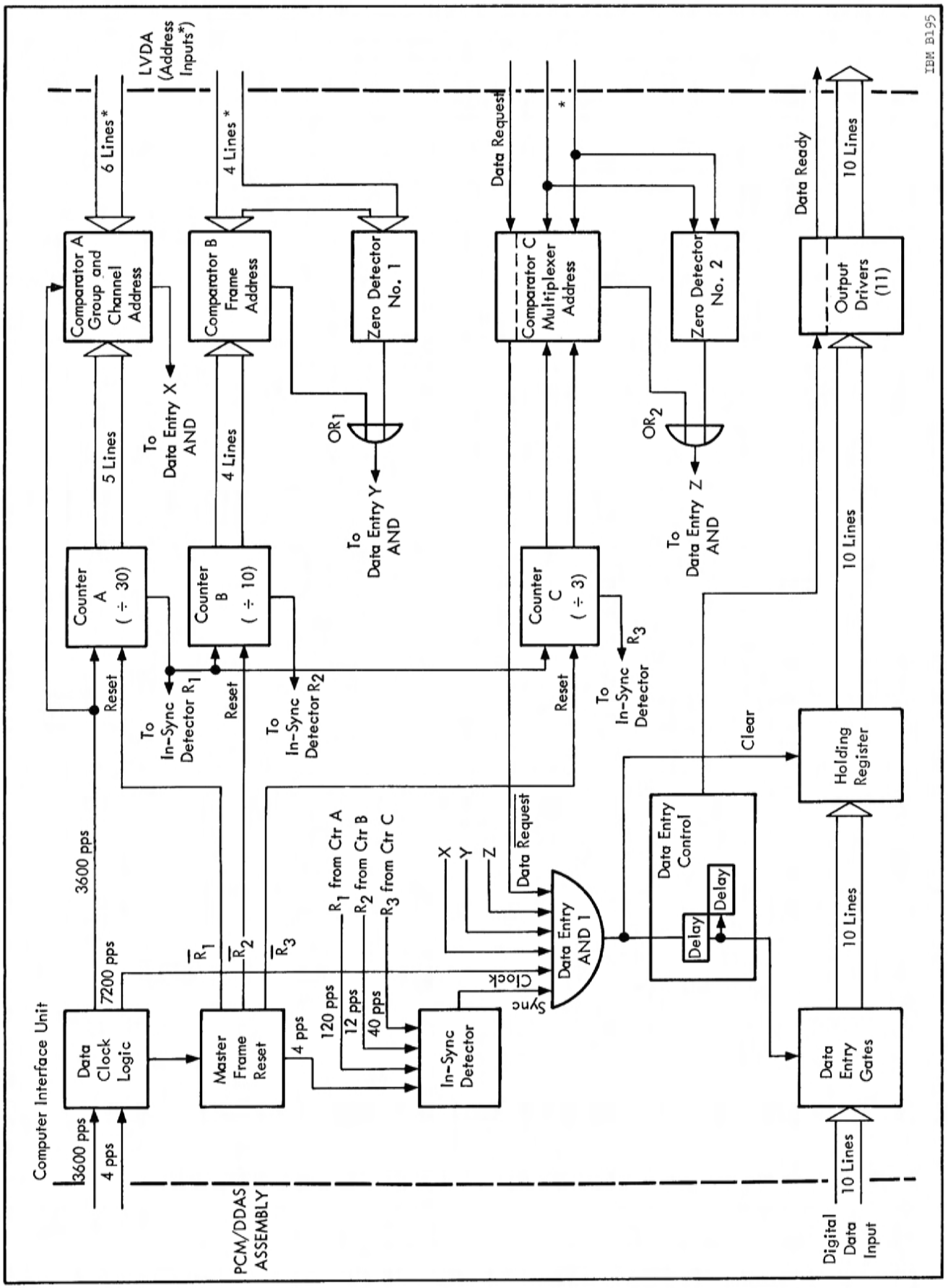


Figure 5.7-2 Computer Interface Unit Block Diagram

Counter C consists of 2 flip flops configured as a divide-by-three binary counter. Its input is triggered at 120 times per second by the internal reset of counter A. At the end of count period three, counter C is internally reset to a count of 1.

The twelve address lines from the LVDA are first buffered, and logic levels are transposed to the internal logic levels of the assembly. They are then compared to the states of the counter array by three comparators and two zero detectors.

Comparator A compares address bit 1 with waveform b, and address bits 2 through 6 with the states of flip flops one through five, respectively, of counter A.

If address bits 7 through 10 are all in the zero state, zero detector No. 1 provides an output which is combined in the OR gate OR_1 with the output of comparator B. Hence OR_1 provides a true output for either an in-register, or all zeros condition of the four address bits.

Comparator C compares address bits 11 and 12 with flip flops one and two, respectively, of counter C.

If address bits 11 and 12 are both in the zero state, zero detector No. 2 provides an output which is combined in OR gate OR_2 with the output of comparator C. Hence OR_2 provides a true output for either an in-register, or all-zeros condition of address bits 11 and 12.

The zero detector provides a means by which the address bits may instruct that the status of either (or both) counter B and C be disregarded. This will provide access to the various sampling rates of the PCM/DDAS. The outputs of comparator A, OR_1, and OR_2 are applied to the data entry AND gate (AND_1). The in-sync detector provides a check of the correct synchronization state of the counters and prevents a transfer of data from occurring when the assembly timing is not synchronized with the PCM/DDAS. The output of the in-sync detector is then applied to AND_1 as a synchronization pulse.

The data request signal (after buffering and logic level transposition) is also applied as a true logic level to AND_1. If the in-sync detector output to AND_1 is true, the next "comparison true" signal then activates AND_1 and a clock pulse passes through to clear the holding register. After a delay of a few microseconds, the data inputs are gated into the holding register. The gating pulse also triggers the monostable multivibrator, which provides a "data ready" signal to the LVDA.

SECTION 5.8

TELEVISION SYSTEM (SATURN V)

The Saturn V Launch Vehicle television system will be used to provide both real-time and permanent visual data on the performance of certain vehicle functions. No television will be used with Saturn IB Vehicles.

A block diagram of the vehicle and ground equipment is illustrated in Figures 5.8-1 and 5.8-2. Table 5.8-1 lists the television system characteristics.

Figure 5.8-1 illustrates the path of the video signal from the camera, through the video register, to the transmitter. A description of the circuitry follows:

The television cameras are small, having an outside diameter of 7 centimeters (1.75 inches) and a length of 35 centimeters (13.75 inches). The Saturn V television system will include two such cameras.

The video register unit is a sync generator and video multiplexing unit. This unit is capable of driving up to 4 cameras, accepting the video outputs of each, and multiplexing the output at either a field, frame, or 2-frame rate. The Saturn V system will be multiplexed at a 2-frame rate.

Since there are actually 4 areas to be viewed in the engine compartment and only 2 cameras, a

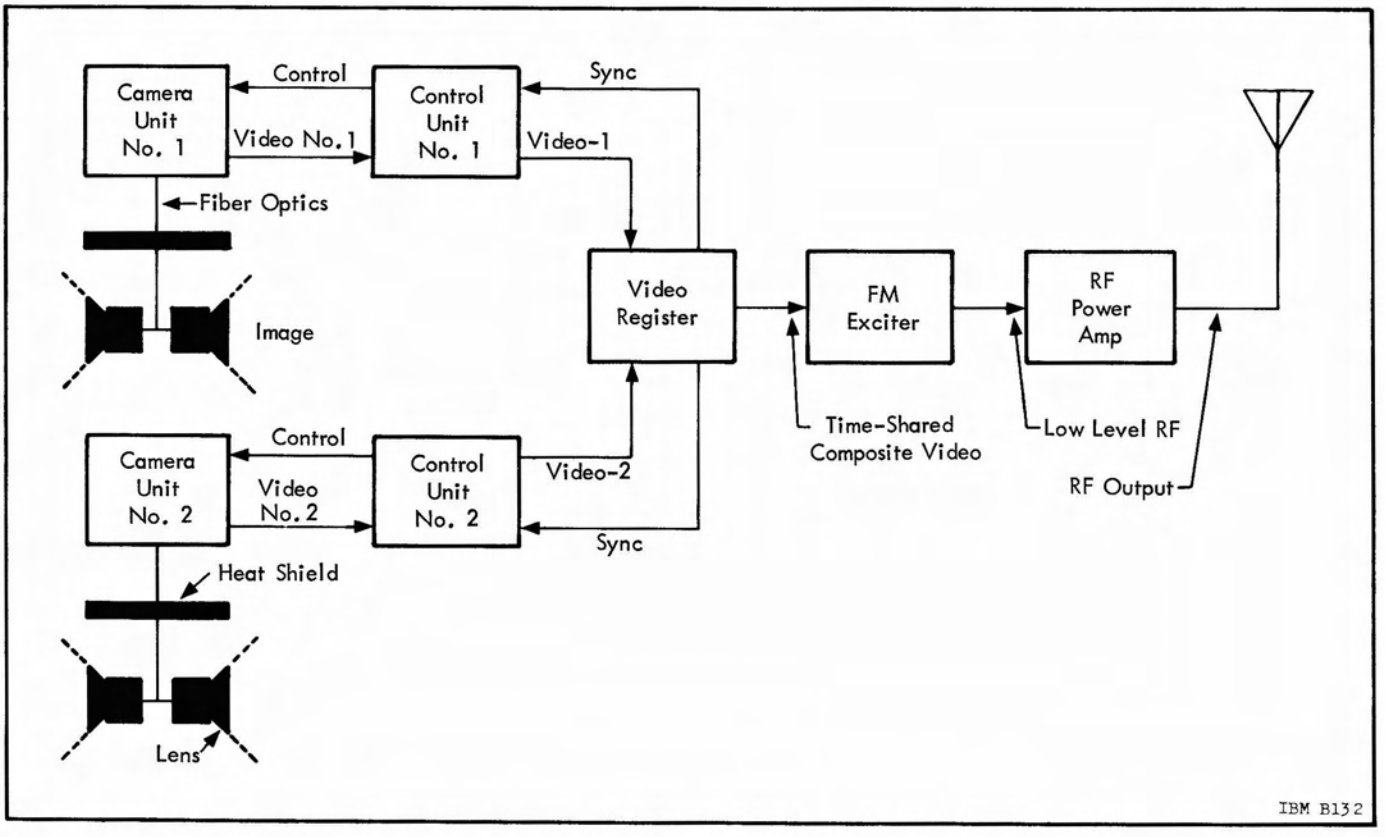


Figure 5.8-1 S-IC Television Function Block Diagram

split fiber optic bundle is used on each camera. Each bundle is split at the lens end and uses two objective lenses. The view covered is shown in Figure 5.8-3.

The output of the video register unit is fed to the transmitter, which is an FM system.

The ground system shown in Figure 5.8-2 provides 2 units for recording the demodulated signal as it is received and a system for real-time viewing.

The systems used for recording the video are one broadcast-type video recorder and one kinescope recorder. Video recorded on both of these systems is still in a multiplexed sequence. For real-time viewing, special equipment is required (i.e., sequence decoder and television viewing unit).

The function of the sequence decoder is to demultiplex the video signal and feed the output of each camera to the same monitor. If the sequence decoder were used alone, the video being fed to each monitor would be composed of 2 frames of video followed by 2 blank frames.

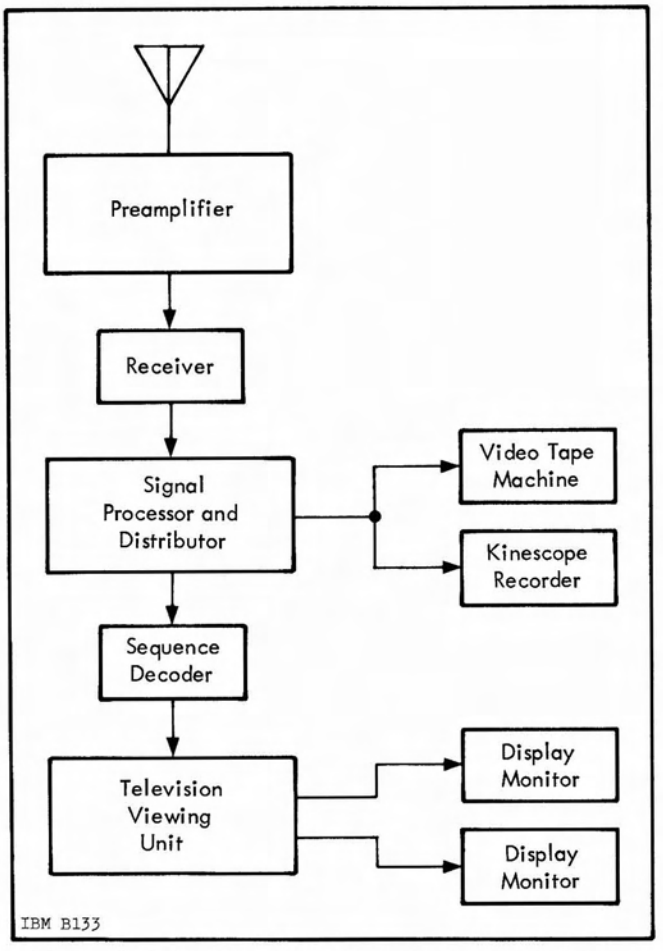


Figure 5.8-2 Television Ground Receiving Station

To eliminate the "blinking" picture caused by the above signal, the television viewing unit is provided. This unit uses a storage system and command signals from the sequence decoder to fill the blank 2-frame time with video information from the previous frame. This gives a steady picture. The picture information rate, however, would be at 7-1/2 frames per second. Although the picture appears steady, motion would be jerky.

Table 5.8-1 Saturn V Launch Vehicle Television Characteristics

Transmitter	
Video bandwidth	8 MHz
Modulation	FM
Deviation	10 MHz (for complete video
Output power	2.5 watts (minimum)
Unmodulated frequency	1705 MHz ± 0.20%
Video resolution (horizonal) of received picture	500 lines
Closed Circuit Camera System	
Camera light sensitivity	10.76 lumens/meter^2 (1.0 foot candle)
Video bandwidth	8 MHz
Frame rate	39/second
Scanning	2:1 Interlace
Specifications of Television Ground Station for Support of Saturn Television Systems	
Parametric amplifier	
Gain	20 db (minimum)
Noise figure	1.35 db
Frequency range	1700 to 1720 MHz
Receiver	
Frequency range	1700 to 1720 MHz
Gain	90 db (minimum)
Noise figures	12 db (maximum)

Table 5.8-1 Saturn V Launch Vehicle Television Characteristics (Cont)

Signal Processing and Distributing Amplifier	
Video bandwidth	8 MHz
Number of outputs	4
Sequence Decoder	
Video bandwidth each output	8 MHz
Number of outputs selectable	1 to 16
Switching time	0.1 us
Video Tape Recorder	
Video bandwidth	5.5 MHz
Tape speed	38 cm/s (15 in./s)
Recorder time	96 minutes

Table 5.8-1 Saturn V Launch Vehicle Television Characteristics (Cont)

Kinescope Recorder	
Camera frame rate	30/second
Film capacity	365.8 meters/minute (1200 feet/minute)
Viewing Monitor	
Video bandwidth	8 MHz
Video resolution (horizontal)	600 lines

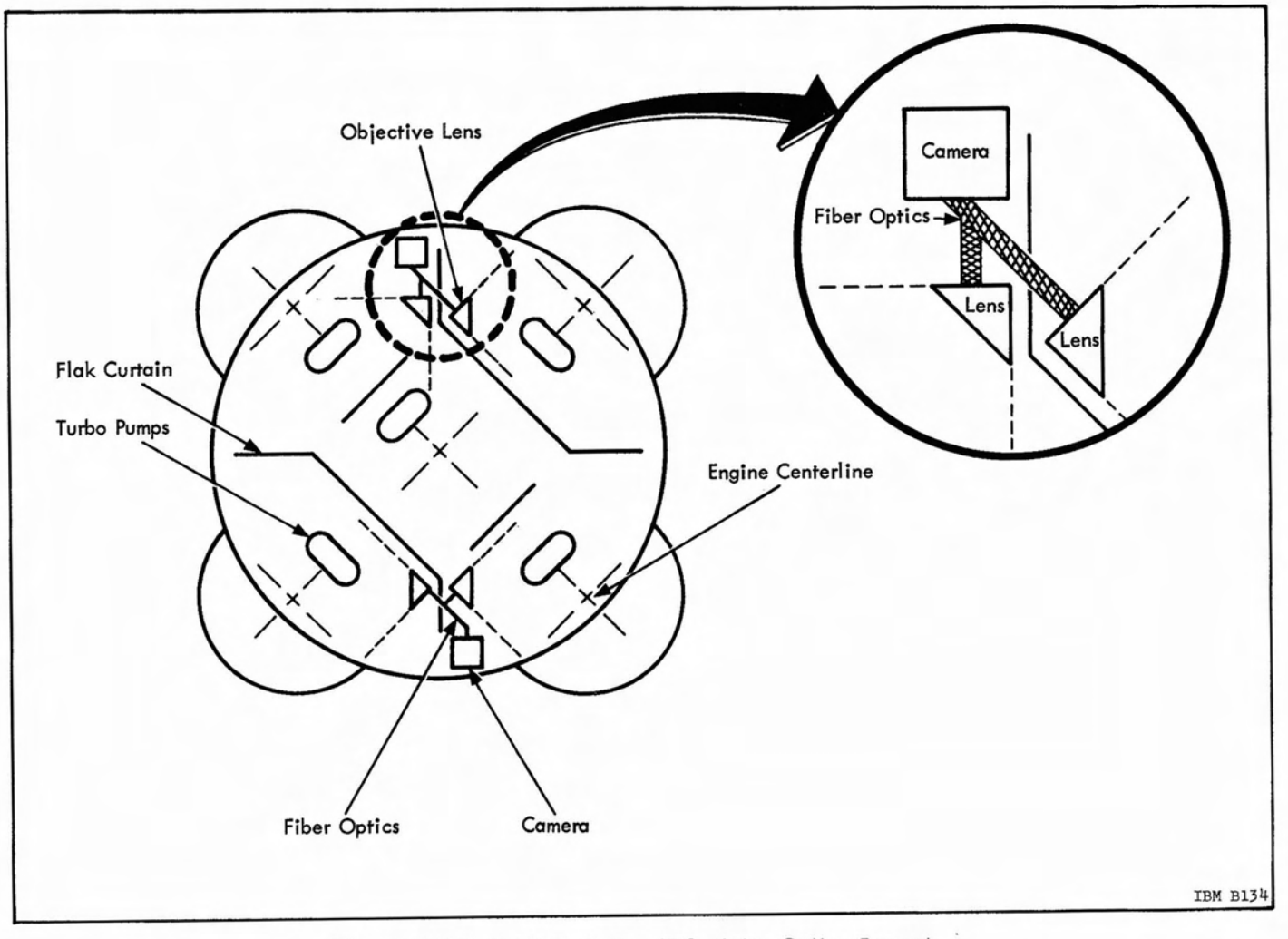


Figure 5.8-3 S-IC Tentative Television Optics Layout

CHAPTER 6

RADIO COMMAND SYSTEMS

TABLE OF CONTENTS

SECTION 6.1

INTRODUCTION

The Saturn Vehicles carry two different types of radio command systems; for range safety and for data transmission to the Instrument Unit.

The Instrument Unit command system provides digital data transmission from ground stations to the Astrionics System in the S-IVB/IU Stage. This system will be used to up-date guidance information or command certain functions in the S-IVB/IU Stage. The Instrument Unit command system will not be used during powered flight phases.

The range safety command system provides a means to terminate the flight of the vehicle by radio command from the ground in case of emergency situations in accordance with range safety requirements. Each powered stage of the vehicle is equipped with two command receivers/decoders and the necessary antennas to provide omni-directional receiving characteristics (range safety requirements). The command destruct system in each stage must be completely separate and independent of those in other stages. In case of vehicle malfunctions which cause trajectory deviations larger than specified limits, the vehicle will be destroyed by the range safety officer by means of the range safety command system. The range safety system is active until the vehicle has achieved orbit. After successful insertion into earth orbit, the destruct system is deactivated (safed) by command from the ground. The early Saturn IB and V Vehicles will be equipped with a tone command system (AN/DRW-13) which will be replaced in later vehicles by a secure range safety command system.

SECTION 6.2

INSTRUMENT UNIT COMMAND SYSTEM

6.2.1 GENERAL SCHEME

The Saturn Instrument Unit command system is used to transmit digital information from ground stations to the Launch Vehicle Digital Computer in the Instrument Unit.

Figure 6.2-1 shows a block diagram of the overall command system for Saturn V. The command message is transmitted in the S-band using a carrier frequency of 2101.8 MHz. The command message is modulated on a 70 kHz subcarrier, which in turn is modulated on the 2101.8 MHz carrier. The signal from the ground station is received through the S-band transponder of the Saturn communication and command system in the IU. The receiver separates the transmitted message from the carrier and feeds the resulting signal to the IU Command Decoder where decoding is accomplished. From the decoder, the command message is sent through the LVDA to the LVDC. Verification of the message received is achieved by transmitting a signal over the IU-PCM telemetry system back to the ground station.

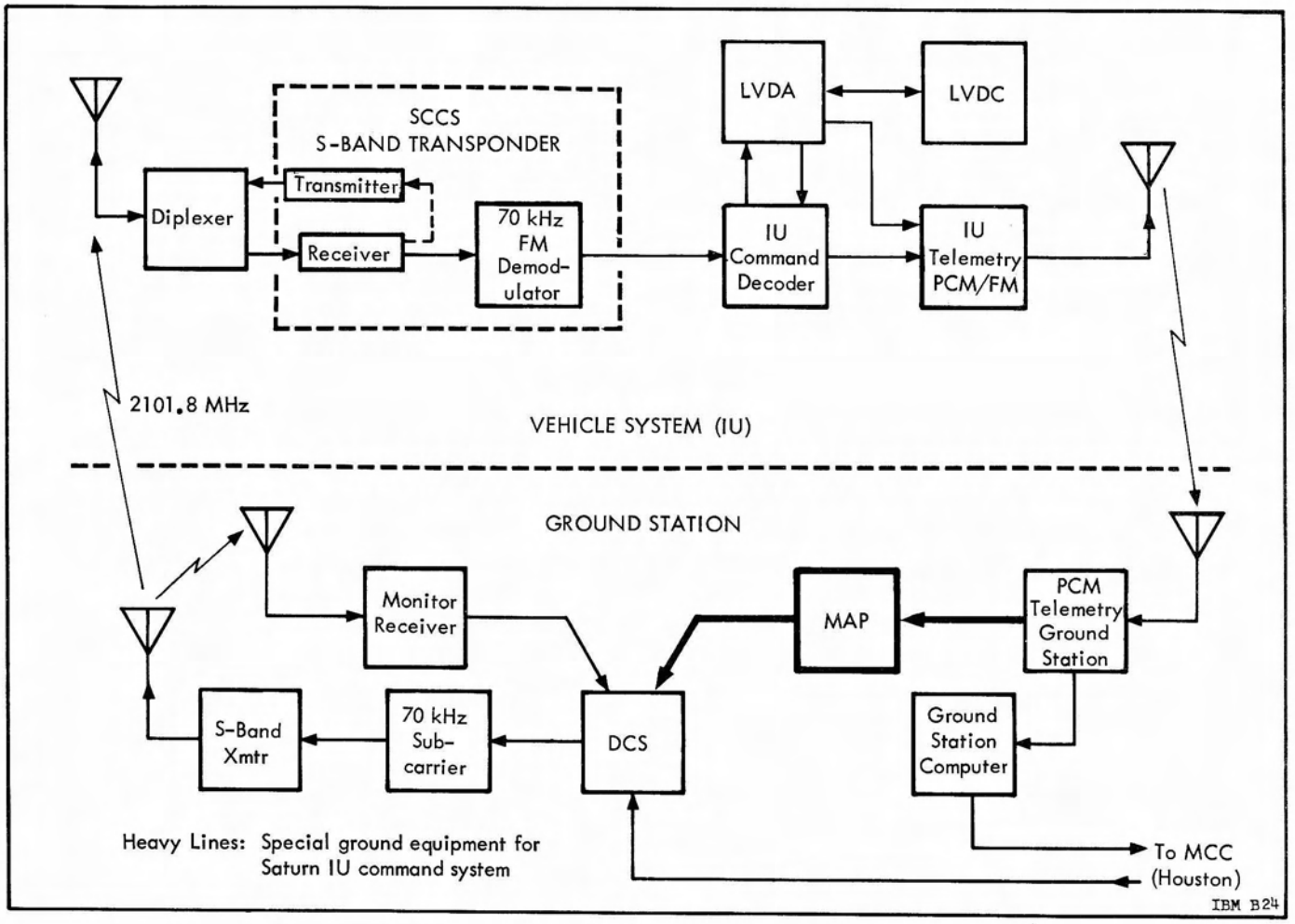


Figure 6.2-1 Saturn V IU Command System

For the flights of the Saturn IB Vehicles, the ground network will not be equipped for S-band operation. Therefore, the IU command system of Saturn IB uses a frequency-modulated carrier at 450 MHz. The IU carries the MCR-503 Receiver for reception of the command signal. The same type of receiver is used also for the secure range safety command system. A block diagram of the Saturn IB IU command system is illustrated in Figure 6.2-2. The functional scheme of the Saturn IB and the Saturn V IU command system is identical, except for the carrier frequency and subcarrier.

The Saturn IU command system is closely related to the Apollo Spacecraft up-data link. Both systems use essentially the same ground station equipment of the manned space-flight network. The Saturn IU command system is designed to assure a high probability that the LVDC receives the correct message.

The commands and data to be transmitted to the vehicle will originate in the Mission Control Center in Houston, Texas, and are sent to the remote stations of the Manned Space Flight Network where they are transmitted to the vehicle.

6.2.2 MODULATION TECHNIQUES

The ground modulator used with the IU command system is the same as the one used on the Gemini Program and for the Apollo Spacecraft up-data link. This PSK modulator is part of the digital command system console, which serves as the encoder for several different space programs.

The DSC, or data processing equipment, utilizes phase-shift keyed baseband modulation. A stable 1 kHz tone is generated in the modulator and used as a synchronizing or "clock" signal. A coherend 2 kHz tone is then biphase modulated so that the binary digits are phase analogous. The 2 kHz tone is modulated at a 1 kHz rate. (A binary "one" is being transmitted when the 2 kHz tone is in phase with the 1 kHz reference at a time when the 1 kHz waveform is crossing zero and has a positive slope.

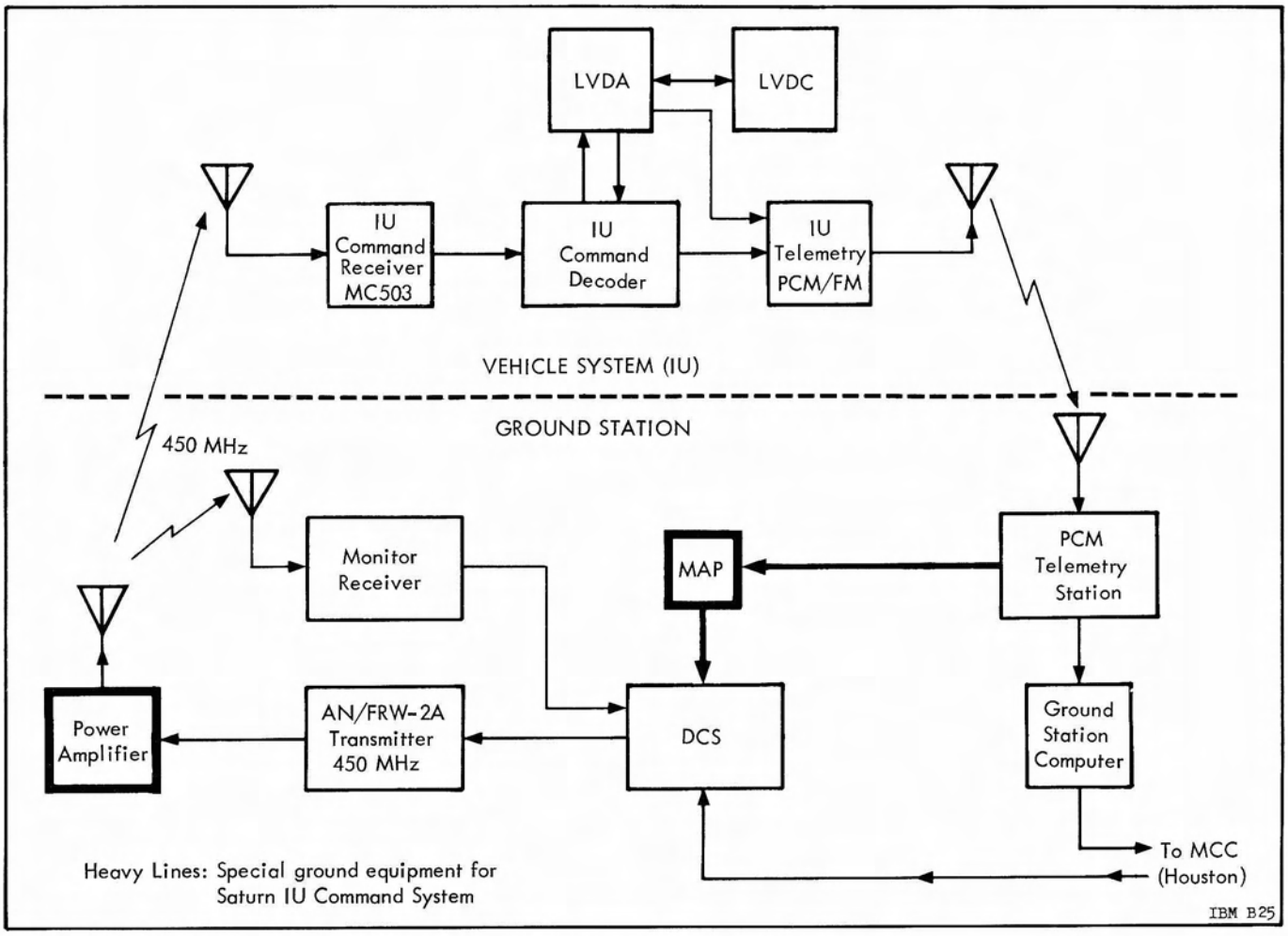


Figure 6.2-2 Saturn IB IU Command System

See A of Figure 6.2-3). The 1 kHz tone and the phase modulated 2 kHz tone are algebraically summed to produce the composite waveform shown in B of Figure 6.2-3. This composite waveform then modulates an RF carrier for transmission to the vehicle. In the Saturn IB IU command system, the 450 MHz RF carrier will be frequency modulated ±60 kHz. In the Saturn V IU command system, the composite baseband waveform will frequency modulate an intermediate carrier (subcarrier) of 70 kHz, which will in turn phase modulate the 2101.8 MHz S-band carrier. The former modulation scheme is referred to as PSK/FM (at 450 MHz), and the latter is called PSK/FM/PM (at 2101.8 MHz).

6.2.3 COMMAND WORD FORMAT

The command word in the IU command system is composed of 35 information bits which are used as follows:

- Three bits for vehicle address
- Fourteen bits for decoder address
- Five bits of control information —
  - One computer mode command bit
  - Two bits for computer "sync" signal
  - Two bits for "interrupt" signal
- Thirteen bits of data to the guidance computer

Each of these 35 information bits is encoded into 5 sub-bits (total of 175 sub-bits). The vehicle address is encoded into a different sub-bit pattern than the following 32 information bits.

Since this is a non-return to zero system, there is no time interval ("dead time") between bits, and individual period synchronization is obtained from the 1 kHz subcarrier. The bit transmission rate is also derived from the 1 kHz timing system; therefore, the sub-bit rate is 1 kHz(0.001 second) and the information bit rate is 200/second (0.005 second).

The sub-bit patterns are chosen for optimum differentiation between information "ones" and "zeros" to provide maximum error detection capability. For any particular flight, only 4 of the possible 32 ($2^5 = 32$) 5-bit patterns are used. Two of these five-bit patterns are used for vehicle address and two are used for the remainder of the message.

To simplify the following discussion, the sub-bits will be disregarded unless particular reference is made to the baseband PSK modulator or demodulator.

The first 3 bits of each command word represent a vehicle address. (These bits are not coded in the same sub-bit pattern as the following 32 bits.) They will be referred to as "X" bits. The 3 bits of vehicle address are applied to distinguish between commands for the Saturn IU and commands for the Apollo Spacecraft. Both messages are transmitted over the same carrier frequency. The vehicle address may be different for each flight. The three "X" bits are also used to reset the onboard decoder prior to receipt of the following 32 bits of the message. Fourteen of the other 32 bits in the word are used as a decoder address. These bits are distributed throughout the word as shown in Figure 6.2-4. The 14 address bits are compared with a prewired

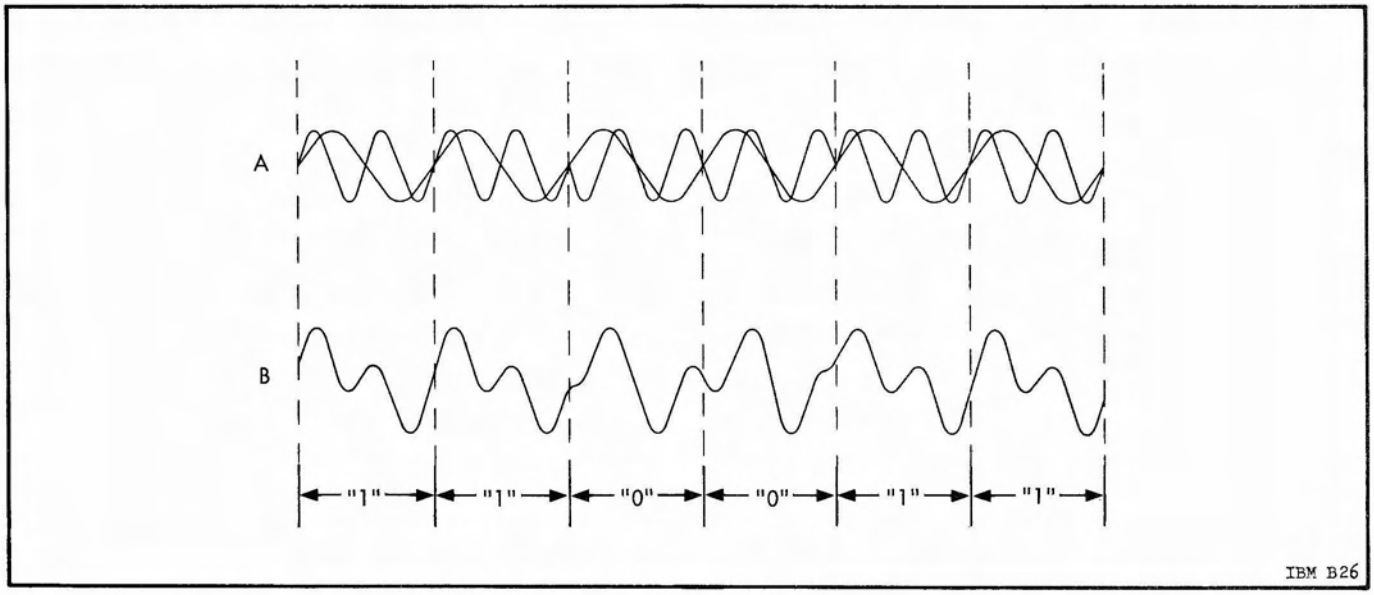


Figure 6.2-3 Phase Shift Keyed Signals

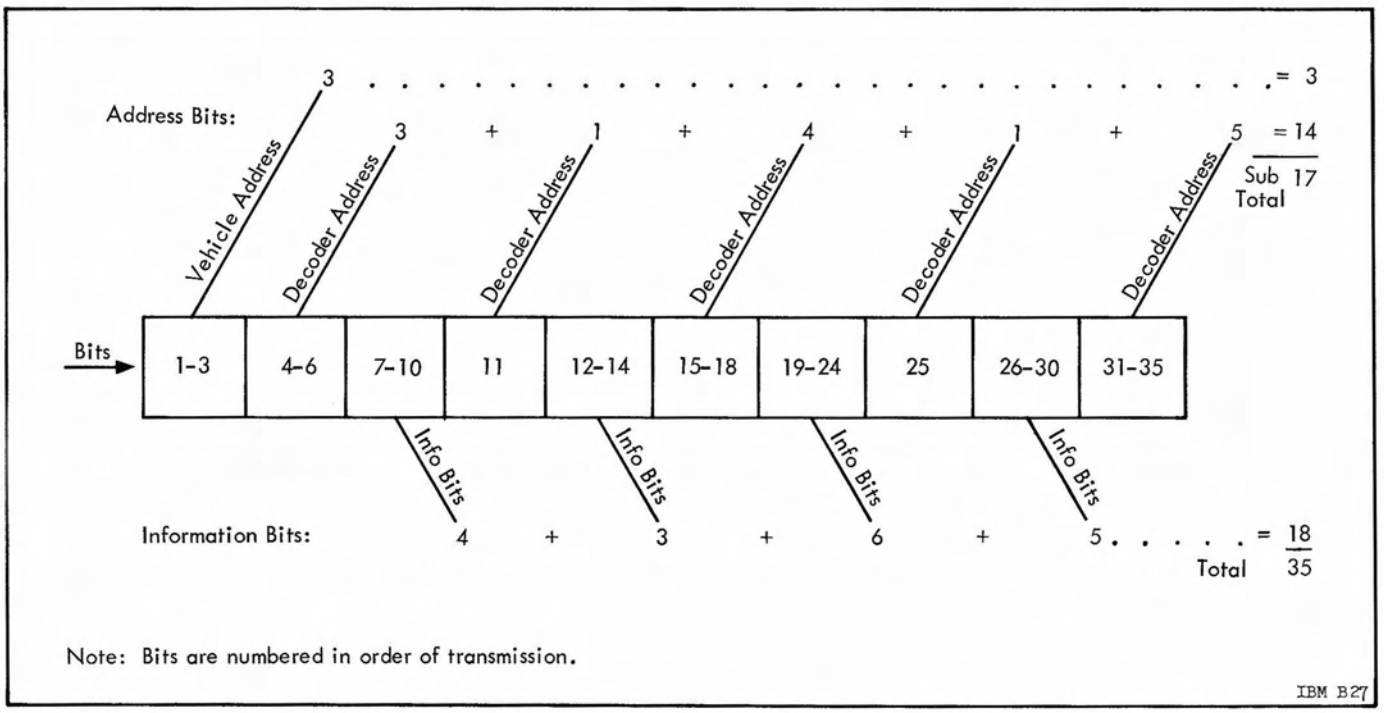


Figure 6.2-4 Digital Format Showing Address Distribution

address in the digital decoder and are used to perform error checking. The remaining 18 bits are information bits which are used to convey binary data to the LVDC. (All data for the LVDC is processed by the LVDA, which is the input-output device for the LVDC.)

The 18 information bits are divided into functional groups as shown in Figure 6.2-5. The first bit is a mode bit, the next two are called interrupt bits, and the next two are sync bits. The remaining 13 bits are called data bits. The two interrupt bits are always binary "1's". These 2 bits are logically combined in the LVDA and presented to the LVDC as an interrupt input. When the LVDC receives this input, it interrupts its normal program sequence and accepts the message from the IU command system. The mode bit and sync bits are all "1's" or all "0's", depending on whether the particular 35-bit command word is a mode command word or a data command word, respectively. The other 13 bits represent the binary coded data for the LVDC.

COMMAND TYPES

Only 13 bits out of each 35-bit command word can be utilized to carry data to the LVDC. It is sometimes necessary to transmit more than one command word to complete a given message (command).

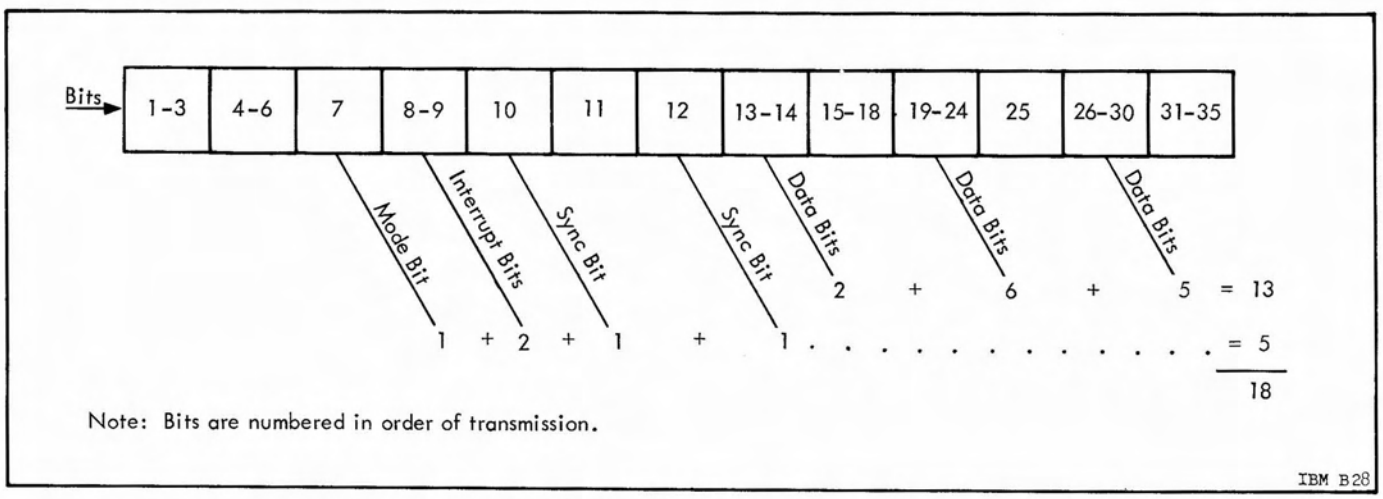


Figure 6.2-5 Digital Format Showing Information Bit Groups

Present plans call for the LVDA to be capable of receiving seven different types of messages, although this can be expanded to many more if necessary. The seven different messages are as follows:

- Update LVDC
- Execute update
- Enter Switch Selector mode
- Enter closed-loop test
- Execute subroutine command (e.g., telemeter flight control measurements)
- Memory sector dump
- Telemeter single memory address

The type of command being transmitted is determined by the first 35-bit word of the message. This first word is always a mode command word, and the most significant 6 bit slots of the 13-bit data group are coded to establish which one of the seven command types is being sent. The next 6 bits are complements of the preceding 6 bits. The last bit in the data group is not used. The second and subsequent 35-bit words of each message are always data command words except for command Types (2), (4), and (5), which are discrete commands requiring only the mode command word. Command Type (1) requires at least four data command words per LVDC word. If additional LVDC words are required, more data command words are sent, but always in multiples of four. As many as 10 groups of four data command words may follow the mode command word to complete one Type (1) command. Command Types (3) and (6) require only two data command words per message. Four data command words are required for Type (7).

Table 6.2-1 summarizes the composition of each of the 7 types of commands. Figure 6.2-6 shows the format for a mode command word. The data command word format depends on the particular command type, and since all of these formats have not been firmly decided, only the proposed format for a Type (1) data command word is shown (see Figure 6.2-7).

Table 6.2-1 Number of Words Transmitted for Different Commands

Command Type	Number of Command Words Required	First Word	Subsequent Words
(1)	5, 9, 13, 17, 21, 25, 29, 33, 37, 41	MCW	DCW
(2)	1	MCW	-
(3)	3	MCW	DCW
(4)	1	MCW	-
(5)	1	MCW	-
(6)	3	MCW	DCW
(7)	5	MCW	DCW

Note: MCW - Mode Command Word
DCW - Data Command Words

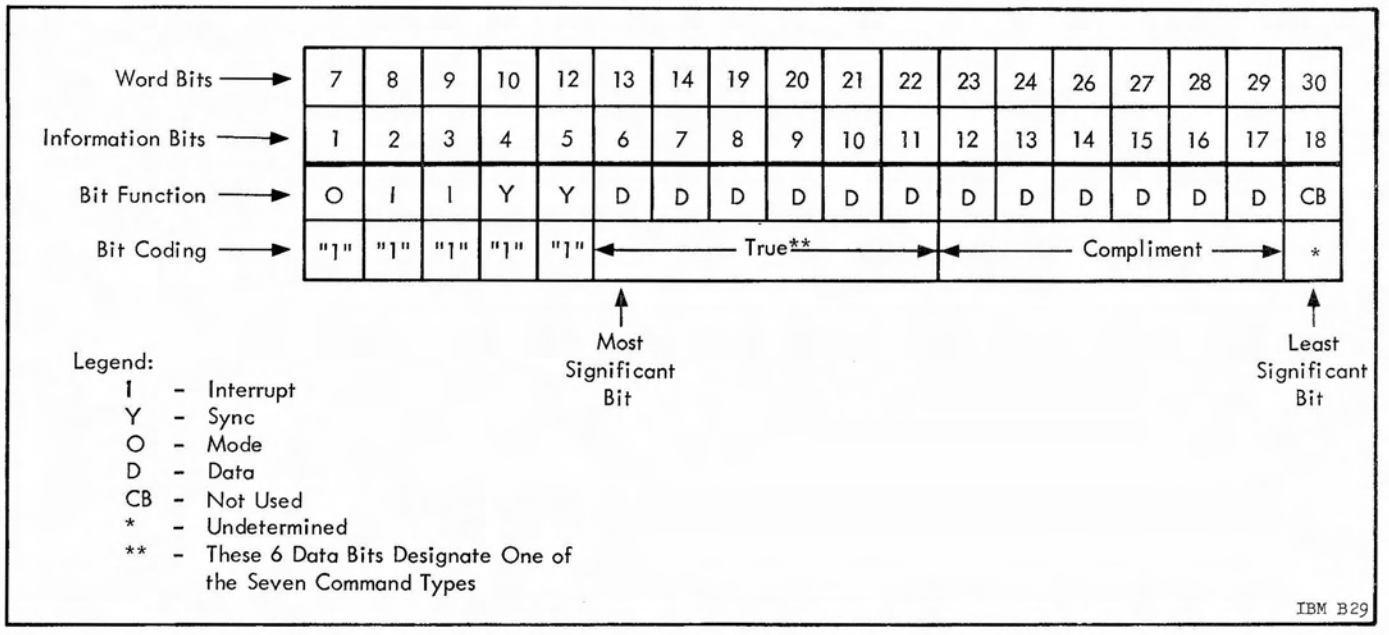


Figure 6.2-6 Mode Command Word Format and Coding

6.2.4 COMMAND RECEIVER

The Saturn IB IU command system uses the MCR-503 Receiver with a frequency range of 406 to 450 MHz. In the Saturn V Vehicle the IU command is received by the S-band transponder of the Saturn command and communication system. This S-band receiver is described in Section 6.4.

A block diagram of the MCR-503 Receiver is shown in Figure 6.2-8. The receiver RF signal is coupled from the RF input, J1, to a fixed-tuned, low-pass filter which has a cutoff frequency of approximately 570 MHz. The output of the low-pass filter is connected to a critically coupled, double-tuned bandpass filter, which is tunable over the required frequency range of 406 MHz to 450 MHz. The bandpass filter output is amplified by the RF amplifier stage. This amplifier provides additional rejection to signals outside the receiver passband and is tunable over the required frequency range. The low-pass filter, bandpass filter, and RF amplifier are contained in the preselector assembly. The -3 db bandwidth of the complete preselector assembly is approximately 4 MHz. The gain is approximately 5 db.

The preselector RF amplifier output is coupled to the first mixer. Here the multiplied output of the local oscillator is heterodyned with the RF signal to produce the first IF signal. The first IF signal is amplified by the first IF amplifier and applied to the second mixer, where it is heterodyned with a signal at the local oscillator frequency to produce the 10.7 MHz second IF signal. The local oscillator is crystal controlled and has a tuning range of 100 to 120 MHz. During factory alignment, the oscillator, multiplier, first mixer, and first IF amplifier are tuned to provide maximum sensitivity. The first and second mixer, first IF amplifier, crystal oscillator, and frequency multiplier are contained in the first IF assembly. The -3 db bandwidth of this assembly is approximately 1.5 MHz and the gain is approximately 43 db.

The 10.7 MHz output of the first IF assembly is coupled directly to the IF bandpass filter. This passive LC filter determines the overall receiver bandpass characteristics. The nominal -3 db bandwidth of the filter is 340 kHz and the -60 db bandwidth is 1200 kHz. The filter insertion loss is approximately 10 db.

The bandpass filter output is fed to the second IF assembly, which contains two feedback amplifier pairs. Each pair has a gain of approximately 30 db. The output of each pair is tuned to 10.7 MHz. The output of the second amplifier pair feeds both the limiter-discriminator assembly and the signal strength telemetry circuit. The low-level signal strength telemetry output is a dc voltage that is proportional to the receiver RF input signal.

Word Bits →	7	8	9	10	12	13	14	19	20	21	22	23	24	26	27	28	29	30
Information Bits →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	O	I	I	Y	Y	S	S	S	S	M	M	M	D	D	D	D	CC	CC
2	O	I	I	Y	Y	A	A	A	A	A	A	A	A	L	*	*	CC	CC
3	O	I	I	Y	Y	D	D	D	D	D	D	D	D	D	D	D	CC	CC
4	O	I	I	Y	Y	D	D	D	D	D	D	D	D	D	D	D	CC	CC

DCW Number →

Legend:

A - Word Time
D - Data
I - Interrupt
O - Mode
Y - Sync
L - Last Word Group
M - Module Address
S - Sector Address
CC- DCW Counters (Tag Bits)
* - Unused

Bit Code:

I - "1's"
O - "0"
Y - "0's"
S,M,D,A,L - As Required
CC- "0-0"=1, "0-1"=2, "1-0"=3, "1-1"=4

IBM B30

Figure 6.2-7 Data Command Word Group Format and Coding for an Update Command

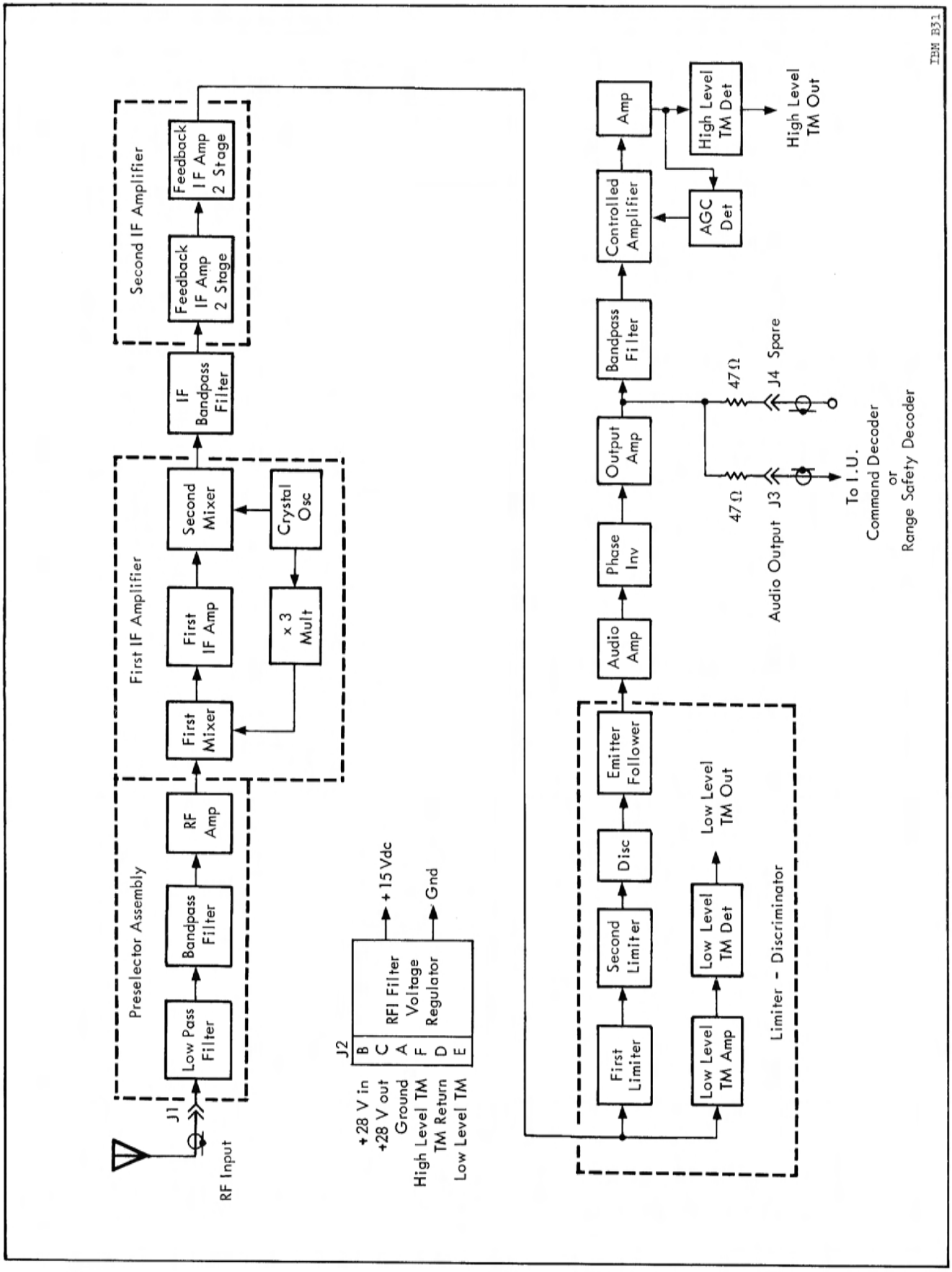


Figure 6.2-8 MCR-503 Command Receiver

Limiting is accomplished in the first limiter by the back-to-back diodes in the transistor collector circuit. The second limiter limits by saturation and cutoff of the transistor and drives the Foster-Seeley discriminator. The discriminator sensitivity is approximately 4 millivolts rms per kHz of peak deviation. The emitter follower output stage is used for impedance isolation between the discriminator and the audio amplifier.

The audio amplifier consists of a voltage amplifier stage, a phase inverter, and a low impedance output stage. The nominal voltage gain of the amplifier is 14 db. The lower -3 db frequency is approximately 250 kHz. The overall receiver -3 db bandwidth is approximately 600 Hz to 80 kHz. This is set by the output circuit of the discriminator. The amplifier output feeds two 47-ohm isolation resistors, each one of which feeds an output connector. These resistors allow one output to be shorted to ground without reducing the other output voltage more than 3 db. One of these outputs will be used as the input for the IU Command Decoder. The amplifier output also feeds a bandpass filter. This filter output is fed to an AGC-controlled amplifier and then to the high-level telemetry detector circuit. The telemetry voltage thus obtained will provide a useful measure of RF input signal up to 500 microvolts.

In the case of the secure range safety command system, one of the receiver outputs will be used as an input to the range safety decoder.

Characteristics of the MCR-503 Receiver are given in Table 6.2-2.

6.2.5 DECODER OPERATION

The decoder is the interface unit between the IU Command Receiver and the LVDA. Data transmission is made through a 32-bit word which is preceded by three vehicle address bits ("X"-bits). Each data and address bit is composed of 5 sub-bits. The total 175 sub-bit message must be decoded into the original message configuration of 35 bits before the data can be transferred into the LVDA for computer acceptance.

The functions of the IU Command Decoder are as follows:

- Demodulate the PSK baseband subcarriers.
- Recover the original 175 sub-bits.
- Compare each 5 sub-bit group against three prewired bit codes to recover the 35-bit command word.
- Check that all 35 bits are received.
- Check that each bit is received within the 5-millisecond bit period.
- Check that the 3-bit vehicle address and the 14-bit decoder address are correct.
- Inhibit any further decoding if any of the checks are invalid.
- Present the 18 information bits to the LVDA in parallel form.
- Present an "address verification" signal to PCM telemetry.
- Receive the "LVDC reset" signal from the LVDA and present this signal to PCM telemetry.

Table 6.2-2 Characteristics of the MCR-503 Receiver

Frequency range	406 to 450 MHz
Frequency deviation	±30 kHz (for 1 V rms output)
Quieting	15 db at 10 microvolts
Maximum RF input	2.0 V rms
Input VSWR	1.5:1 maximum
Tuning stability	± 30 kHz
Oscillator	Crystal controlled, single crystal
RF bandwidth (-3 db)	340 ± 30 kHz
RF bandwidth (-60 db)	1200 kHz
Type of output	Audio, two isolated outputs
Audio bandwidth (-3 db)	1 to 80 kHz
Audio distortion	Less than 5 percent
Audio output level	1.4 V rms into 75 ohms (with two tones, ± 30 kHz deviation per tone)
Input voltage	+22 Vdc to +36 Vdc
Weight	1.4 kg (3.1 lbs)
Power	3.5 watts at 28 Vdc
Outline dimensions	
Height	8.6 cm (3-3/8 in.) (less connectors)
Width	13.4 cm (5-1/4 in.)
Depth	11.7 cm (4-9/16 in.)

The operation of the decoder can best be explained by breaking the decoder into two logical functional parts as shown in Figure 6.2-9.

PSK SUB-BIT DEMODULATOR

The onboard receiver demodulates the RF carrier and presents the composite baseband signal (Figure 6.2-3) to the IU Command Decoder. The purpose of the PSK demodulator is to separate the 1 and 2 kHz signals, compare the phase of the 2 kHz tone with the 1 kHz reference tone once each millisecond, and generate a pulse on the "1" output circuit or the "0" output circuit, as the case may be. Figure 6.2-10 is a synchrogram of the various waveforms generated in the PSK demodulator by the input signal. Figure 6.2-11 is a simplified block diagram of the PSK demodulator. For the purpose of illustration, a transmitted signal consisting of 3 sub-bits in 0-1-0 order is shown in A of Figure 6.2-10. This composite signal is amplified and fed to an emitter-follower stage to provide signal driving power for the tuned filters. The overall gain of these first 2 stages is approximately 3. This gain varies slightly over the temperature range due to the action of a temperature sensitive resistor in the emitter-follower stage. This gain change compensates for other temperature-caused gain changes in the detector.

A sharply tuned filter network recovers the 1 kHz component of the composite input waveform. The output of this network is shown in B of Figure 6.2-10.

The 1 kHz sine wave is capacitive coupled to a shaper circuit which acts to "square up" the positive half cycle of the input waveform (see C of Figure 6.2-10). This waveform is differentiated and the positive pulse used to trigger a monostable multivibrator. The trailing edge of the monostable output waveform is differentiated, shaped and amplified, and fed as one input to each of two AND gates. The output of the amplifier, shown in D of Figure 6.2-10, is a very narrow pulse appearing at a 1 kHz rate, and will hereinafter be referred to as the "sampling" pulse.

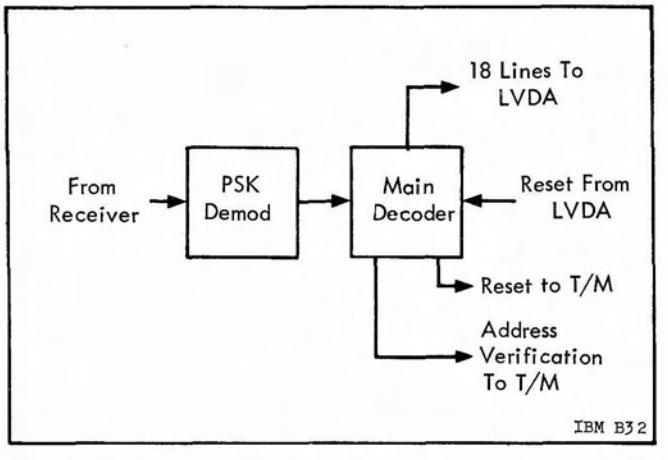


Figure 6.2-9 IU Command Decoder Functional Block Diagram

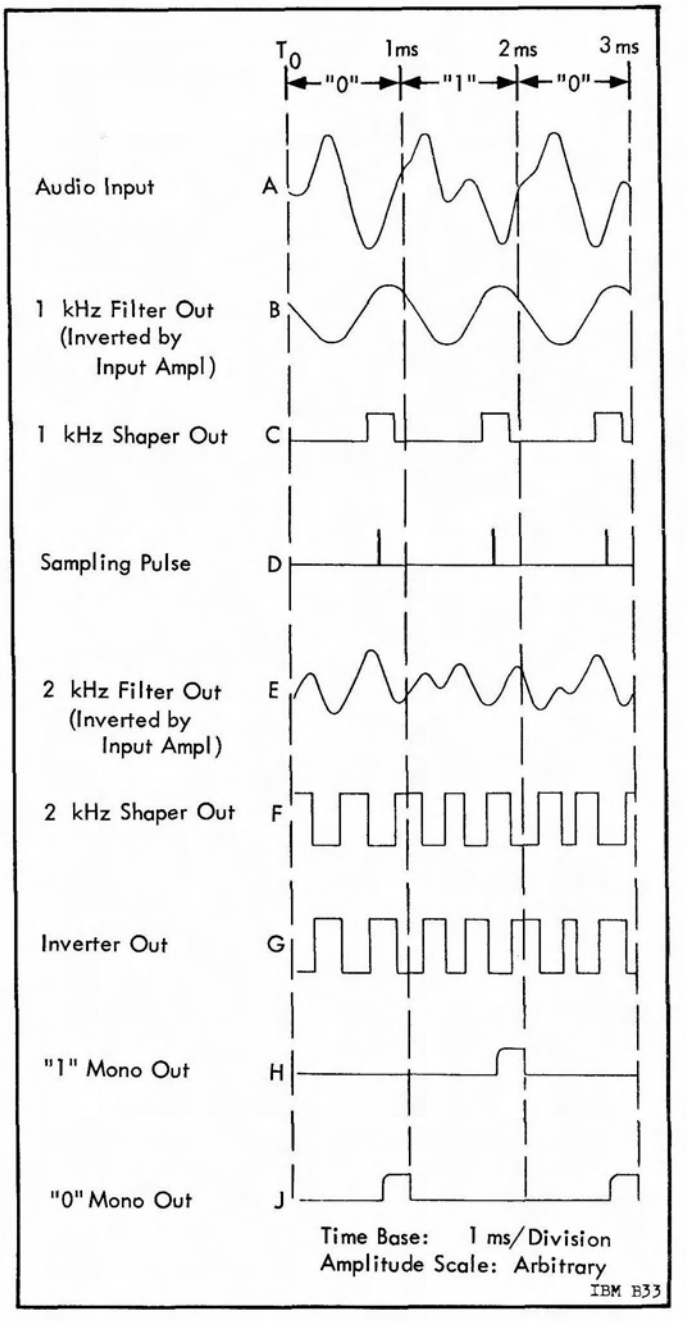


Figure 6.2-10 PSK Sub-bit Detector Synchrogram

The output of the emitter-follower driver is also applied to a 2 kHz tuned filter. In contrast to the 1 kHz filter, the 2 kHz filter is broadly tuned, thus providing greater sensitivity at low receiver RF input levels. The output of the 2 kHz filter is shown in E of Figure 6.2-10. The 2 kHz waveform is capacitive coupled to a shaper circuit. The output of this shaper is shown in F of Figure 6.2-10. The shaper output is applied to 2 places: first, it is applied to an inverter stage, and second, it is applied to the "1" AND gate. Waveform D of Figure 6.2-10 shows the sampling pulse input to the "1" AND gate, and F of Figure 6.2-10 shows the shaped 2 kHz input to the same gate. When the 2 kHz waveform is positive and time coincident with the sampling pulse, the "1" AND gate will produce an output pulse. This pulse will trigger the "1" monostable multivibrator to the "ON" stage. The time period of this monostable is 200 microseconds ± 10 percent. Waveform H of Figure 6.2-10 shows the monostable output, which is fed to the input of the sub-bit decoder.

The output of the inverter (G of Figure 6.2-10) is applied to the "0" AND gate along with the sampling pulse (D of Figure 6.2-10). In a manner similar to that described previously, the "0" AND gate will produce an output pulse and trigger the "0" monostable (see J of Figure 6.2-10). Note that both AND gates cannot have an output at the same time.

The synchrogram shows an approximate phase lag of the 1 kHz waveform, with respect to t_o, of about 45 degrees. The 2 kHz waveform also exhibits a phase lag, although the degree of lag is difficult to measure unless all "1's" or all "0's" are being transmitted. The RF link is a contributor to this phase lag, as well as the filters in the PSK sub-bit detector. It is obvious that too much of a relative phase difference between the 1 kHz and the 2 kHz components will cause the detector to malfunction (lose data). In order to provide maximum insensitivity to this relative phase difference, the timing resistor of the sampling monostable is selected so that the sampling pulse falls as

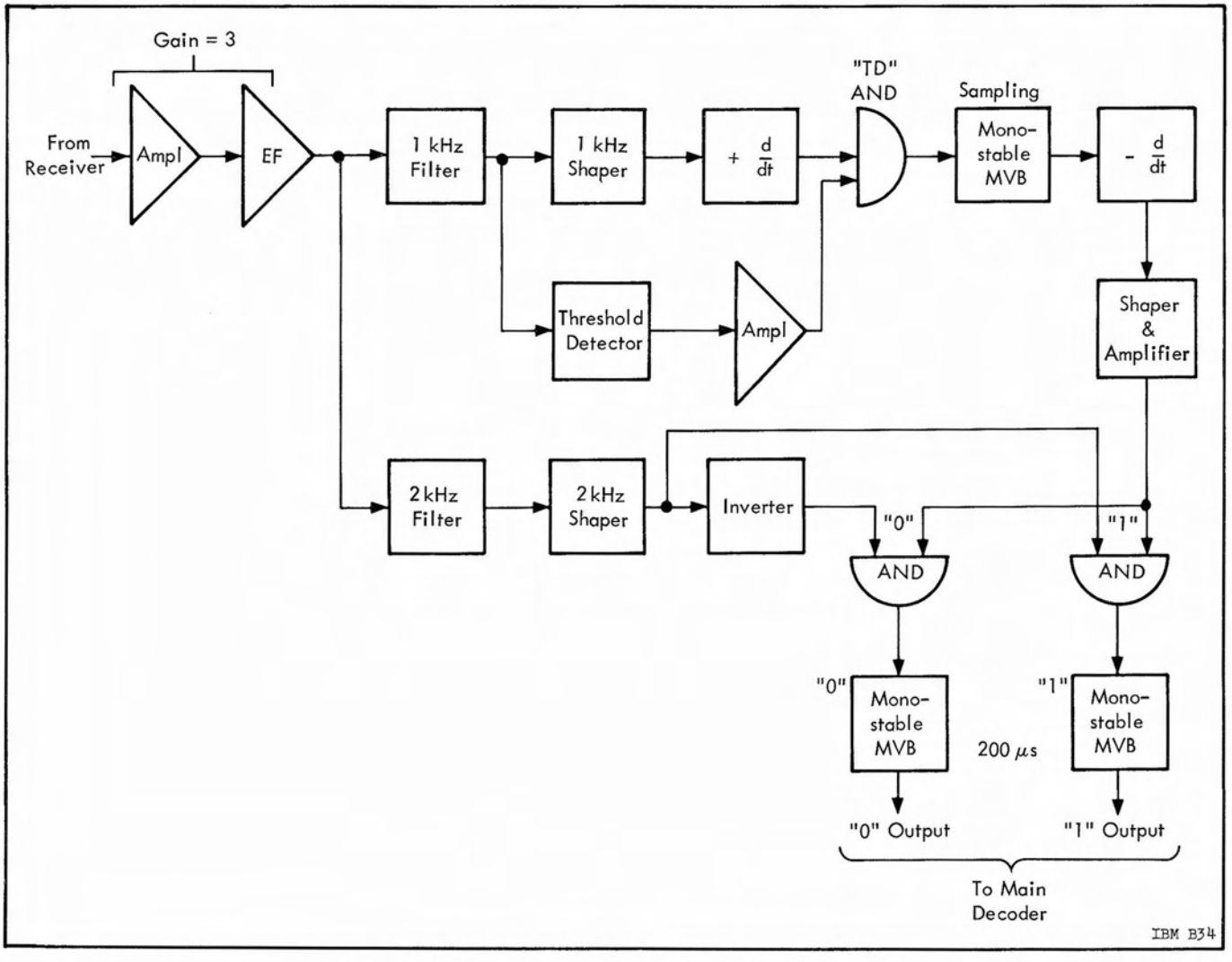


Figure 6.2-11 PSK Sub-bit Detector Block Diagram

closely as possible to the center of the positive portion of the second cycle of the 2 kHz shaped waveform. This timing is accomplished under conditions as near ideal as possible; which means the use of a modulator known to be in good phase alignment, a properly operating signal generator, and a flight qualified (electrically) receiver. Such a procedure ensures that any relative phase difference caused by the equipment is compensated for, and that any variation encountered during flight will occur only from uncontrollable sources (such as differences in ground equipment).

When the IU command system is operating with an uncaptured receiver, it is desirable to inhibit the PSK demodulator from making decisions due to noise. This is accomplished by the threshold detector, amplifier, and the TD AND gate (Figure 6.2-11). When a PSK-modulated carrier is present, the output of the 1 kHz filter will be of sufficient amplitude to cause the threshold detector to reach a decision. The voltage obtained is amplified and used as the control input for the TD AND gate. Thus, when a normal signal is present, the TD AND gate will not inhibit the differentiated 1 kHz shaper output pulses from triggering the sampling monostable. When only noise is present at the detector input, the 1 kHz filter output will not be large enough to cause the threshold detector to reach a decision. Consequently, the TD AND gate will not allow any pulses to get through and trigger the sampling monostable. This prevents any sub-bit detection.

A continuous series of sub-bit "1's" are transmitted during "dead time" between messages from the digital command system unit in the ground station. The threshold detector, therefore, will have an output and the detector will be "ready" to accept a message.

MAIN DECODER

The operation of the main decoder is best explained by the use of the block diagram, Figure 6.2-12, and the flow diagram, Figure 6.2-13. During "dead time" between messages, a continuous stream of sub-bit "1's" is being transmitted. These sub-bits are fed to the sub-bit decoder where they are written into the 5-bit shift register. Each sub-bit, as it leaves the sub-bit detector, is 200 microseconds in duration. The leading edge of this 200-microsecond waveform is differentiated and used as the shift pulse for the 5-bit shift register. The bits are written into the register by the differentiated trailing edge.

The shift register has 10 outputs (2 for each position) resulting in 2^5 (32) possible sub-bit patterns. Each of the 3 sub-bit comparators "X", "1", and "0", have 5 wires connected to the 5-bit shift register, 1 wire to each position (Figure 6.2-13). If, for example, the sub-bit code for a "1" is chosen as "11010", the sub-bit code for a "0" may be chosen as the "1" complement, and the "X" sub-bit code is chosen to be "11000", then the wiring between the sub-bit comparators and the 5-bit shift registers will be shown in Figure 6.2-14.

With all "1's" being transmitted, the comparators will not have an output. When a message starts, the first 3 bits will be "X" bits (vehicle address). The first "X" bit is recognized in the "X" comparator even though the 5-bit counter is not operating because AND 1 is inhibited (Figure 6.2-12). The first "X" comparison is made possible because the output from OR 6 is not significant at this time. This inhibiting output of OR 6 is inverted by a logical inverter, passes through OR 3, and provides the sixth input to the "X" comparator. The 200-microsecond output pulse from the "X" comparator is then differentiated. The leading edge passes through AND 2 since the inhibiting input is not present, and resets the 5-bit counter and the 3-bit counter (if they are not already reset). The trailing edge of the "X" comparator output waveform goes to 2 places: (1) it adds a count to the 3-bit counter, and (2) it starts the missing-bit clock.

The missing-bit clock is essentially two monostable multivibrators, which, if a proper message is being received, will provide a continuous output from OR 6. This is accomplished by alternately triggering first one multivibrator, then the other. The "ON" cycle of the multivibrators is adjusted to be slightly greater (5.4 ms) than the duration of each data bit (5.0 ms). Thus the "OFF" multivibrator is triggered "ON" 400 microseconds before the "ON" multivibrator completes its cycle, and OR 6 will always have at least one input. When the missing-bit clock starts, the output of OR 6 will: (1) open AND 1, (2) inhibit AND 2, and (3) cause the output of the inverter (connected to input of OR 3) to change to the non-significant state.

As the next 5 sub-bits are written into the 5-bit shift register, they are counted by the 5-bit counter. When the counter reaches a count of five, the output passes through OR 3, thus enabling an "X" comparison. A valid "X" comparison will cause the 3-bit counter to advance to the count-of-two state, and will also keep the missing-bit clock running. The count-of-two output from the 3-bit counter will (1) clear the 32-bit shift register (the cleared state of this register is when there is a "0" stored in the "0" side of all 32 stages), (2) send a reset pulse to the

32-bit counter, and (3) send a reset pulse to the output flip-flop. After the third "X" bit has been recognized, the count-of-three output from the 3-bit counter will provide a direct-coupled signal to AND 3 and AND 4. As long as this signal is present, AND 3 and AND 4 are "open", that is, they will allow valid "0" and "1" bits to pass through.

The next 32 bits will be coded with "0's" and "1's" as required. Each time a count-of-five state is reached by the 5-bit counter, a comparison is made to determine if the bit is a "0" or a "1". If it is a "0" or a "1", a pulse will be produced at the output of OR 5, thus keeping the missing-bit clock running. These 32 bits will also be shifted and written into the 32-bit shift register, and counted by the 32-bit counter. Upon the count of 32, a 1-millisecond monostable multivibrator is triggered "ON". This signal opens AND 5 and allows an address comparison to be made. If the address is correct, a signal will pass through AND 5 and trigger the output flip flop (a bistable multivibrator) to its set state. In addition, the two 60-millisecond monostable multivibrators will be triggered "ON", providing an indication to telemetry that the address was valid. Two multivibrators are used for reliability.

The set output of the flip flop also resets the 3-bit counter (through OR 4), and provides an enabling voltage to the 18 data output drivers. The binary information stored in the 18 data stages of the 32-bit shift register is thus transferred in parallel form to the LVDA. When the LVDC accepts these data-bits from the LVDA, a reset pulse acknowledging receipt is sent through the LVDA to the decoder. This pulse will pass through OR 8 and will clear the 32-bit shift register, reset the output flip flop thus disabling the 18 data-output drivers, and trigger two 60-millisecond monostable multivibrators. The outputs of these 2 multivibrators are sent to telemetry to indicate receipt of the LVDC reset pulse. If, for some reason, the LVDC reset pulse does not arrive prior to the beginning of the next message, the second "X" bit of vehicle address will provide an output from the 3-bit counter to reset the decoder circuits.

Characteristic data of the IU command system are summarized in Table 6.2-3.

6.2.6 DATA VERIFICATION

The application of the IU command system and the information transmitted through the system requires a high probability that a correct command message will be received in the vehicle. This high probability is obtained by the use of several different techniques throughout the system.

First of all, the Manned Space Flight Network is designed to provide a high degree of data transmission accuracy from the originating station in Houston, Texas, to the down-range DCS unit, or data processing computer, which actually transmits the message to the vehicle. Secondly, in order to transpose a "1" bit to a "0" bit or vice-versa, every one of the five sub-bits must be transposed to its compliment; and this must be done in multiples of five in synchronism with the bit rate (200 bits per second) or the message will be rejected. Thirdly, 17 bits of each 35-bit transmission must be correct (there is no possibility of an undetected error here) before the 18 information bits are presented to the LVDA. Last of all, a verification loop utilizing telemetry as a down-link is employed to verify the 18 information bits for critical commands (the LVDC update commands). The other types of commands are not so critical in nature and do not require bit-for-bit verification.

The verification loop works as follows. If the 14-bit address is correct, an address verification pulse is sent to telemetry. This pulse is decommutated in real time at the ground station and presented to the message acceptance pulse circuitry. See Figure 6.2-15. A second pulse is also derived in the vehicle and sent to telemetry. This is the LVDC reset pulse which signifies that the LVDC has received the 18 information bits. This pulse is also decommutated in real time and routed to the message acceptance pulse circuitry. The address verification pulse triggers a 200-millisecond monostable multivibrator to

Table 6.2-3 Characteristics of the IU Command System

Transmission frequency band	406 to 450 MHz
Transmission sub-bit rate	1000 per second
Transmission bit rate	200 per second
Modulation	PSK
Word length	35 bits
Probability of an undetected error	$\approx 1 \times 10^{-9}$
Dual mode of operation	(A) Bit-by-bit verification (B) Message verification
Transmission message rate	Two per second as determined by message verification

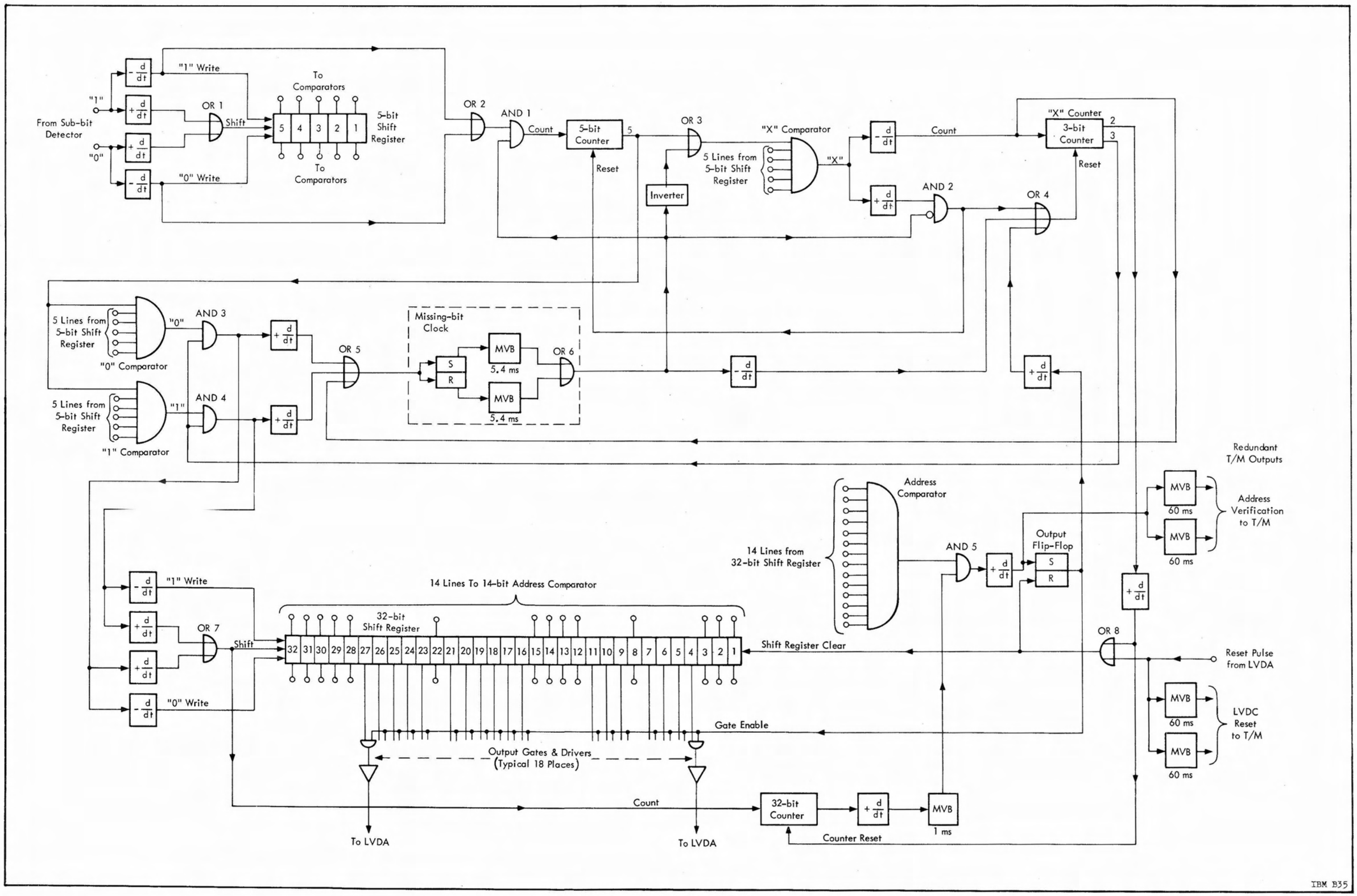


Figure 6.2-12 IU Command Decoder Simplified Logic Diagram

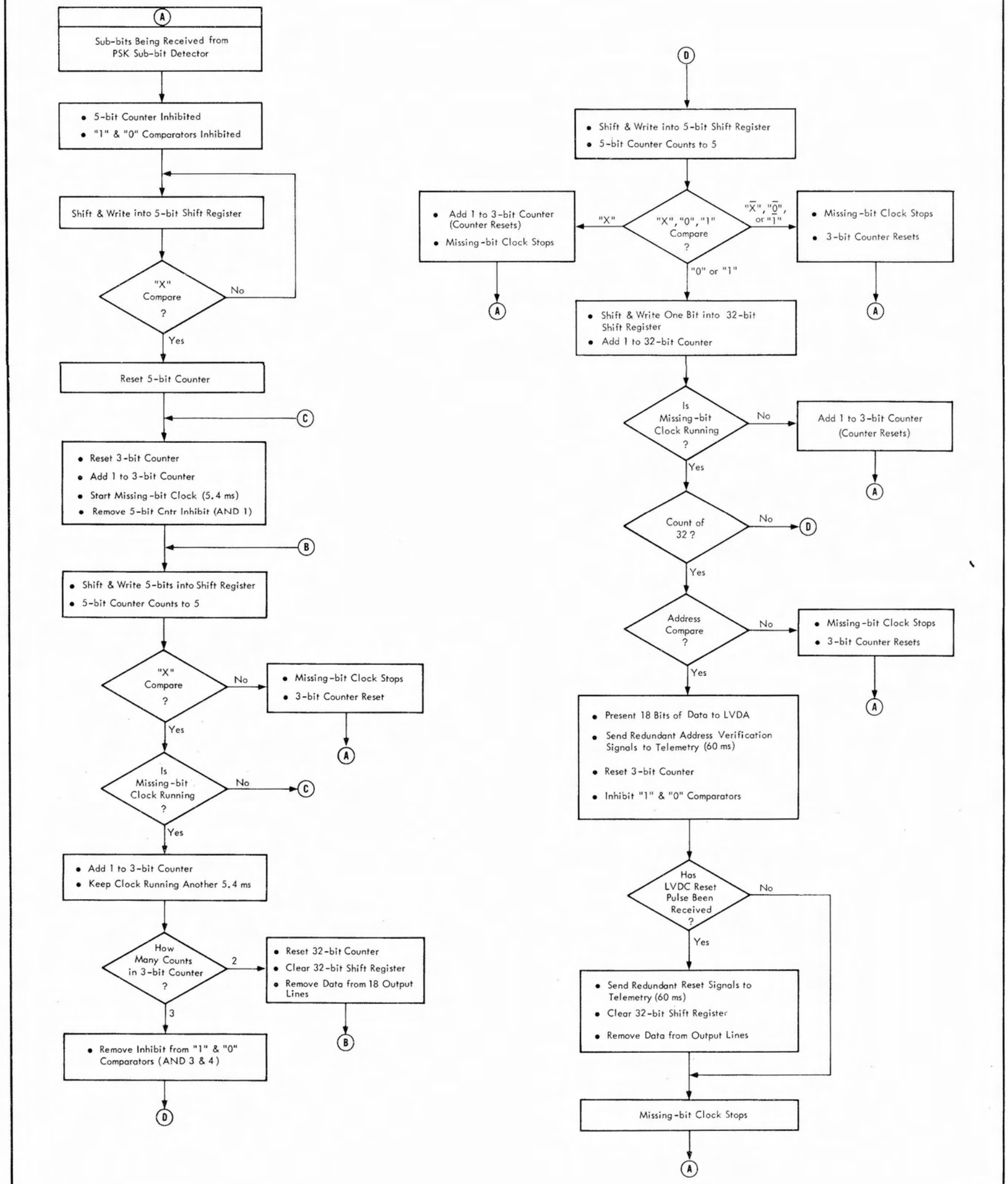


Figure 6.2-13 IU Command Decoder Flow Diagram

the "ON" state. The LVDC reset pulse will occur a short time thereafter and trigger a 10-millisecond monostable multivibrator to the "ON" state. If the LVDC reset pulse does not appear during the "ON" time of the address verification pulse multivibrator, then it will not appear at all for a given transmission. The 2 multivibrator outputs are logically-combined in an AND gate, which will have an output only when both multivibrators are "ON" at the same time.

The 10-millisecond pulse thus produced is called the message acceptance pulse and is fed to the DCS, or data processing computer. The DCS, or data processing computer, uses this message acceptance pulse as a "next-message-transmit" pulse. Upon receipt of this pulse, the DCS, or data processing computer, will transmit the next message (if any). If the message acceptance pulse does not appear within a certain length of time (approximately 400 milliseconds from start of message), the DCS, or data processing computer, will then retransmit the message.

To complete the data verification, the LVDC stores all LVDC update messages (as many as forty 18-bit groups) and non-destructively reads out these data bits to telemetry. Upon receipt by the ground station, these bits are sent to Houston via the Manned Space Flight Network and compared with those originally transmitted. If all bits are verified, an "execute update" command is sent to the DCS, or data processing computer and thence to the vehicle. Only upon receipt of this message will the LVDC act upon the "update" data bits.

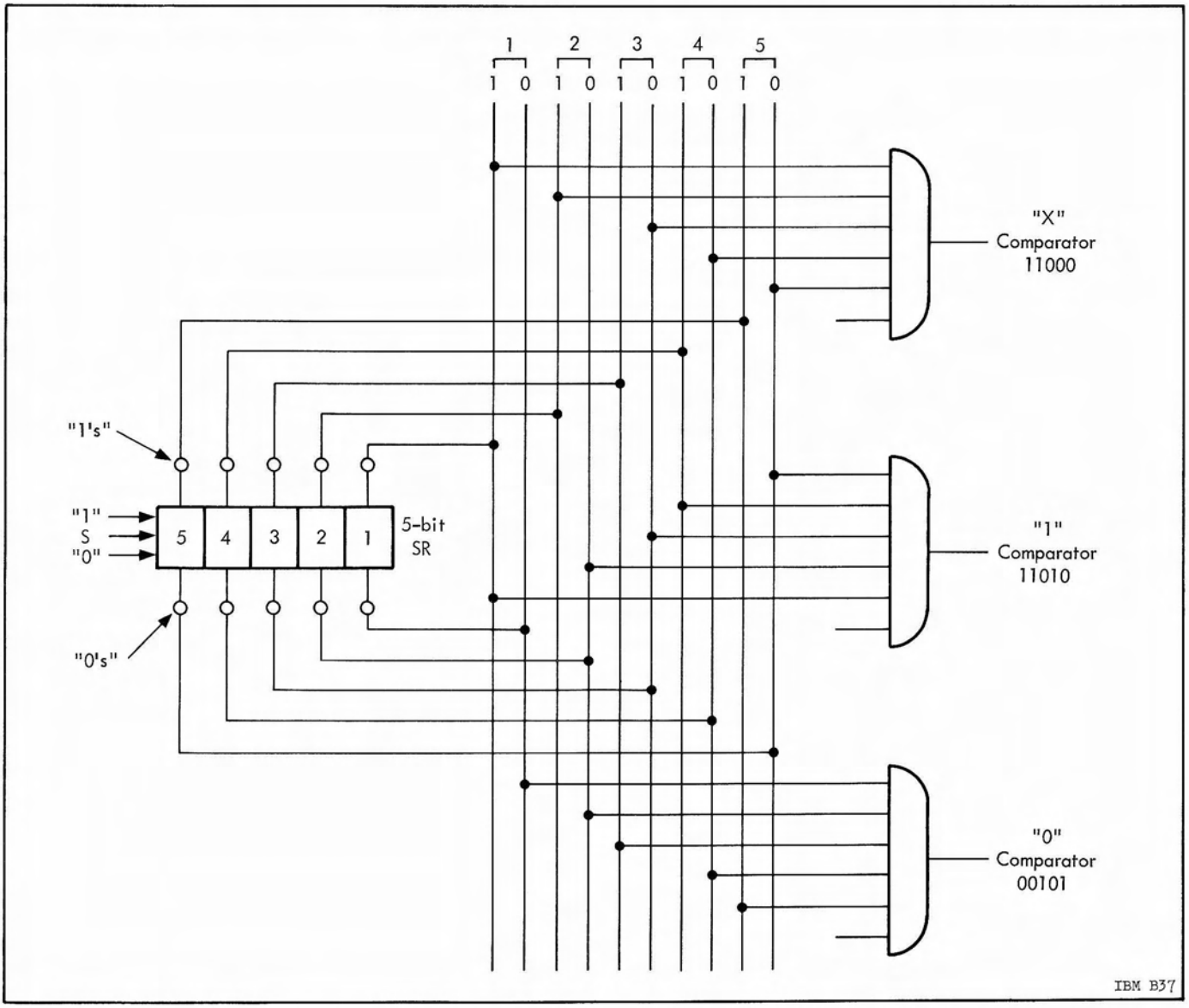


Figure 6.2-14 Example of Wiring Between Shift Register and Sub-bit Comparators

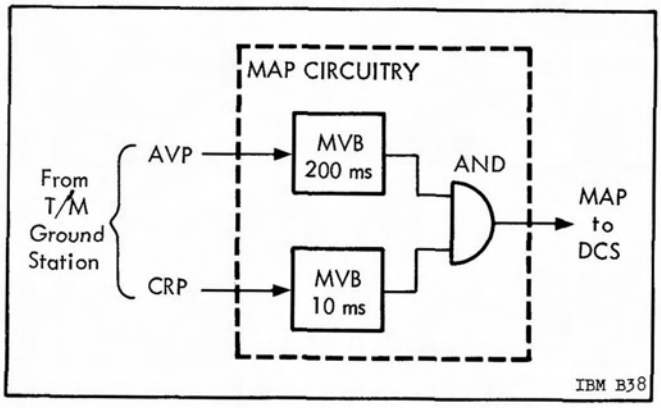


Figure 6.2-15 MAP Circuitry Block Diagram

A different approach of message verification is used for all mode command words and the data command words for command Types (3), (6), and (7). For these commands, one-half of all data bits are transmitted as required in "true" form; and the other half in complimentary form. This is called duplex coding. The LVDA will reject a command unless the compliment bits check out to be the inverse of the true bits. Such a procedure provides a greater probability of receiving the same message as was transmitted.

SECTION 6.3

SECURE RANGE SAFETY COMMAND SYSTEM

6.3.1 OVERALL SYSTEM

The secure range safety command system provides a high degree of protection against intentional interrogation by unfriendly intruders and against unintentional interrogation (false alarms) by noise. The security against intentional interrogation is measured by the fraction of the total code combinations that an intelligent unfriendly interrogator, having unlimited technical resources, would be able to transmit during equipment access time. It is assumed that all system parameters are known to him except the code-of-the mission. The security against unintentional or randomly generated false alarms is, as it should be, much greater than against intentional, intelligent interrogation. All hardware is unclassified except the actual flight code plugs.

A simplified block diagram of the secure range safety command system is illustrated in Figure 6.3-1. Each address character is chosen by the code plug. Two identical code plugs, one in the ground encoder and the other in the flight decoder, are used. This removable, inexpensive, easily stored code plug minimizes the actual operational difficulties of handling the security aspects of the system, thus eliminating the necessity of classifying the system hardware (decoder and encoder).

6.3.2 MESSAGE FORMAT

The message transmitted to the vehicle consists of 2 words; an address word and a function or command word. The address word consists of 9 characters of a high-alphabet system, and the function word consists of 2 characters; thus the total message comprises 11 characters.

Each character consists of two simultaneous symbols, which are audio-frequency tones between 7.35 kHz and 13.65 kHz. Each character can be tone coded by choosing from a symbol alphabet of 7 tones.

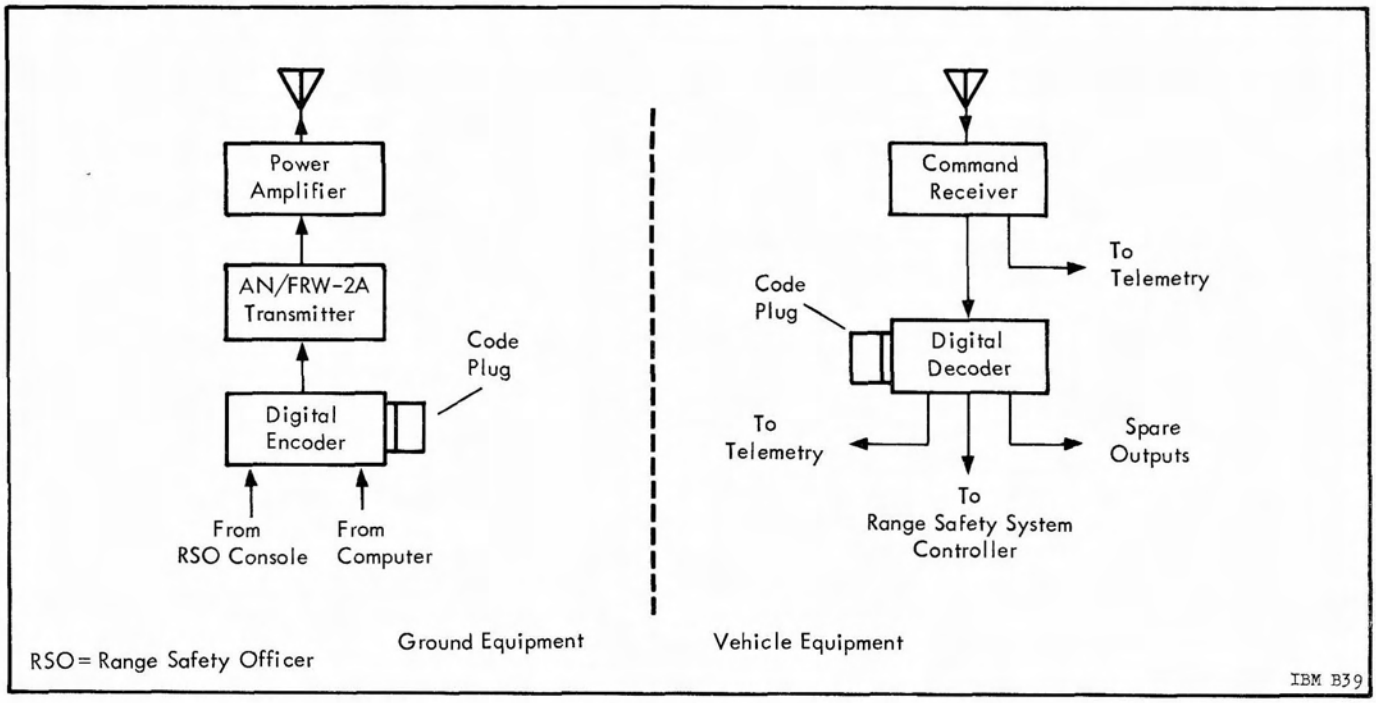


Figure 6.3-1 Secure Range Safety Command System

Since 2 tones are used simultaneously, the character alphabet is established at 21 possibilities or choices (no choice is repeated within a given word). Thus the encoding scheme is logically called high-alphabet.

The security of the message is realized mainly from the fact that only 9 out of 21 possibilities are used per address, and that these 9 address characters are position coded. The limited time of access to the equipment is the final factor in the security, for any code can be broken if access time is unlimited.

The function word consists of 2 characters. Since there are 21 character-coding arrangements available for the first function character and 20 for the second, 420 character/position codes are available for the function word. Only 5 functions are required of the system. To provide the maximum langauge difference between any two of these functions, 5 codes were chosen as commands in a spacing scheme which provides maximum security against command translations. These commands and their codes are listed in Table 6.3-1.

Each character period, including "dead time", is approximately 8.6 milliseconds in duration, except the eleventh, which is three times as long.

Each character of the 9 character address word is unique within a given address, and therefore the new system can operate without the necessity of a transmitted clock or reference synchronizing information. The symbols are, however, synchronous with the character interval period (and with each other) and are spaced and phased to minimize intersymbol interference, which could create unwanted characters.

Table 6.3-1 Coding Scheme for Function Characters

Command	10th Character Tones	11th Character Tones
1. Destruct (propellant dispersion)	1 and 2	1 and 3
2. Arm/fuel cutoff (charging of the EBW firing unit and thrust termination.)	2 and 3	2 and 4
3. MSCO/ASCO (Saturn spare No. 1)	4 and 5	4 and 6
4. Spare (No. 2)	3 and 4	3 and 5
5. Safe (command system switched OFF)	5 and 6	5 and 7

Note: Commands are listed in priority order.

The main RF carrier (450 MHz) is frequency modulated by a subcarrier system which in turn employs a multiple frequency shift technique. The term frequency shift keying is also used to describe the technique. The portion of the baseband occupied by the subcarrier system is approximately the same as that now reserved and used for range safety purposes (see Figure 6.5-2). The nominal tone frequencies, however, are not the same as the inter-range instrumentation group tone channel frequencies. The tone-frequency spacing is by design an integral multiple of the character repetition rate. This makes possible a simple phase-coherent tone keying scheme.

6.3.3 GROUND EQUIPMENT

A block diagram of the ground system is illustrated in Figure 6.3-2.

When the range safety officer decides to initiate a command from his console, he actuates a hooded toggle switch. The output of the encoder is then routed in parallel form to a tone remoting transmitter which processes the message for transmission over the 8 km distance to the transmitter site. A tone remoting receiver at the transmitter site demodulates the message and feeds it to a modulator that converts the parallel information to the high-alphabet 11-character format. The 11 dual-tone bursts are then fed to the AN/FRW-2A Transmitter System and to the vehicle. For reliability, a completely redundant backup system is provided, with a continuously monitoring error detector that provides automatic transfer to the backup system in case of a failure in the primary chain (this error detection and switching circuitry is not shown in the diagram).

The range safety equipment incorporates a priority-interrupt scheme that will interrupt any command being transmitted and transmit any higher-priority command selected by the range safety officer or originated by the computer. After completion of the transmission of the higher-priority command, the transmission of the interrupted command will resume.

The equipment at the downrange sites is illustrated in the block diagram of Figure 6.3-3. All downrange sites are connected by cable, and when the range safety officer presses a command switch on his console, the command pulse will be transmitted over the cable via the supervisory control system

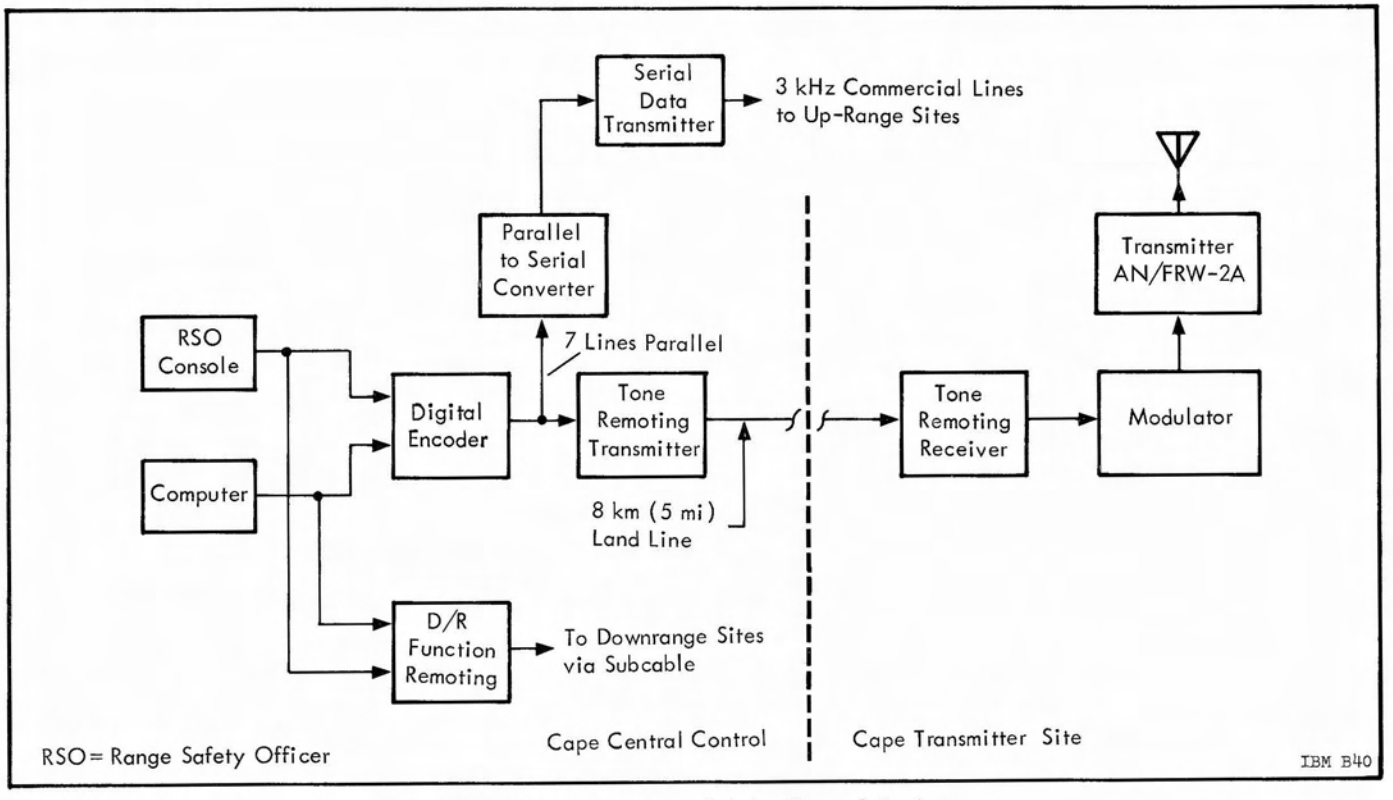


Figure 6.3-2 Range Safety Ground System

(this system will be replaced by a digital remoting system in the near future). All sites will receive the command, and the transmitter on the air at the moment the command is received transmits the message to the vehicle (to keep the onboard receiver captured, one transmitter is always radiating).

When the vehicle must be interrogated from an uprange site, the signal processing and routing is slightly different. As the parallel data leave the encoder at the cape central control, they are changed to serial form by a parallel-to-serial converter and then applied to a serial data remoting transmitter. After being checked for errors, the serial message will be received at the proper uprange site, converted to parallel form, and fed to the modulator. The modulator will convert the binary-coded message to the high-alphabet 11-character format. This message is then transmitted to the vehicle.

6.3.4 VEHICLE-BORNE EQUIPMENT

ANTENNAS

The type and number of antennas used will be such that their radiation pattern meets the requirements of range safety at the Eastern Test Range.

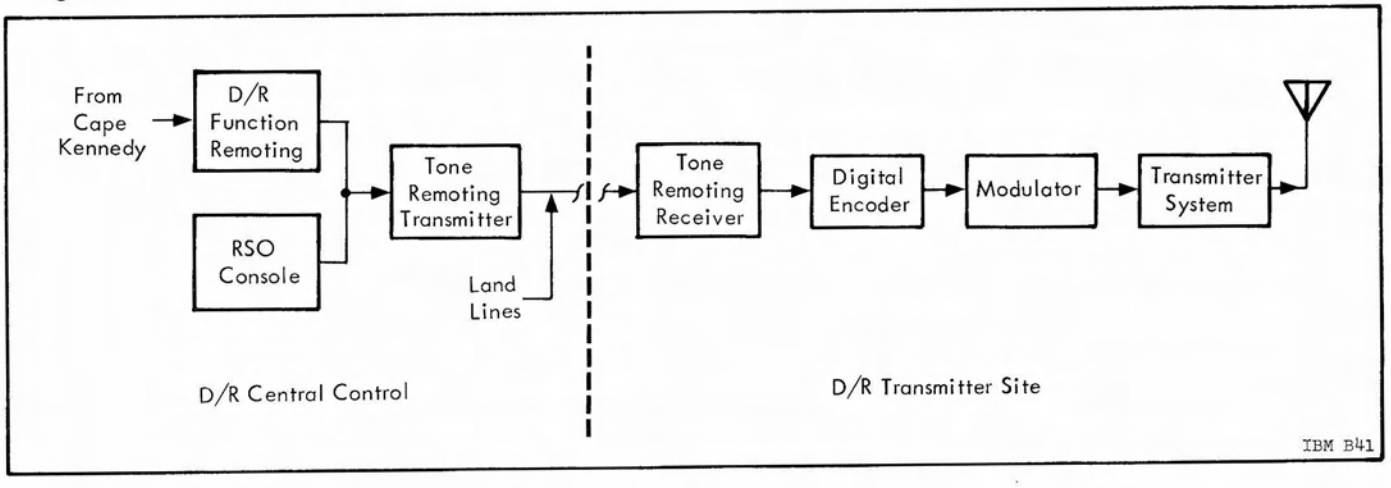


Figure 6.3-3 Downrange Station

RECEIVER

The command signal from the ground station is received in the vehicle with the MCR-503 Receiver. The same type of receiver is used also in the Instrument Unit command system and is described in Section 6. 2.

DECODER

A logic diagram of the vehicle-borne decoder is illustrated in Figure 6. 3-5. The front end consists of the filter driver, optimum decision circuitry, seven tone filters, and seven threshold detectors. The optimum decision circuitry will be discussed in more detail later, but operationally, the circuit can be considered as a hybrid, fast-acting AGC circuit. The purpose of each filter is to detect a particular tone, and the purpose of the threshold detectors is to establish the decision level and to amplitude standardize the output of each filter into a well-shaped pulse suitable for use in the circuitry which follows.

- The AND matrix consists of 21 AND gates and interconnections to the input of the code plug. The purpose of the matrix is to form the main alphabet of characters from the sub-alphabet of symbols (tones).

- The code plug consists of a multi-pin plug wired in the chosen code-of-the-mission configuration. The code plug can be wired in a number of unique ways. The purpose of the code plug is to unscramble the code and apply the 9 address character outputs to the sequence register. A second purpose of the plug is to present the 12 unused characters to OR 1.

- The sequence register or address memory consists of: (1) eight electronic switches (SW1 through SW 8), (2) one delay element consisting of a monostable multivibrator (DELAY MVB 1) and a trailing-edge differentiator, and (3) eight AND gates with inhibiting inputs (AND 1 through AND 8). In general, the purpose of the sequence register is to provide a pulsed signal to the input of AND 9 if each of the 9 characters of the address word is received in the proper sequence. A second function of the register is to provide a pulsed signal (up to eight) to the input of OR 1 if one or more characters are received out of sequence. The register will not provide a signal to the input of OR 1 if a character is repeated, which is desirable since radar blanking could cause a friendly character to be interrupted. The purpose of the eight passive time-delay elements (τ) in the register is to prevent an unfriendly intruder from gaining any advantage by transmitting more than 2 tones simultaneously. If 3 tones are transmitted, 3 characters will be formed. Because of the short time delay introduced by (τ), 2 of the 3 characters will be recognized as being out of sequence, even if they have the correct tone coding.

- The false-character action circuit consists of OR 1, OR 3, CLEAR MVB, FF 9, and AND 9. The purpose of this circuit is to provide a pulse whenever, (1) one of the unused characters is received, or (2) a character is received out of sequence. The pulse appears at the output of OR 1 and is routed to 3 places. First, it triggers FF 9 to its set state, which inhibits AND 9 so that the ENABLE MVB cannot be turned ON for the duration of the message interval, regardless of what occurs elsewhere in the decoder. Second, it passes through OR3 and clears (resets) the sequence register. A third action also to be initiated, provided that the character corresponding to point A has not yet occurred, is the triggering of the interval timer (a monostable multivibrator).

- The interval timing circuit consists of OR 2, the interval timer multivibrator, and a differentiating circuit which produces a pulse at the end of the timed interval. This pulse resets all decoder circuitry to the proper condition for receiving another message. Note that the presence of any of the 21 possible characters will initiate the timer. The purpose of OR 2 is to allow either the first character (point A) or any of the other 20 characters (the output of OR 1) to initiate the timer. The function of OR 6 and AND 16 is to establish a fixed recovery time for the interval timer MVB.

- The enabling circuit consists of DELAY MVB 2, the ENABLE MVB, and the power switch. The purpose of this circuit is to

prevent the function relays from being activated until after the address has been verified and the 11th character has arrived. Only when the 9 address characters have been sent in accordance with the chosen code, will a pulse appear at the input of AND 9, find it uninhibited, and trigger DELAY MVB 2. When this multivibrator completes its cycle, the -d/dt circuit triggers the ENABLE MVB ON for the function interval. The "ON" state of the ENABLE MVB closes the power switch, thus providing power to the function relays and associated logic circuitry.

- The decoding inhibit circuit consists of OR 4, OR 5, and AND 15. In general, the purpose of this circuit is to prevent decoding during the "clear" interval of the sequence register. The circuit does not function during the reception of a friendly message and therefore will not be discussed further.

- The function relays and logic circuitry represent the remainder of the decoder. The purpose of this circuitry is to allow the proper command transmission to close the appropriate relay(s), which supplies 28-volt power to the desired output functions.

- Signal tracing a friendly message. The code jack (Figure 6.3-5) has 21 inputs and 9 address outputs. For purposes of analysis, assume that the code plug is wired as shown in Figure 6.3-4 (top).

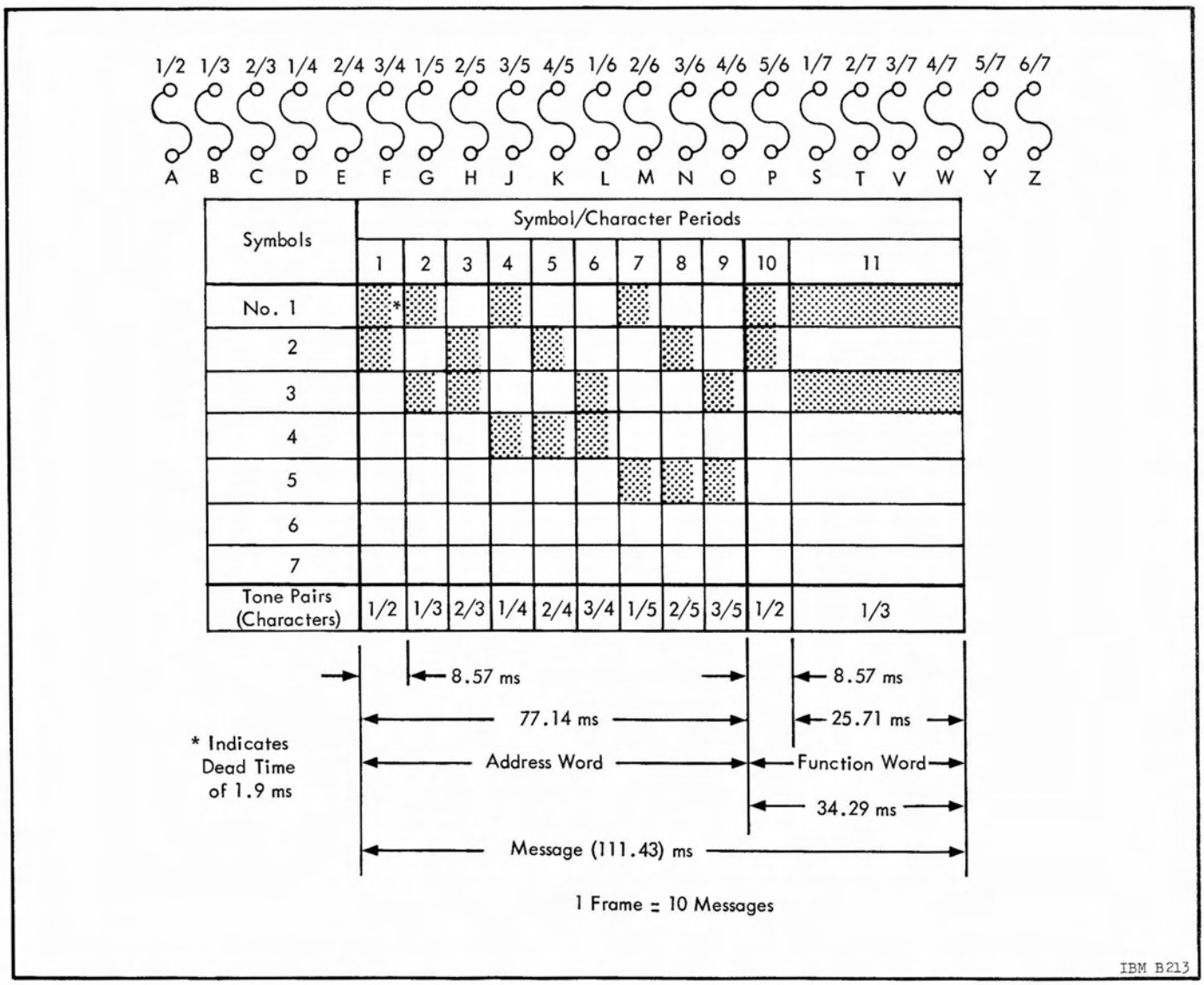


Figure 6.3-4 Code Plug Wiring

Based on such a code-plug wiring and on the message format previously mentioned, the total transmitted message will appear as shown in Figure 6.3-4 (bottom) if a command is to be effected. (The command is assumed to be destruct.)

The demodulated composite audio signal corresponding to the chosen tone pairs is fed from the receiver to the seven tone filters in the decoder. The filter outputs are matrixed to the 21 AND gates, thus providing the 21 required combinations. The outputs of the 21 AND gates are wired to a connector that feeds the input of the removable code plug. Assuming the code-plug wiring shown in Figure 6.3-4, the first tone pair (1 and 2) will cause a pulsed signal to appear on the output side of the code plug at point A. The signal at point A is distributed to 2 points: (1) it turns ON[1] the first electronic switch (SW 1) in the sequence register, which in turn supplies a voltage to the inhibiting input of AND 1; and (2) it passes through OR 2 and AND 16 and turns ON the interval timer. Approximately 8.5 milliseconds after the start of the first character, the second character arrives. Tone pair 1 and 3 corresponds to point B, and a pulsed signal at this point is distributed to 2 places: (1) it is applied as a signal input to AND 1, but cannot pass through because of the presence of the inhibiting voltage from SW 1; and (2) it turns ON SW 2. In addition, the output of SW 2 supplies a voltage to the inhibiting input of AND 2.

The third through the eighth characters (C through H) create results analogous to those of A and B. When the ninth-character pulse arrives (point J), it triggers DELAY MVB 1 to its "ON" state. When the multivibrator completes its cycle, the -d/dt circuit applies a pulse to AND 9. Since the interval timer is in its "ON" state and FF 9 is in the "reset" state, AND 9 will not be inhibited. Thus this pulsed signal will be allowed to pass through and trigger DELAY MVB 2 to its "ON" state. Eight and five tenths milliseconds later, the ENABLE MVB will be triggered to its "ON" state. Note that at no time during the address word is there an output from OR 1. This is because the address is the correct address and an output from OR1 will occur only if the address is not correct. After the ninth-character pulse turns ON the ENABLE MVB, the voltage thus obtained is (1) used to turn ON the power switch, which in turn supplies 28-volt power to the relay armatures, and (2) used as the supply voltage input to SW 10 and SW 11. Since we have assumed a destruct command, the tenth-character pulse will be formed by tone pair 1 and 2. This pulse will turn ON SW 10. The output of SW 10 is applied as a control voltage input to AND 10. Note that even though the time period of the tenth character is over, neither of the 2 relays is as yet energized. When the eleventh-character pulse arrives, it passes through AND 10 and is used to turn ON SW 11, thus energizing both relays in the destruct channel. Since both relays are now closed, 28 volts will be applied to the appropriate pin of the output plug and routed out of the decoder to the range safety system controller, which then takes over and initiates the destruct action and any preliminary critical functions (such as payload jettison, if applicable). As soon as the ENABLE MVB completes its cycle, the power switch will turn OFF, thus turning OFF SW 10 and SW 11. A short time later, the interval timer will complete its cycle, and the -d/dt circuits will reset all decoder circuitry to the proper state.

Much attention has been given to preventing execution of a catastrophic command should one component (transistor, relay, etc.) fail during flight. In many cases of component failure, the decoder design will still allow reliable interrogation.

The purpose of the DELAY MVB 2 is to delay the triggering of the ENABLE MVB for 8.5 milliseconds. This is necessary if complete freedom of choice for the ninth-character coding is to be maintained, for observe what would happen if the ninth, tenth, and eleventh characters were coded as follows (assuming that DELAY MVB 2 was not present):

9th	10th	11th
5 and 6	1 and 2	1 and 3

Destruct command

Since the ninth character corresponds to the first function-character of the safe command, and since the ENABLE MVB would be turned ON upon recognition of the ninth character, SW 14 would turn ON. This would degrade reliability and increase the probability of a command translation, since the intended command is destruct. Delaying the turn-ON of the ENABLE MVB until the time period of the ninth character is over, solves the problem without restricting the choice of the ninth character coding to one of the codes not used for a tenth character.

[1] Each electronic switch in the sequence register assumes the OFF state when B+ is removed. Therefore, when the decoder is first turned ON, all switches are OFF.

CLOSED-LOOP CHECKOUT

Until such time that a full security requirement is placed on flights of the Saturn Vehicle, the code-of-the-mission will be openly transmitted during the prelaunch countdown. This will be done to facilitate the pad checkout procedures.

If it is ever necessary to utilize the full security capabilities of the system, then a closed-loop prelaunch checkout procedure will be used in lieu of the open-loop transmission. In anticipation of such a requirement, a closed-loop procedure is being developed which will be compatible with the range procedure.

The characteristics of the Command Decoder are given in Table 6.3-2.

Table 6.3-2 Characteristics of the Command Decoder

Number of inputs	Two (isolated): receiver and hardwire
Type of input	Audio (75 ohms)
Audio input level	1 V rms per tone (1.4 V rms per tone pair)
Input dymanic range	At least 12 db (0.56 V rms to 2.2 V rms)
Sensitivity	Approximately 0.2 V rms at room temperature
Number of command outputs	Five
Type of output	Switched +28 Vdc rated 2 amperes (resistive) each output
Duration of output	Approximately 25 milliseconds
Type of code plug	Quick disconnect (Deutch)
Weight	2.1 kg (4.6 lbs)
Power	
Quiescent	2.5 watts (no audio input)
Operating	3 watts
Input voltage	+24 to +38 Vdc
Outline Dimensions	
Height	6.1 cm (2-3/8 in.)
Width	20.5 cm (8-1/16 in.)
Depth	11.7 cm (4-9/16 in.)

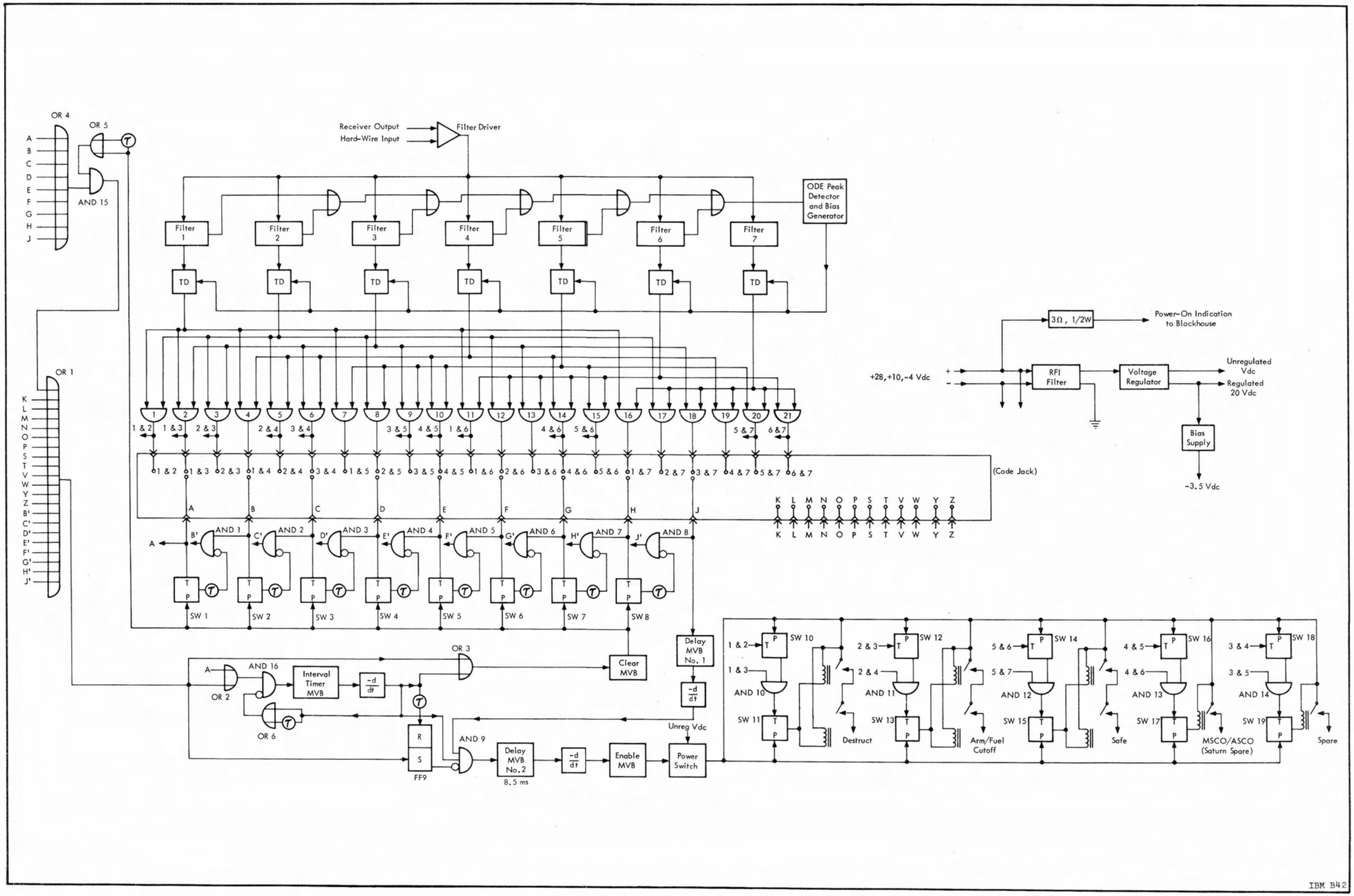


Figure 6.3-5 Secure Range Safety Decoder Simplified Logic Diagram

SECTION 6.4

SATURN COMMAND AND COMMUNICATION SYSTEM (SCCS)

(To be supplied at a later date)

SECTION 6.5

RANGE SAFETY COMMAND SYSTEM (AN/DRW-13)

An overall diagram of the range safety command-destruct system is shown in Figure 6.5-1. The ground portion of the system is the responsibility of the Atlantic Missile Range (USAF). The three range safety commands applicable to Saturn flights are:

- ARM/ FUEL CUTOFF - Arming of the exploding bridge wire and thrust termination.
- DESTRUCT - Firing of the exploding bridge wire. (Propellant Dispersion Command)
- SAFE - Disconnecting the command decoding equipment from the battery.

The commands are originated by a range safety officer who monitors the vehicle's powered flight with the help of tracking equipment. In order to keep the FM receiver "captured" during flight, the vehicle is constantly illuminated by an RF carrier until the last command is transmitted. This is accomplished by transmitters at several downrange stations when the vehicle is beyond the radio horizon of the Kennedy Space Center. The commands are transmitted by frequency modulating the command transmitters (at the launch site and downrange stations) with selected combinations of audio tones.

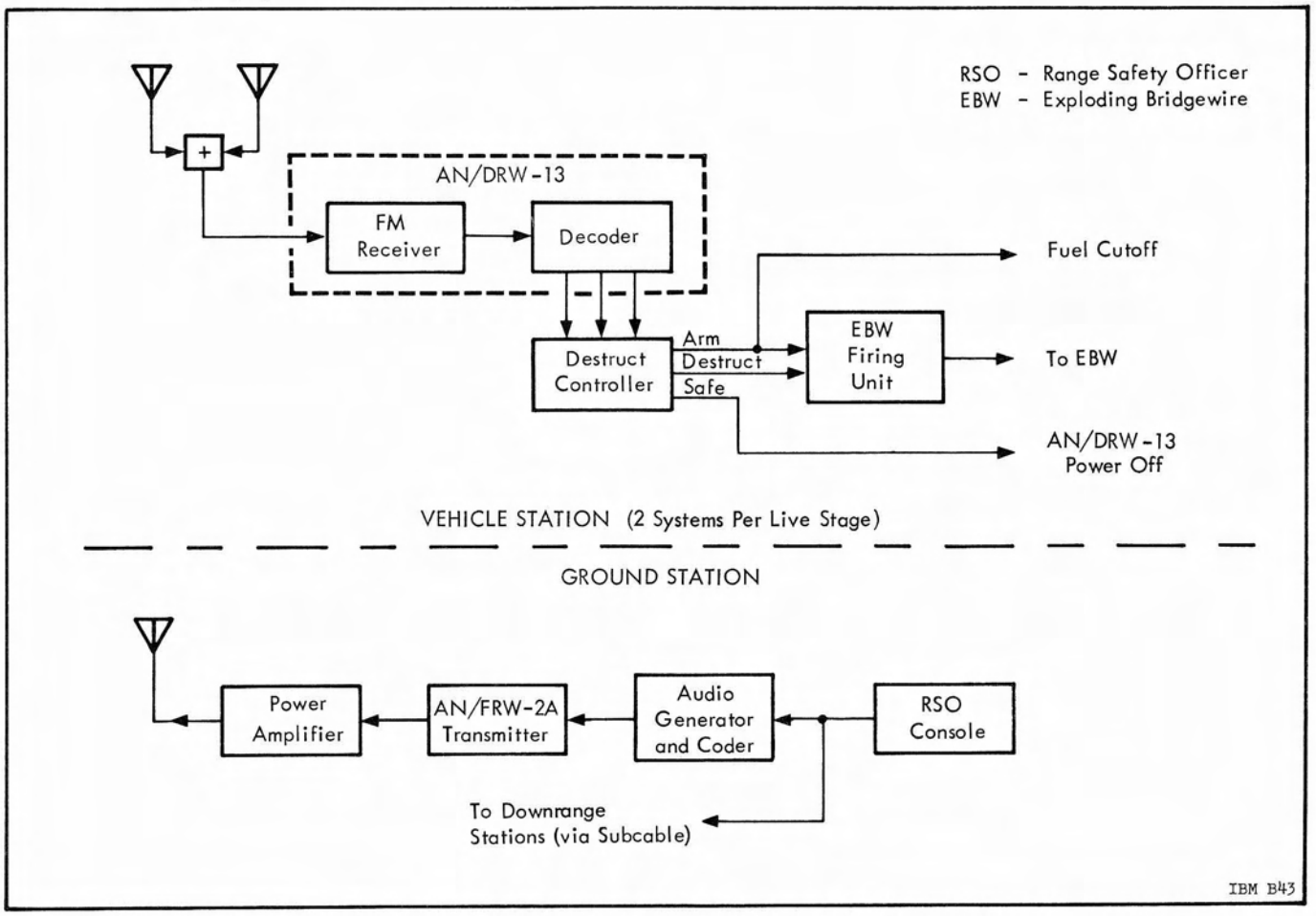


Figure 6.5-1 Range Safety Command System

The RF carrier is generated by the AN/FRW-2A Transmitter whose usable modulation bandwidth is from 600 Hz to 80 kHz. This audio-frequency baseband has been divided into 20 channels known as inter-range instrumentation group channels. The spacing of the channels is such that second harmonics of a given channel will fall outside the bandwidth of any of the other channels, thus minimizing interference. The baseband spectrum, with the center frequencies of the 20 inter-range instrumentation group channels designated, is shown in Figure 6.5-2. Although all 20 channels are available for range safety use, the actual practice has been to use only the lower baseband frequencies for range safety and to reserve the remainder of the baseband for other uses.

On most vehicles launched thus far, range safety has utilized only three of the reserved tone channels (channels 1, 2, and 5) although the Saturn program now uses channels 6 and 7 for a command system SAFE function (deactivation). To provide some insurance against noise or transient RF pulses accidentally triggering a function, 2 tones are always transmitted simultaneously. Thus, two audio tones are required to compose one command signal.

Range safety commands have priority over all other users of the AN/FRW-2A baseband; therefore all other users are automatically silenced during transmission of a range safety command.

The carrier frequency of the AN/FRW-2A Transmitter is frequency-modulated by the two simultaneous inter-range instrumentation group tones, and the resultant signal is transmitted to the vehicle. The transmitter frequency can be set anywhere between 406 MHz to 550 MHz, although the antennas presently used limit the high end to a 500 MHz capability. The effective radiated power of the system is over 100 kW.

The antenna system on the vehicle receives the RF signals and channels them to the Command Receiver. Saturn Vehicles use the AN/DRW-13 Command Receiver. Figure 6.5-3 is a simplified block diagram of this receiver. The audio tones representing the command are recovered by demodulation of the received RF carrier. The tones are applied to bandpass filters which detect whether a particular tone is present. Each filter output is applied to the coil of a relay which is energized only when the filter output detects a tone. The contacts of the relays are wired so that only the two correct simultaneous tones will complete the series circuit and perform the desired range safety function.

The AN/DRW-13 is a dual-conversion FM receiver with ten audio channels, each channel (filter) tuned to a different tone frequency in the modulation bandwidth of the transmitter. Characteristic data of the receiver is given in Table 6.5-1.

Table 6.5-1 Range Safety Command Receiver/ Decoder (AN/DRW-13) Characteristics

Frequency range	405 to 450 MHz
Minimum sensitivity	5 mV
Power consumption	7 watts
Weight (receiver, decoder, and power supply)	1.24 kg (2.76 lbs)
Volume	0.017 meters^3 (1048 inches^3)

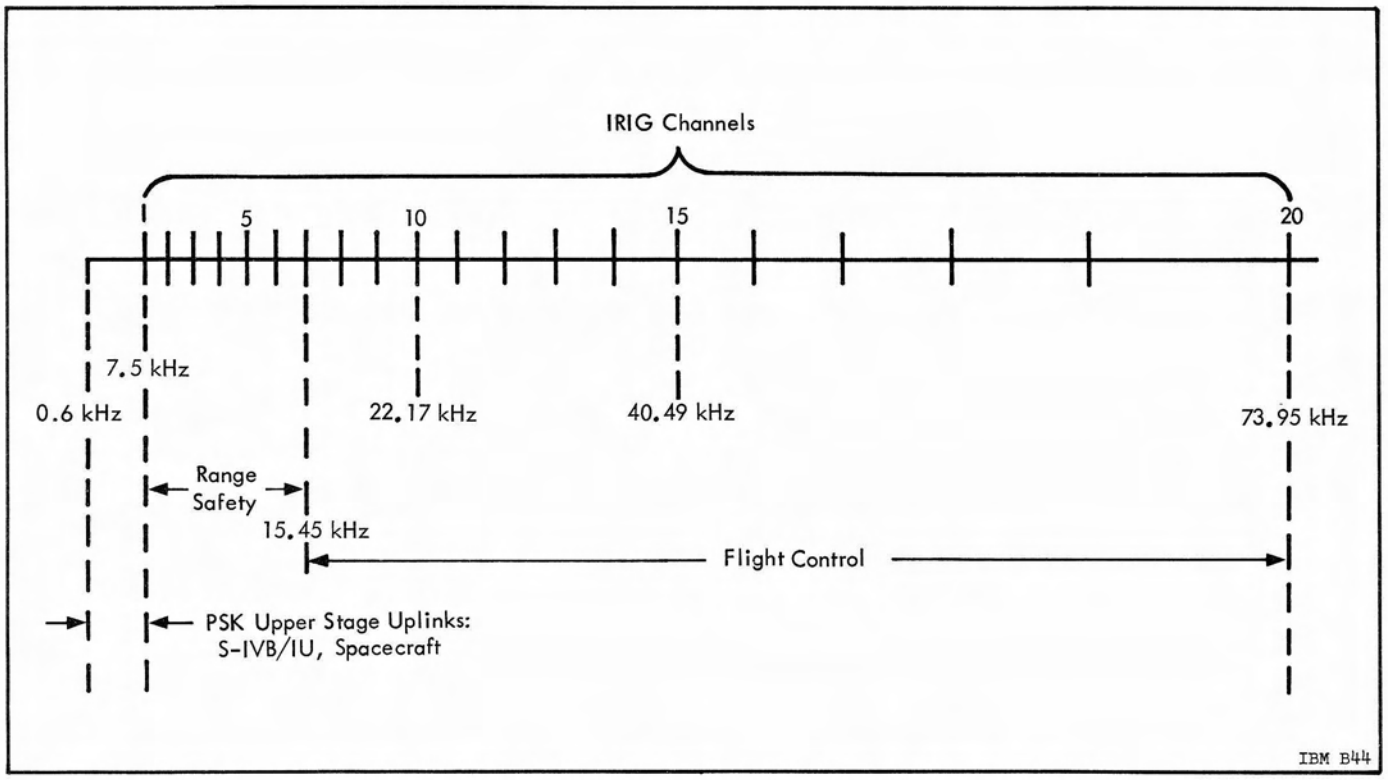


Figure 6.5-2 AN/FRW-2A Modulation Bandwidth Usage

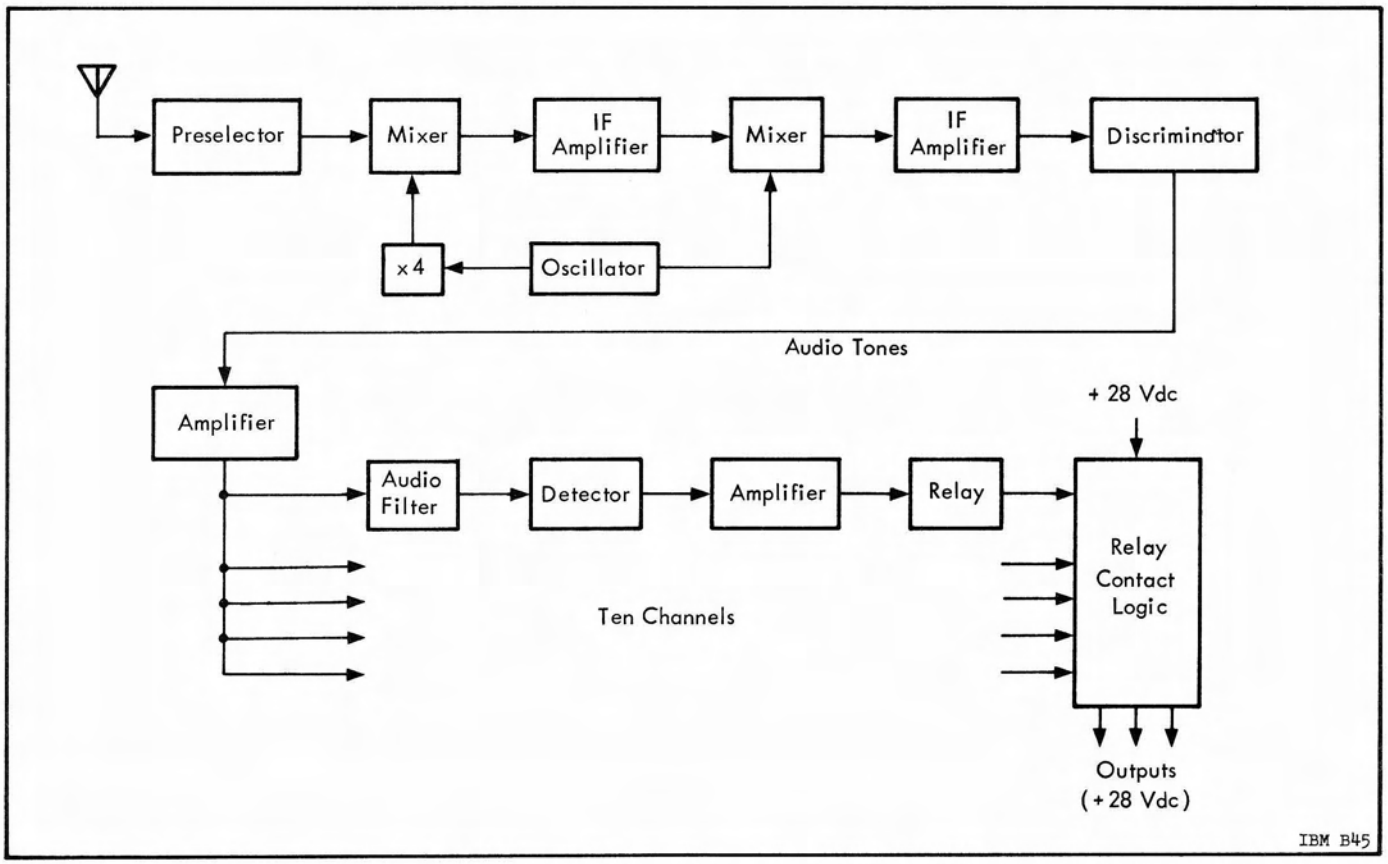


Figure 6.5-3 AN/DRW-13 Receiver/Decoder

CHAPTER 7

TRACKING SYSTEMS

TABLE OF CONTENTS

SECTION 7.1

SATURN TRACKING INSTRUMENTATION

The purpose of radio tracking is the determination of the vehicle's trajectory. Tracking data is used for mission control, range safety, and post-flight evaluation of vehicle performance.

The Saturn vehicles carry several tracking transponders as listed in Table 7.1-1. A combination of tracking data from different tracking systems provides the best possible trajectory information and increased reliability through redundant data. The tracking of the Saturn Launch Vehicle may be divided into 4 phases: (1) powered flight into earth orbit, (2) orbital flight, (3) injection into translunar trajectory, and (4) coast flight after injection.

Continuous tracking is required during powered flight into earth orbit. Because of the long burning time (700 seconds) of the 3-stage Saturn V Launch Vehicle, the end of the powered flight phase cannot be covered sufficiently from land-based tracking stations. Therefore, a tracking ship will be located in the Atlantic to obtain the very important tracking data during insertion which is required for orbit determination. Figure 7.1-1 shows tracking stations used during the powered flight into earth orbit. The number of stations which can "see" the vehicle depends on the launch azimuth. Station visibilities are indicated in Figure 7.1-2 for launch azimuths of 72.5 degrees and 105 degrees. Accuracy of position and velocity measurements obtained from combined tracking information are shown in Figure 7.1-3. Both Figures 7.1-2 and 7.1-3, are based on a typical Saturn V powered flight trajectory.

In addition, the Saturn Launch Vehicle will be tracked from S-band stations at Cape Kennedy and on the Atlantic tracking ship. These stations have dual tracking capability; i.e., they can simultaneously track the two S-band transponders on the vehicle (one in the IU and the other in the Apollo Spacecraft). The S-band station on Bermuda has only a single capability and will track the Apollo Spacecraft transponder.

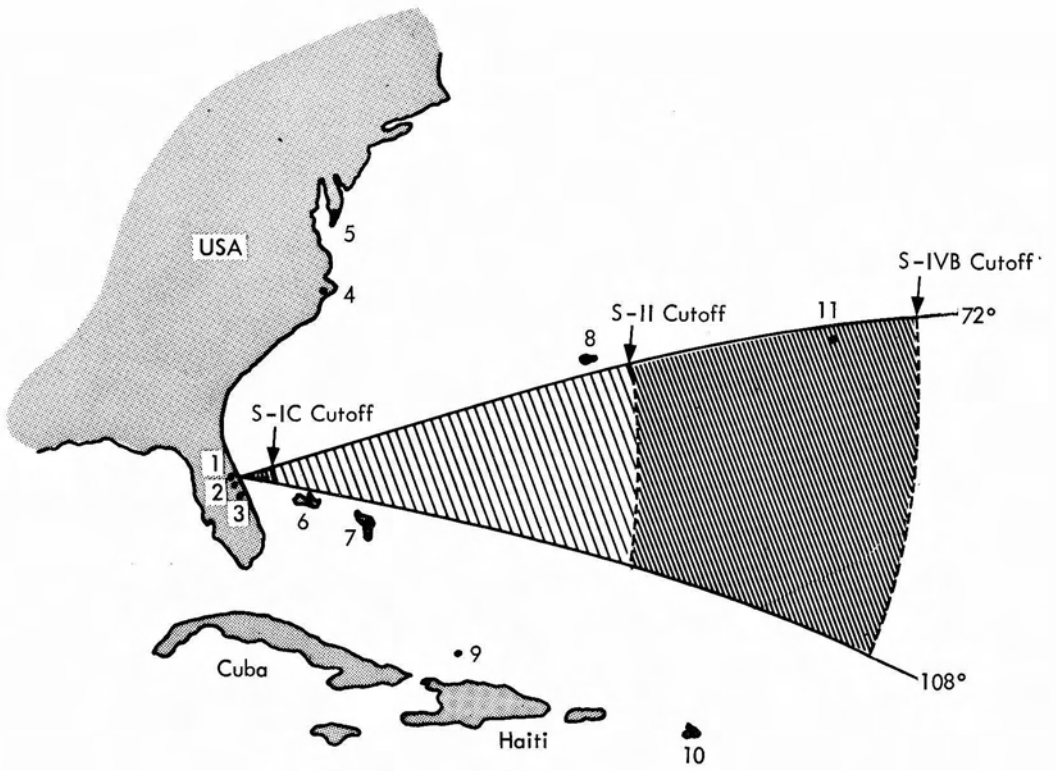
During orbital flight, tracking is accomplished by S-band stations of the Manned Space Flight Network and by C-band radar stations listed in Table 7.1-2. The S-band stations, including the Deep Space Instrumentation Facility, can track the Apollo Spacecraft to the moon and will also be involved in tracking after injection. Tracking information collected during orbital flight may be used to update the Saturn guidance system before injection.

In addition to land-based stations, five tracking ships, equipped with C-band radar, and S-band stations, will be available. One of these ships will be used for insertion tracking in the Atlantic.

Tracking requirements for the launch vehicle during second burn of the S-IVB Stage and during the flight period following injection have not been completely defined. Stations listed in Table 7.1-2 will participate in this operation. The DSIF and MSFN stations have essentially the same capabilities. All S-band tracking stations will be equipped for reception of PCM telemetry at VHF and UHF.

Table 7.1-1 Saturn Tracking Instrumentation

Tracking System	Transponder Location	
	Saturn IB	Saturn V
S-band	-	IU
C-band radar (2)	IU	IU
AZUSA/GLOTRAC	IU	IU
ODOP	S-IB Stage	S-IC Stage



Number	Location	Tracking System
1.	Cape Kennedy, Florida	C-Band Radar ODOP AZUSA/GLOTRAC
2.	Patrick, Florida	C-Band Radar
3.	Valkaria, Florida	(Not used presently for Saturn tracking)
4.	Cherry Point, North Carolina	GLOTRAC Receiver
5.	Wallops Island, Virginia	C-Band Radar
6.	Grand Bahama Island	C-Band Radar AZUSA
7.	Eleuthera Island	GLOTRACK Receiver
8.	Bermuda Island	C-Band Radar GLOTRAC Transmitter & Receiver
9.	Grand Turk Island	C-Band Radar GLOTRAC Receiver
10.	Antigua	C-Band Radar GLOTRAC Transmitter & Receiver
11.	Atlantic Ship (Position depends on launch azimuth)	C-Band Radar

IBM B73

Figure 7. 1-1 Launch Phase Tracking Stations

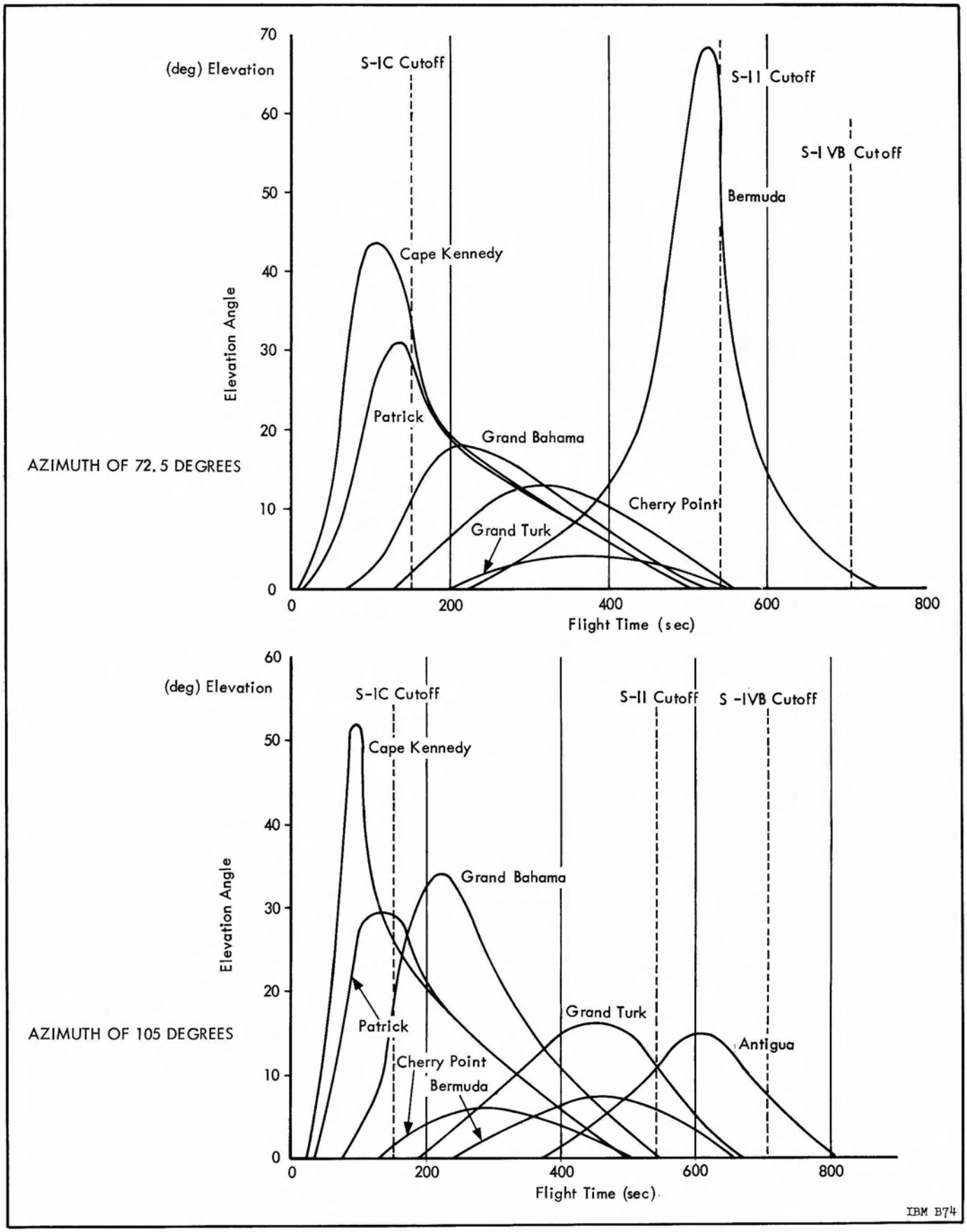


Figure 7.1-2 Station Visibility for Saturn V Powered Flight

Table 7.1-2 Orbital Tracking Stations

Name and Location	S-Band Tracking Single Dual	Ant. Dia		C-Band Radar
Cape Kennedy, Florida	D	9.2 m	MSFN	X
Bermuda	S	"	"	X
Antigua Island	S	"	"	X
Canary Island	S	"	"	X
Ascension Island	D	"	"	X
Canarvon, Australia	D	"	"	X
Hawaii, USA	D	"	"	X
Guaymas, Mexico	S	"	"	
Wallops Island, USA	D	"	"	
Guam	D	"	"	
Texas Station, USA	S	"	"	
Canberra, Australia	D	26 m	DSIF/ JPL	
Goldstone, USA	D	"	"	
Madrid, Spain	D	"	"	
Goldstone, USA	D	"	MSFN	
Madrid, Spain	D	"	"	
Canberra, Australia	D	"	"	
Point Aguello, USA				X
White Sands, USA				X
1 Ship (Atlantic)	D			X
4 Ships	S			X

9.2 m = 30 ft 26 m = 85 ft

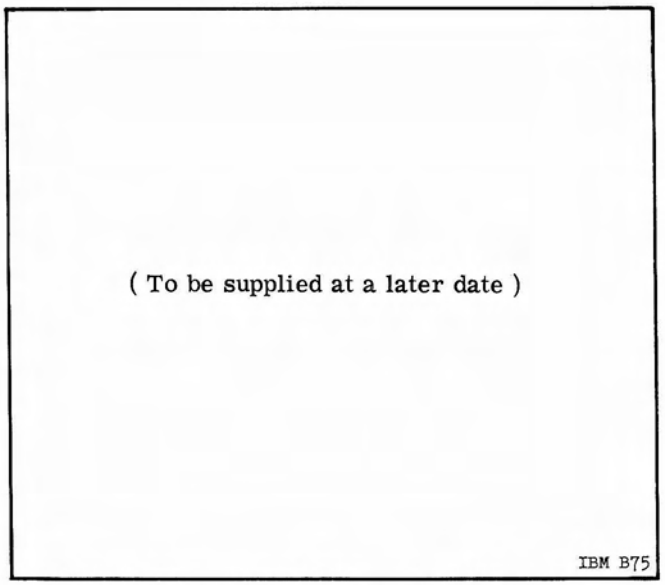


Figure 7.1-3 Accuracy of Position and Velocity Measurements

SECTION 7.2

C-BAND RADAR

The function of the C-Band Radar Transponder (Model SST-135C) is to increase the range and accuracy of the radar ground stations equipped with AN/FPS-16, and AN/FPQ-6 Radar Systems. C-band radar stations at the Kennedy Space Center, along the Atlantic Missile Range, and at many other locations around the world, provide global tracking capabilities. Beginning with Vehicles 204 and 501 two C-band radar transponders will be carried in the IU to provide radar tracking capabilities independent of the vehicle attitude. This arrangement is more reliable than the antenna switching circuits necessary if only one transponder would be used.

The transponder receives coded or single pulse interrogation from ground stations and transmits a single-pulse reply in the same frequency band. A block diagram of the transponder is shown in Figure 7.2-1. A common antenna is used for receiving and transmitting. The transponder consists of five functional systems: superheterodyne receiver, decoder, modulator, transmitter, and power supply. The duplexer (a 4-part ferromagnetic circulator) provides isolation between receiver and transmitter. Interrogating pulses are directed from the antenna to the receiver, and reply pulses are directed from the transmitter to the antenna. The preselector, consisting of three coaxial cavaties, attenuates all RF signals outside the receiving band. The received signal is heterodyned to a 50 MHz intermediate frequency in the mixer and amplified in the IF amplifier which also contains the detector. In case of coded transmission, the decoder module provides a pulse output only if the correct spacing exists between pulse pairs received. The shaped-pulse output of the decoder is directed to the modulator which converts it into a high-power, precisely-shaped and precisely delayed pulse which is applied to the magnetron to produce the reply pulse. Six telemetry outputs are provided: input signal level, input PRF, temperature, incident power, reflected power, and reply PRF.

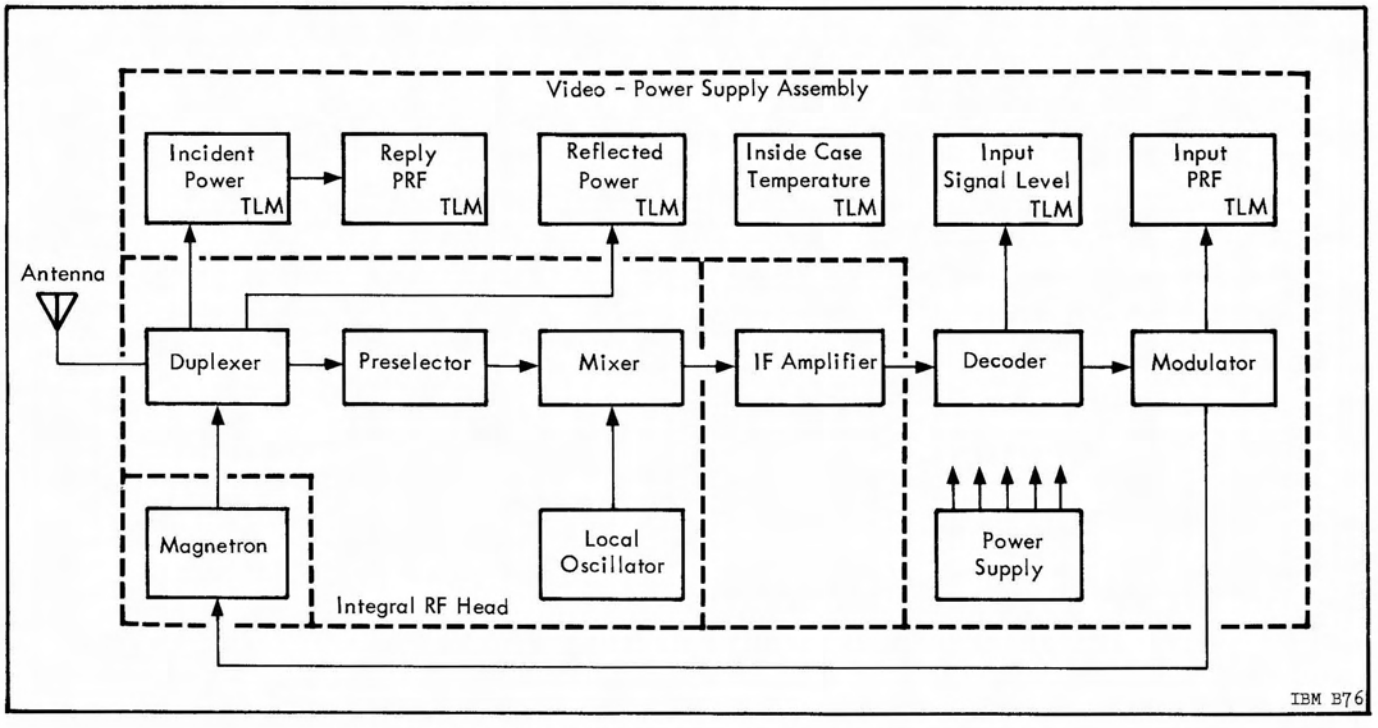


Figure 7.2-1 SST-135C Transponder System Block Diagram

Semiconductors are used in all circuitry, with the exception of the local oscillator and magnetron. The characteristics of the transponder are given in Table 7.2-1.

The radar ground stations determine the position of the vehicle C-band transponder by measuring range, azimuth angle, and elevation angle. Range is derived from pulse travel time, and angle tracking is accomplished by amplitude-comparison monopulse techniques. As many as four radar stations may track the beacon simultaneously. Some data about the AN/FPS-16 and AN/FPQ-6 radar is listed in Table 7.2-2.

Table 7.2-2 Radar Ground Station Characteristics

	AN/FPS-16	AN/FPQ-6
Frequency band (MHz) . .	5400-5900	5400-5900
Peak power (mw)	1.3	3.0
Antenna size (meters). . . .	3.9	9.2
Antenna gain (db)	47	52
Receiver noise figure (db) .	6.5	8
Angle precision (units) . . .	0.15	0.1
Range precision (meters). .	4.5	3.0

Table 7.2-1 C-Band Radar Transponder, Model SST-135C

Receiver Characteristics	
Frequency (tunable externally)	5400 to 5900 MHz (set to 5690 ±2 MHz)
Frequency stability	± 2.0 MHz
Bandwidth (3 db)	10 MHz
Off-frequency rejection	50 db image; 80 db minimum, 0.15 to 10,000 MHz
Sensitivity (99% reply)	-65 dbm over entire frequency range and all environments
Maximum input signal	+20 dbm
Interrogation code	Single or double pulse
Pulse width	0.2 to 5.0 us (single pulse), 0.2 to 1.0 us (double pulse)
Pulse spacing	Continuously settable between 5 and 12 us (set to 8 ±0.05 us)
Decoder limits	±0.25 us accept, ±0.85 us reject (5 to 12 us)
Transmitter Characteristics	
Frequency (tunable externally)	5400 to 5900 MHz (set to 5765 ± 2 MHz)
Peak power output	400 watts minimum, 700 watts nominal
Pulse width	1.0 ± 0.1 us
Pulse jitter	0.020 us maximum for signals above -55 dbm
Pulse rise time (10% to 90%)	0.1 us maximum
Duty cycle	0.002 maximum
VSWR of load	1.5 : 1 maximum
Pulse repetition rate	10 to 2000 pps; overinterrogation protection allows interrogation at much higher rates with count-down; replies during overinterrogation meet all requirements
Transponder Characteristics	
Recovery time	50 us single pulse, 62 us double pulse maximum for input signal levels differing by up to 65 db (recovers to full sensitivity with no change in transmitter reply power or frequency with multiple radars interrogating simultaneously)
Fixed delay	Settable 2 ± 0.1 and 3.0 to 0.01 us (set to 3.0 ± 0.01 us)
Delay variation with signal level	50 nanoseconds maximum from -65 dbm to 0 dbm
Power requirements	24 to 30 volts
Primary current drain	0.7 ampere standby; 0.9 ampere at 1000 pps
Weight	2.5 kg (5.5 lbs)

SECTION 7.3

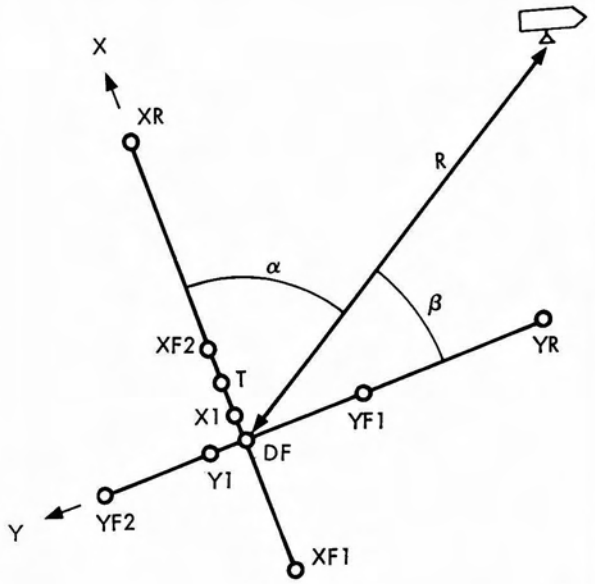
AZUSA/GLOTRAC

7.3.1 AZUSA

AZUSA is an interferometer tracking system which determines the position of a vehicle-borne transponder. Two AZUSA stations are in operation, one station (MK II) at Cape Kennedy and the other station (MK I) at Grand Bahama Island. The AZUSA system provides real-time tracking data used for range safety impact prediction and post flight trajectory analysis. AZUSA stations cover only a portion of the Saturn V powered flight trajectory.

The position of the vehicle (transponder) is determined at the AZUSA ground stations by measuring range (R) and two direction cosines (l, m) with respect to the antenna baselines. The antenna layout of the AZUSA MK II station, shown in Figure 7. 3-1, consists of two crossed baselines (at right angle) with three antenna pairs each. The transmitter antenna (T) radiates a CW signal at 5 GHz to the vehicle. This signal is offset by 60 MHz in the transponder and retransmitted to the ground station receiving antennas. The direction cosine, with respect to a baseline, is obtained from the measurement of the phase difference between signals received at spaced antenna pairs along this baseline. The range to the transponder is found by measuring the phase difference between transmitted and received signal. For range ambiguity resolution, the transmitted carrier is modulated with several low frequencies.

Direction cosine measurement is accomplished by using the antennas in pairs to provide baselines of 5 meters, 50 meters, and 500 meters as indicated in the table of Figure 7. 3-1. A conical scan antenna (DF) yields unambiguous direction measurement and furnishes ambiguity resolution for the 5-meter baselines. The 5-meter baselines resolve ambiguity for the more accurate 50-meter baselines, and the 500-meter baselines supply information for computing cosine rate data. The direction finder antenna DF (conical scan antenna) provides pointing information for all other antennas.



$$l = \cos\alpha = \frac{L_x}{R}$$

$$m = \cos\beta = \frac{L_y}{R}$$

T: Transmitter Antenna
DF: Direction Finder Antenna (Receiving)
XF, XR, YF, YR: Receiving Antennas
L: Distance between antennas

Antennas	Baseline Length L_x , L_y	Measurements
DF - X1	5 m	Intermediate cosα
XF1 - XF2	50 m	Fine cos α
XF1 - XR	500 m	Rate cos α
DF - Y1	5 m	Intermediate cosβ
YF2 - YF1	50 m	Fine cosβ
YF2 - YR	500 m	Rate cos β

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Figure 7. 3-1 AZUSA (MK II) Ground Station Layout

The signals received at the two spaced antennas of an antenna pair have a phase difference caused by the difference in range between the transponder and each of the antennas. This phase difference is measured and used to compute the direction cosine. The accuracy of the measurement increases with increasing baseline length, but data becomes ambiguous and coarse measurements are necessary for ambiguity resolution.

Range is determined at the ground station by comparing the instantaneous phase of the transmitted modulation signal to that of the received modulation signal. The resulting phase difference is directly proportional to the propagation time from the ground station to the transponder and back to the ground station. In other words, phase difference is proportional to range. Using a high range modulation frequency to obtain fine resolution, results in output data that are ambiguous, the number of ambiguities is proportional to the modulation frequency.

The ambiguities in range measurement are resolved by using three modulation frequencies that are obtained by the frequency division of a single, precise, frequency source at the ground station. The phase shift is measured for each one of these harmonically related frequencies. The lower frequency phase data is used to resolve the ambiguities in the next higher frequency phase data. This arrangement has, as advantages, the resolving power of the highest frequency signal and the extended unambiguous range data provided by the lower data frequency. The modulation signals used for range measurement are 157.4 Hz, 3.934 kHz, and 98.356 kHz. The fine range modulation signal, 98.356 kHz, remains ON at all times so the transponder can "lock-on" with the ground station. Higher resolution range data is obtained by coherent carrier phase comparison.

The coherent transponder includes a phase-control loop in which the 98.356 kHz fine range modulation frequency is multiplied by a factor of 612 to establish the transponder offset frequency (60.194 MHz) and a frequency and phase-coherent response signal (5000 MHz).

At the ground station, the 98.356 kHz frequency is also multiplied by 612 to equal the transponder offset frequency (60.194 MHz). Both, the 5000 MHz signal received from the transponder and the data signal, are heterodyned with a local oscillator signal to obtain approximately 5 MHz. Data and reference signals are then fed into a discriminator which provides one pulse (count) output for each 360-degree phase difference (1 cycle) in the input circuit. Plus and minus pulses are fed on separate lines to a bidirectional counter. The coherent carrier range data is then fed to an IBM 7090 Computer with the direction cosine data (l, m) and modulation-derived slant range data. The computer, using 20 input samples per second, solves the equations for the position of the vehicle.

AUTOMATIC FREQUENCY CONTROL LOOP

The AZUSA Type-C Transponder used in the Saturn Vehicles is a part of the overall AFC loop in the AZUSA system (Figure 7.3-2). Upon transponder activation, the klystron transmits a 5060.194 MHz signal which is swept ±2 MHz by a 15 Hz internal sweep generator. This enables the ground station and the transponder to find a common frequency so that lock-on can occur. When frequency lock-on occurs, the 5060.194 MHz signal transmitted by the ground station will be shifted slightly by AFC action so that, after the transponder receives the signal and retransmits it, the frequency received by the ground station receivers will be 5000 MHz. The 5060.194 MHz (plus Doppler) signal entering the transponder receiver is mixed with a fraction of the retransmitted signal to produce a 60.194 MHz offset frequency. A frequency discriminator is used to maintain the offset frequency within 30 Hz.

Phase lock between the transponder and ground station is established by multiplying the fine range modulation frequency (98.356 kHz) received from the ground station and using it as a reference for a phase discriminator. This phase discriminator has higher output gain than the frequency loop discriminator and holds the transponder offset frequency (60.194 MHz) correct to within a fraction of a cycle. The Type-C Transponder uses this combination frequency-phase discriminator to obtain maximum stability in both AFC and APC loops. This coherent condition in the transponder enables phase measurements to be made at the ground station between the received 5000 MHz signal and the 5060.194 MHz transmitted signal (heterodyned to 5000 MHz) to obtain high-resolution incremental range data. Similarly, phase comparison of the transmitted and received 98.356 kHz modulation signals produces non-ambiguous range data.

Before lock-on, the transmitter local AFC loop and the local over-all AFC loop are used to keep the ground station transmitter frequency at 5060.194 MHz. When the ground station and the transponder are frequency locked, a 5 MHz signal from the ground station range receiver IF amplifier controls the over-all AFC loop. This high-gain loop overrides both the local over-all AFC loop and the transmitter AFC loop

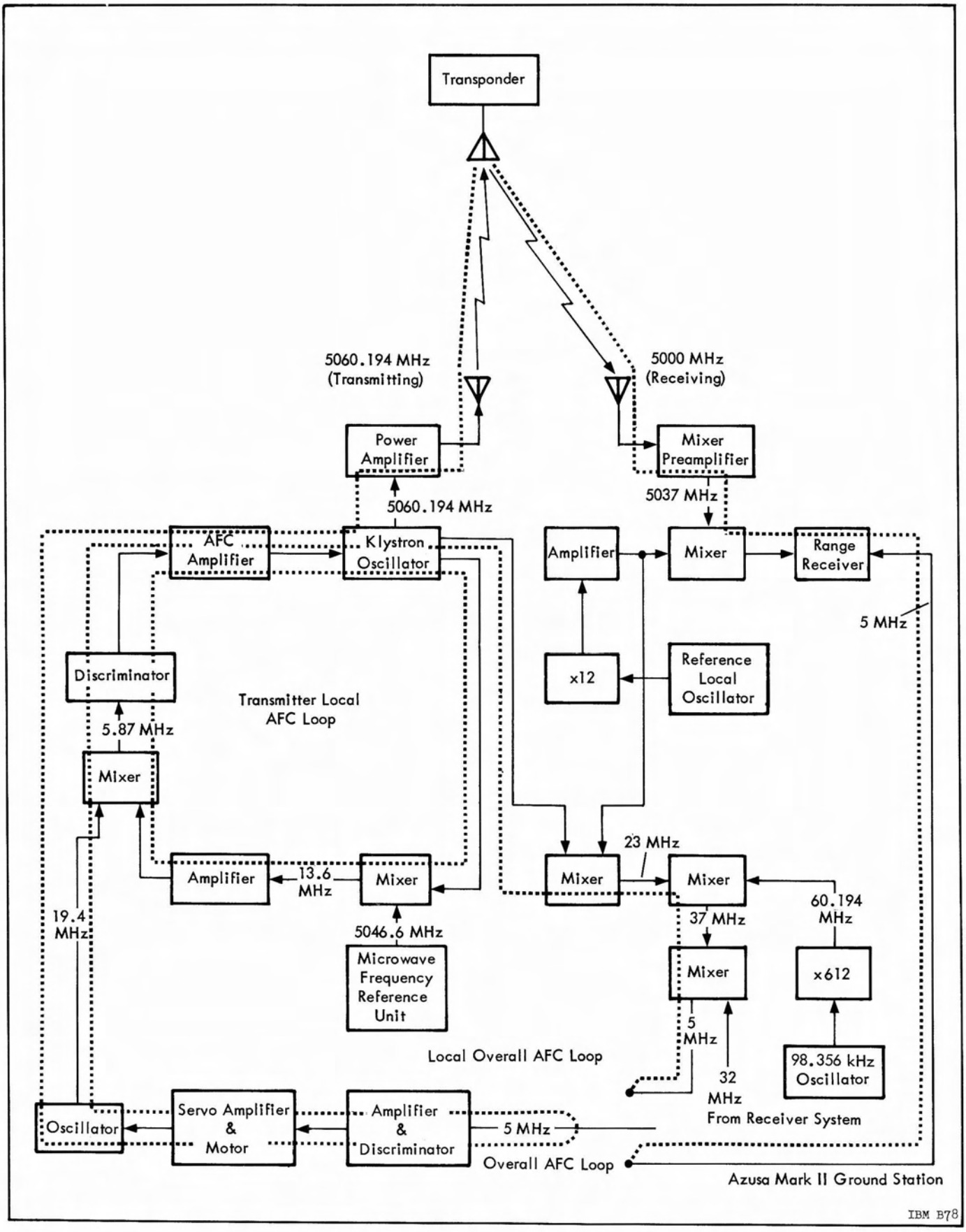

Figure 7.3-2 AFC Loops, Ground Station and Transponder

(Figure 7. 3-2). Should the return signal received from the transponder deviate from 5000 MHz at the ground station receiver, the ground station receiver will detect the error and cause the ground station transmitter frequency to shift slightly in a direction to correct the error (through AFC action). The transponder receiver detects the frequency or phase change and corrects the return frequency so that the offset frequency remains exactly 60. 194 MHz (through the transponder AFC and APC loops). Thus, the vehicle-to-ground link maintains a constant frequency (5000 MHz) at the ground station receivers despite systematic frequency drift and Doppler shift.

TRANSPONDER

In the transponder (Figure 7. 3-3), the 5060. 194 MHz interrogation signal and the 5000 MHz klystron local oscillator signal produce a 60. 194 MHz IF, or offset frequency, in the crystal mixer. This signal is mixed with a 55. 2 MHz second local oscillator signal. The second IF (4. 994 MHz) is amplified and fed to the receiver frequency discriminator where the range signals which modulate the ground station carrier are detected. This range modulation (98. 356 kHz) is fed to the compensation network. The 4. 994 MHz IF signal is also fed to the phase network and to one side of the frequency-phase discriminator.

A 4. 994 MHz reference signal for phase lock is provided as follows: The 98. 356 kHz range signal is directed through the compensation network, an amplifier, and two crystal filters, to a frequency multiplier circuit. Here the signal is multiplied to 60. 194 MHz. (One crystal filter is in the compensation network subassembly and one is in the sweep oscillator subassembly.) The 60. 194 MHz signal enters the phase network and is mixed with 55. 2 MHz from the receiver second local oscillator to obtain the 4. 994 MHz reference for the phase discriminator.

In the compensation network, the phase and frequency discriminator error voltage from the phase network overrides the output from the sweep oscillator. It is then combined with the 98. 356 kHz range modulation and fed to the modulator. In the modulator these signals are superimposed on the klystron anode voltage. The dc error signal maintains phase lock between the 5060. 194 MHz received signal and the 5000 MHz response signal. The 98. 356 kHz is used to modulate the response signal. The 98. 356 kHz phase shift in the transponder is held to an absolute minimum so that phase comparison of the received signal and transmitted signal at the ground station will indicate actual range to the transponder.

The waveguide subassembly is designed with two bandpass filters internally connected to a symmet-

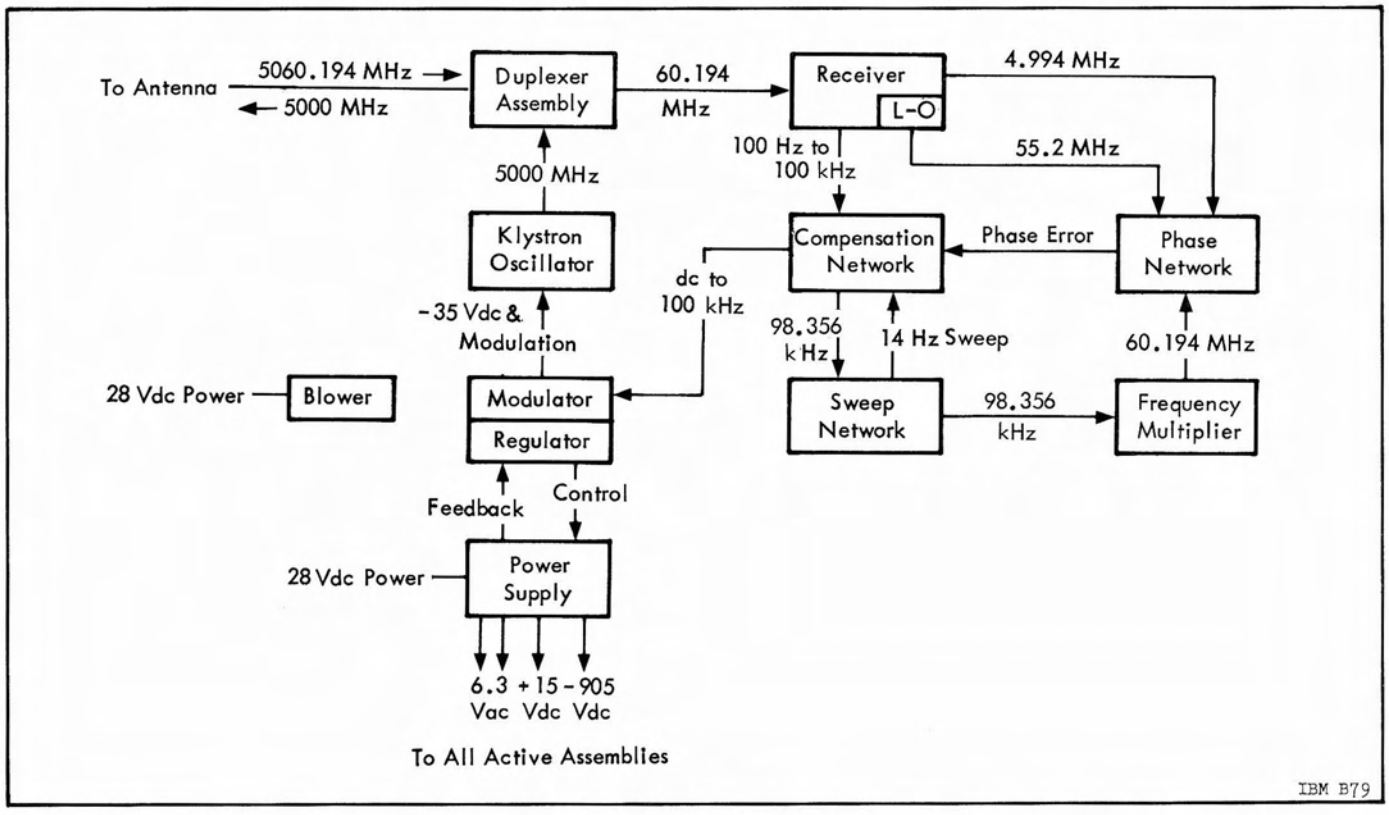

Figure 7. 3-3 AZUSA Transponder Block Diagram

rical Y section. This arrangement permits the use of a single receiving-transmitting antenna. The klystron output is carried to the 5000 MHz filter by coaxial cable. The signal passes through a 3-section filter, the symmetrical Y, and a waveguide-to-coaxial transition and is carried to the antenna by coaxial cable. A 5060.194 MHz signal entering the antenna passes through the same coaxial cable into the waveguide. A 2-section filter passes the incoming 5060.194 MHz signal and a small amount of the 5000 MHz signal present in the symmetrical Y to a crystal mixer which produces a 60.194 MHz offset frequency.

The Type-C Transponder uses transistors in all circuitry except for the klystron. The Type-C Transponder operates also with GLOTRAC stations described briefly in the following paragraphs. Table 7.3-1 lists the characteristics of the AZUSA system.

7.3.2 GLOTRAC

GLOTRAC (GLObal TRACking) was originally planned as a global tracking system, but changes in programs restricted the number of ground stations. GLOTRAC uses the AZUSA Type-C Transponder in the vehicle. GLOTRAC ground stations are equipped with either a transmitter or a receiver or both as indicated in Figure 7.1-1. Both existing AZUSA stations may be considered as part of GLOTRAC. The transponder in the vehicle is interrogated by an AZUSA ground station or by a GLOTRAC transmitter site. The transponder offsets the received frequency and retransmits the signal to GLOTRAC receiving sites where the Doppler shift is measured by comparing the received signal with the transmitter signal (if receiver is located near the transmitter) or with a local frequency source. The measured Doppler shift provides the range sum similar to ODOP (refer to Section 7.4). At GLOTRAC stations equipped with both a transmitter and receiver, the range to the transponder is measured by phase comparison between the transmitted and received signals. The AZUSA Type-C Transponder can also be interrogated by C-band radars for range and angle determination.

The range rates measured at three receiving stations yield the vehicle velocity, and by integrating this velocity, the position is obtained. Initial conditions for integration are obtained from radar range measurements. Data measured at all stations is transmitted to the computer at Cape Kennedy. Accuracy of GLOTRAC measurements is 30 meters (98.4 feet) in position and 0.15 meters/second (0.49 feet/second) velocity.

Table 7.3-1 AZUSA Characteristics

Transponder Type-C	
Receiver frequency	5060.194 MHz
Transmitter frequency	5000.000 MHz
RF power output	2.5 watts
Input voltage	28 Vdc
Input current	-5 amperes
Receiver input signal	-12 to -90 dbm
Weight	8.74 kg (19.3 lbs)
Size	0.006 meters^3 (372 inches^3)
AZUSA Ground Station Mark II	
Transmitted power	2 kw
Transmitter frequency	5060.2 MHz ±0.75 MHz
Ranging modulation	157.4 Hz, 3.934 kHz, 98.351 kHz
Receiver frequency	5000 MHz
Receiver sensitivity	-145 to -147 dbm
Receiver antenna gain	33 db (MK II)
Accuracies:	
Range	3.05 meters
Angle	1 x 10^{-5} in cosine data

SECTION 7.4

ODOP TRACKING SYSTEM

The ODOP (Offset DOPpler) tracking system is essentially the same as the UDOP system used for many years at the Atlantic Missile Range, but ODOP operates at different frequencies. It is a phase-coherent, multistation Doppler tracking system which measures position of a vehicle equipped with the ODOP transponder. ODOP stations are located at and around Cape Kennedy. The ODOP transponder is carried in the first stage (S-IB or S-IC) of the Saturn Vehicles and, therefore, ODOP tracking data is limited to the flight of the first stage only. The ODOP tracking system provides data immediately following lift-off while other tracking systems cannot "see" the vehicle or their accuracy is reduced by multipath propagation during the early phase of the flight.

The basic operation of the ODOP system is illustrated in Figure 7.4-1. The ground transmitter radiates a CW signal of 890 MHz to the transponder in the vehicle. The transponder shifts the received signal in frequency by 70 MHz and retransmits it to the receiving stations (R1, R2, R3). The signal from the transponder received at the ground stations contains a 2-way Doppler shift f_D which is extracted by mixing the received signal (f_i = 960 MHz + f_D) with the reference frequency (f_R = 960 MHz) derived from the transmitter frequency. Actually, a reference frequency of 53.33 MHz is transmitted over a VHF link to each transmitter station and then multiplied by a factor of 18, yielding 959.94 MHz. When this frequency is combined with the signal received from the

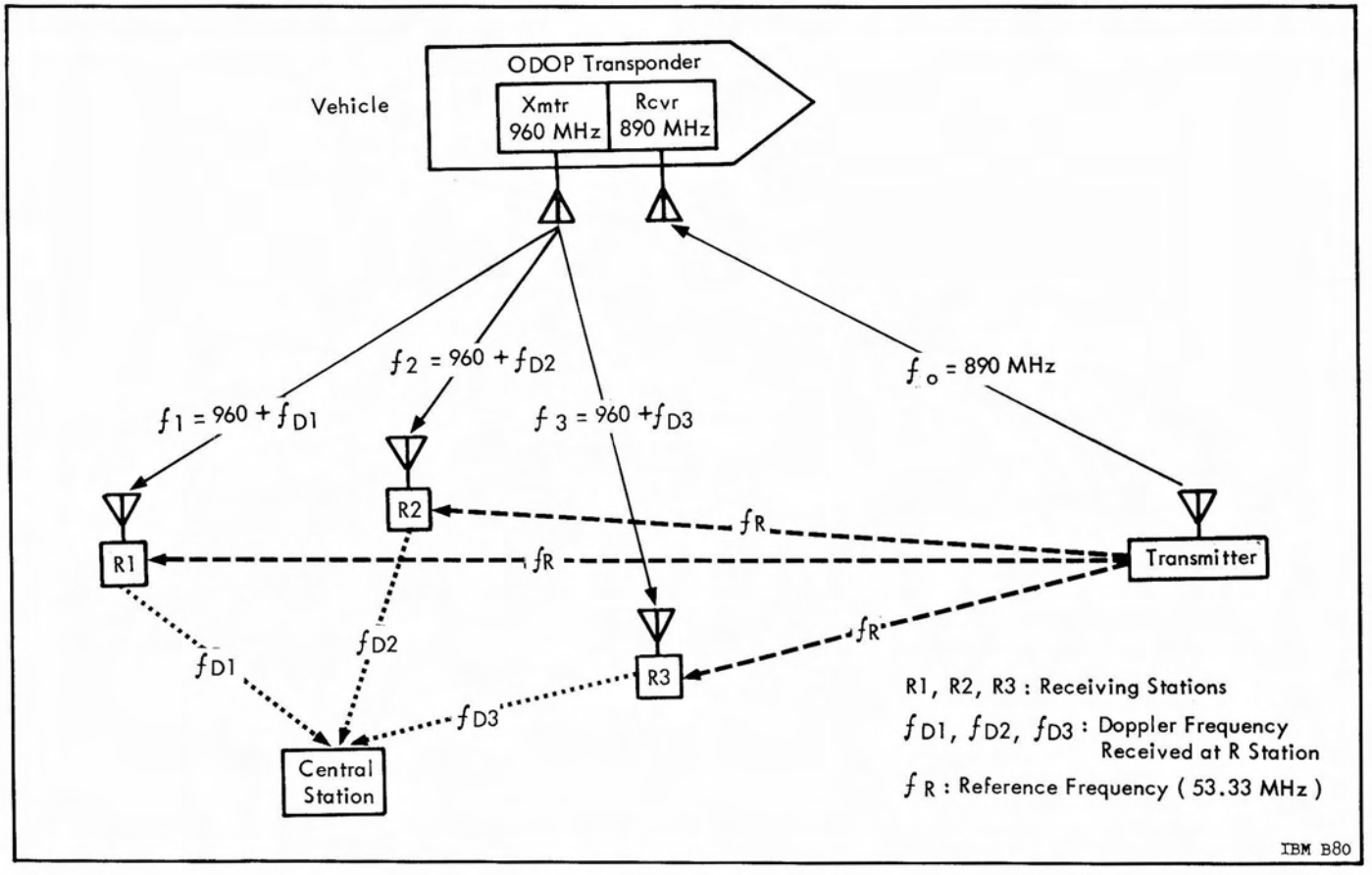

Figure 7.4-1 ODOP System Configuration

transponder, the Doppler shift is obtained with a 60 kHz bias frequency (60 kHz $+f_D$). The UDOP system used a transmitter frequency of 450 MHz which was doubled in the transponder (900 MHz). The higher frequency in the ODOP system (890 MHz versus 450 MHz) is less affected by the ionosphere and the result is increased tracking accuracy.

The Doppler frequencies, f_D, (including the bias frequency) from all receiving stations are transmitted to the central station and recorded on magnetic tape. Integration of the Doppler frequency received at a particular station provides the range sum, i.e., the distance transmitter-transponder-receiver. At least three range sums (for three different stations) are necessary to compute the position of the vehicle (transponder). The ODOP system uses 20 receiver stations around Cape Kennedy for redundancy and optimum tracking geometry. ODOP tracking data is not available in real time but is obtained from post-flight evaluation.

A block diagram of the ODOP transponder is shown in Figure 7.4-2. It is a modified version of the transponder used by the Jet Propulsion Laboratory in the Ranger Vehicles. Separate antennas are used for the receiver and the transmitter. The transponder consists of a double superheterodyne receiver (890 MHz) and a transmitter (960 MHz). The signal transmitted from the transponder is phase-coherent with the signal received by the transponder. Phase coherence is accomplished by an automatic phase tracking loop. The transponder is completely transistorized.

The characteristics of the ODOP tracking system are listed in Table 7.4-1.

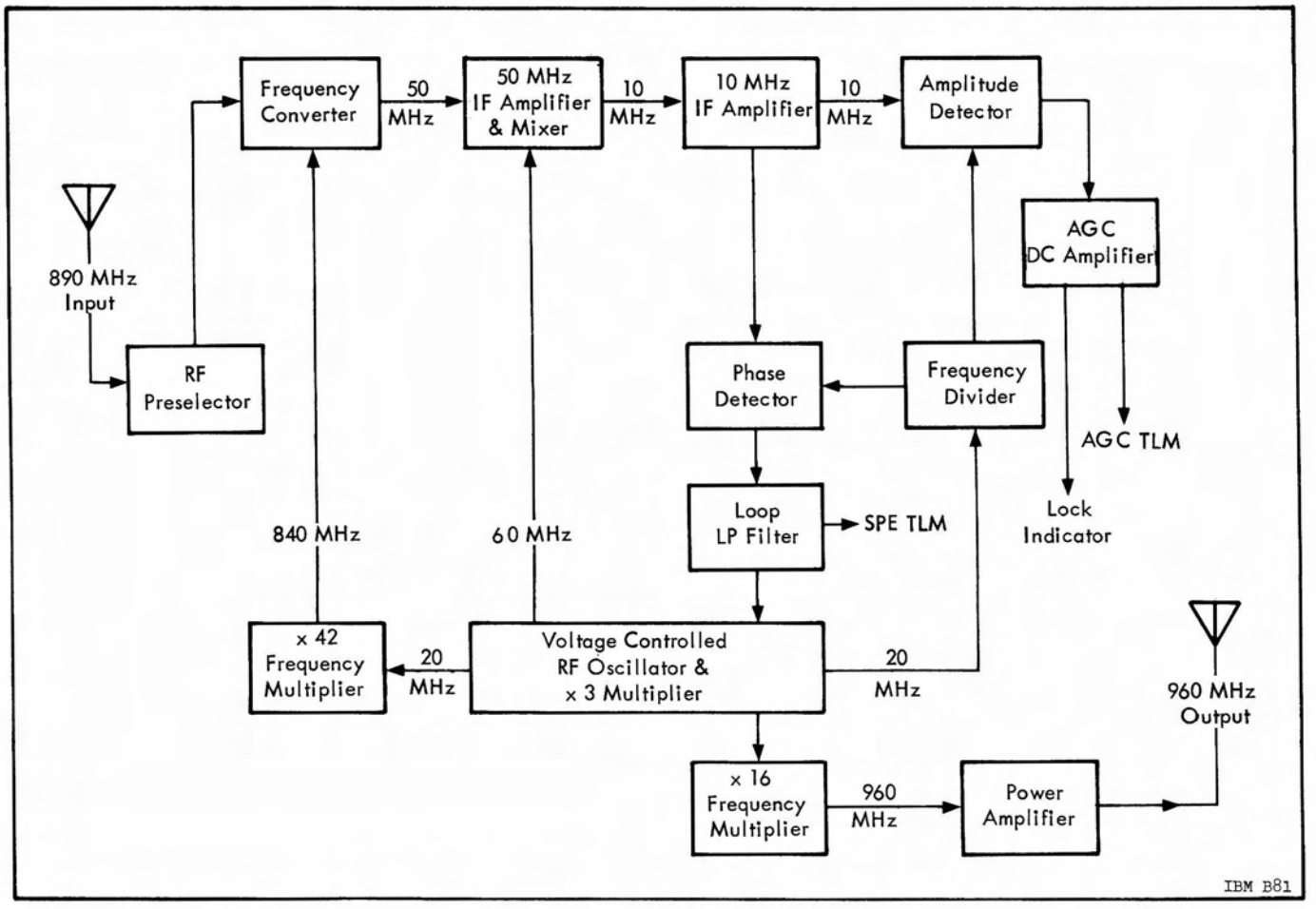

Figure 7.4-2 ODOP Transponder Block Diagram

Table 7.4-1 ODOP System Characteristics

Ground Transmitter:	
Frequency	890 MHz
Transponder:	
Receiver frequency	890 MHz
Receiver noise figure	14 db
Receiver threshold sensitivity	-132 dbm
Predetection bandwidth	100 kHz
Threshold noise bandwidth.	600 Hz
Strong signal noise bandwidth	1400 Hz
Transmitted frequency.	960 MHz
Transmitter power	1 watt
Required dc power	36 watts (28 volts)
Weight	10.25 kg (23.0 lbs)
Size	7370 cm^3 (448 in^3)
Ground Receiving Station:	
Receiver frequency	960 MHz
Receiver sensitivity	Not Available
Receiver bandwidth	Not Available
Receiver noise figure	Not Available

SECTION 7.5

S-BAND TRACKING

(To be supplied at a later date)

CHAPTER 8
POWER SUPPLY AND DISTRIBUTION SYSTEM

TABLE OF CONTENTS

SECTION 8.1

GENERAL DISCUSSION

The power supplies for the Saturn Launch Vehicles provide the electrical power necessary to operate the various onboard electronic and electromechanical components. Each vehicle stage contains batteries, power supplies, cables, connectors, and distributors. The distribution system interconnects these units. Figure 8.1-1 illustrates the arrangement of the power and distribution system components within each Saturn V Stage.

While the component interconnection is similar in each stage, the grounding scheme differs between stages. The IU grounding system is discussed later in this chapter.

The Power Distributor is the only distribution system component whose basic function may not be obvious. Essentially, it is a junction box which provides quick access to stage circuitry and overall stage and vehicle logic. Such a device becomes necessary because of the impact on airborne and ESE hardware which is created by the variety of mission requirements assigned to the Saturn Vehicles. The Power Distributors are equipped with terminals, relays, resistors, and diodes. These component parts are either hard mounted or mounted on printed circuit boards to permit rapid access to the distribution, switching, and isolation networks.

An illustration of the power and distribution system is shown in Figure 8.1-2. The figure represents a small portion of the actual logic involved, and only the IU system is detailed.

Functions provided by the power supply and distribution system include the following:

- Primary power is fed to high current capacity buses in the Power Distributor. Components which require high current levels are supplied directly from these buses.
- Each stage is equipped with a power transfer switch to select a power source either internal or external to the vehicle. During normal checkout operations, a ground power source will be used in place of the airborne batteries. A detailed explanation of power transfer is provided in Section 8.2.
- Each power source generally supplies at least one bus in each distributor.
- Buses are provided to other stages for event logic and EDS signal transmission.
- Power requirements, other than that supplied by the airborne batteries, are usually provided by a special power supply (e.g., power source for component D in Figure 8.1-2).
- Distributor switching facilitates checkout operations and is essential for control of certain flight events. Figure 8.1-2 illustrates how both intra-stage and inter-stage switching is accomplished.
- During prelaunch operations, many switching operations are possible from the ESE. Figure 8.1-2 illustrates how Power Distributor relays K1 and K2 are utilized to control the power to components C and D when the power transfer switch is in the external position. Typical Switch Selector control of power application and discrete event transmission is illustrated by the configuration of relays K3 and K4.

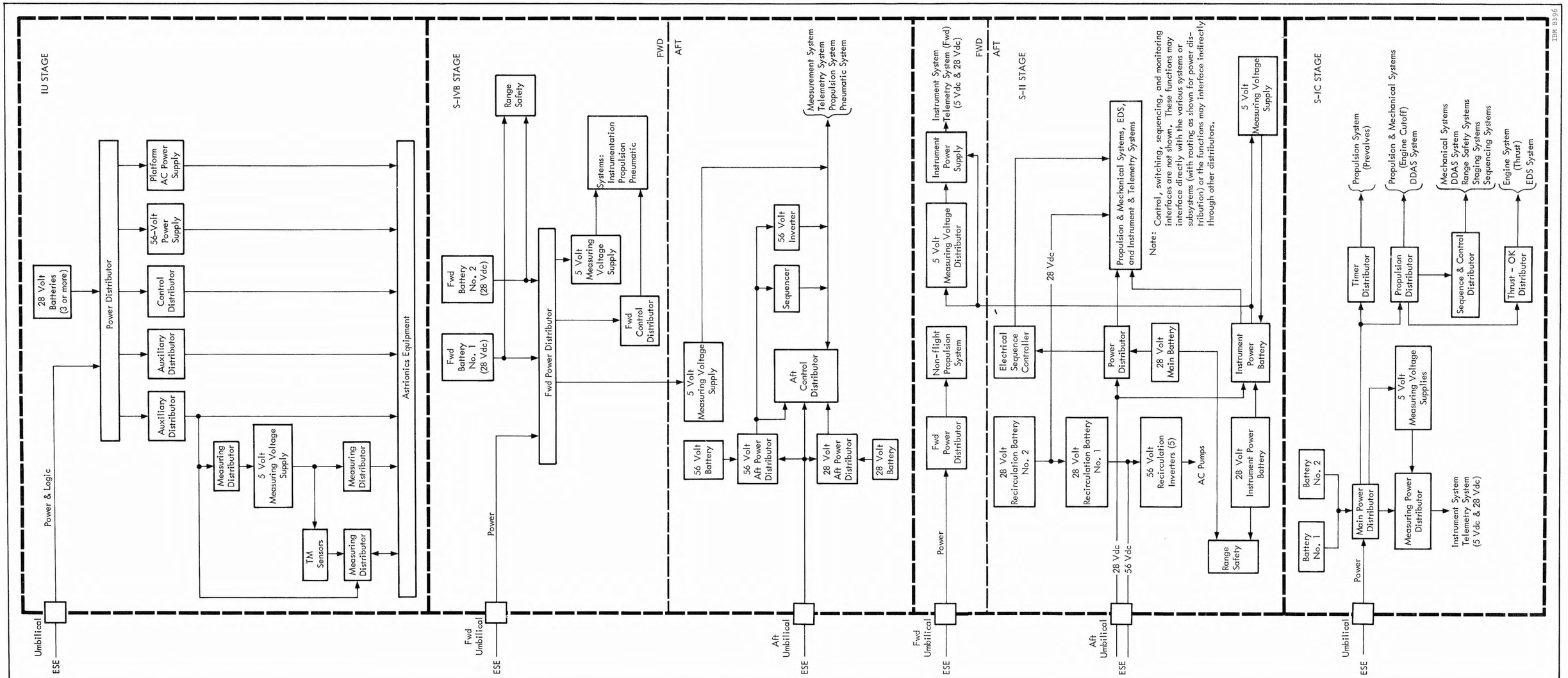

Figure 8.1-1 Block Diagram of the Saturn V Power Supply and Distribution Systems

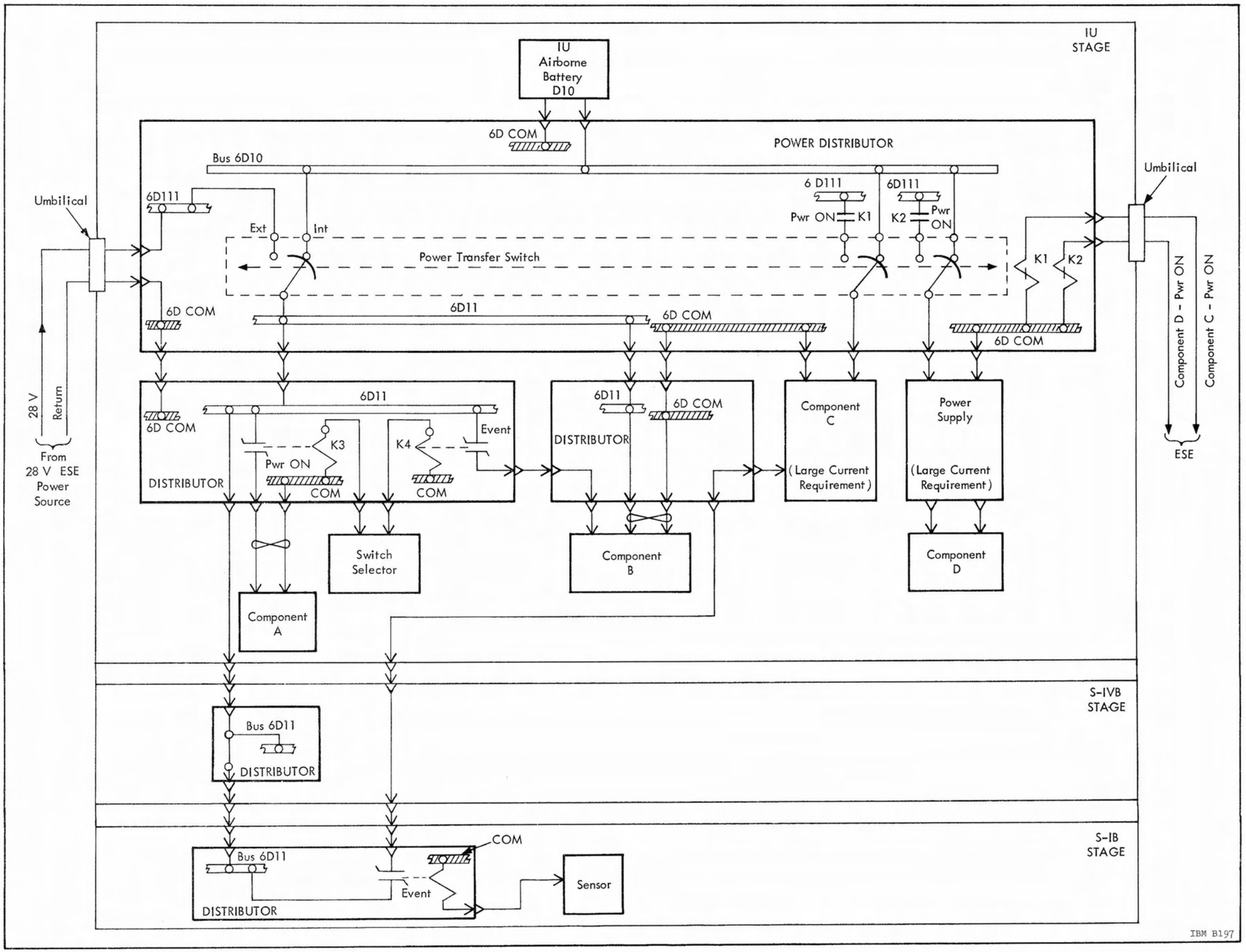

Figure 8.1-2 Partial Schematic of the Power and Distribution Systems

SECTION 8.2

IU POWER AND DISTRIBUTION SYSTEMS

The following paragraphs discuss the power supplies and distribution system within the IU Stage of the vehicle. The operation of the other stages is somewhat similar to that of the IU, and detailed discussions of these stages will not be presented.

8.2.1 POWER SYSTEM

The IU power components may be divided into 3 groups:

- Primary 28 Vdc power sources (internal and external)
- Inertial Platform system power
- Instrumentation system power

PRIMARY POWER SOURCES

The total IU power requirements vary according to mission assignment. The initial S-IB vehicles will use four IU Stage batteries. As the vehicle load requirements decrease, 3 batteries will normally be used. Load profiles are illustrated in Figures 8.2-1 and 8.2-2. The figures show the absolute and relative differences of IU Stage current drains between S-IB Vehicles, SA 201 and 205.

As stated in Section 8.1, each stage is equipped with a power transfer switch which is used to select either an internal or an external power source. During normal checkout operations, power from the ESE will be used in place of the vehicle batteries. A discription of the batteries will be found in Section 8.3.

Approximately 30 seconds prior to lift-off, a power transfer sequence (to internal power) is initiated. This action is accomplished by the power transfer switch which is similar to the switch illustrated in Figure 8.2-3.

To switch to the internal or external power state, an ESE command (28 Vdc) is sent to one of the drive-motor field coils. The motor switches the make-before-break contacts to the desired position. The switch will remain in that position until another ESE command is generated.

During prelaunch testing, the power transfer switch will be actuated several times. Figure 8.2-4 illustrates how the ESE generated power is used to simulate the airborne battery. As shown in the figure, the primary 28 Vdc (external) power is normally routed through an umbilical to the IU Power Distributor. The battery simulator shunts the internal and external buses in the Power Distributor to provide power to both input contacts of the transfer switch. During an umbilical plug drop test, a test cable is used to maintain continuity when the umbilical circuit is opened.

INERTIAL PLATFORM SYSTEM POWER

The Inertial Platform system requires several unique voltages. These are provided by the ST-124-M Platform AC Power Supply and the 56 Volt Power Supply. See Figure 8.2-5. The AC Power Supply is defined as a part of the Inertial Platform system and is presented in Chapter 14. Details of the 56 Volt Power Supply are contained in Section 8.4.

INSTRUMENTATION SYSTEM POWER

The instrumentation system requires special excitation and reference voltages for transducers and signal conditioning equipment. The power flow for this system is shown on Figure 8.2-6.

The 5 Volt Measuring Voltage Supply generates a highly regulated 5 Vdc output for use as a signal conditioning reference voltage and as excitation for some transducers. Transducer excitation voltages, other than the 5 Vdc supplied by the Measuring Voltage Supply, are generated in the Measuring Racks.

8.2.2 THE IU DISTRIBUTION SYSTEM

The IU distribution system provides the following:

- Power switching to large loads
- Power switching to medium loads
- Switching of low-power logic signals
- Proper interconnection of all electrical equipment

The Power Distributor performs the required switching of high-current loads. Medium-current load switching is accomplished by the Control Distributor and two Auxiliary Distributors. The large number of unique requirements presented by the emergency detection and instrumentation systems necessitates separate distributors for each of these systems. The remainder of the logic switching is performed by the Control Distributor and, to a limited extent, by the two Auxiliary Distributors.

The placement of the Control, EDS, and Auxiliary Distributors is illustrated in Figure 8.2-7. In general, components which require high-current switching are mounted near the Power Distributor, and components requiring numerous logic switching are located near the Control Distributor. The distributor mounting, relative to other components, provides for a minimum amount of cabling.

Certain hardware configuration problems arise where it is impractical to alter or redesign existing components just to provide correct signal routing. In cases such as this, a device called a Plug-type J-box is used. The J-box is a standard plug used as an adapter.

Redundancies in circuit design provide an increase in vehicle reliability. Certain components receive primary power from three separate batteries as a precaution against a primary power failure.

Measuring Distributors route the numerous airborne measurements to their respective destinations. A measurement originates in a transducer or within another component and is routed either directly to the telemetry system or indirectly through Measuring Rack signal conditioning equipment and a Measuring Distributor.

The large number of telemetry signals and numerous configuration changes require several Measuring Distributors. The Measuring Distributors provide the routing, voltage division, and current-limiting networks to ensure compatability between the measuring and telemetry systems. Through their switching capabilities, the Measuring Distributors can change the selection of measurements monitored by the telemetry system. The switching function transfers certain measurements to channels which had been allotted to expended functions. If it were not for this switching, these channels would normally be "wasted" for the remainder of the flight. The Measuring Distributor also provides the option of using RF link or PCM (DDAS) coaxial cable transmission during checkout operations for a more thorough and comprehensive system test evaluation.

The EDS Distributor contains the relay logic needed to monitor and interpret emergency indications and to issue the appropriate commands. Since the EDS Distributor is an integral part of the EDS, a more thorough description will follow in Chapter 9, Emergency Detection System.

8.2.3 IU GROUNDING SYSTEM

IN-FLIGHT ELECTRICAL GROUNDING

All Instrument Unit grounding is referenced to the outer skin of the stage. The methods used to accomplish IU grounding are illustrated in Figure 8.2-8. Each area will be described separately.

Power System Grounding. The power system is grounded by means of hardwires routed from the 6D COM bus in the Power Distributor to the 601E1 ground stud attached to the stage skin. This connection provides the single-point ground for the power system. All 6D COM buses in the various distributors are wired back to the 6D COM bus in the Power Distributor. The common buses, for the most part, are isolated from the chassis of the components in which they are enclosed. Isolating power supplies are utilized in some instances to accomplish this. The close proximity of the Power Distributor, batteries, and outer skin power ground termination point (601E1) assures that a relatively low potential difference will be developed by their respective ground levels.

Electrical or Black Box Grounding. Grounding of individual boxes and components is accomplished by direct metal-to-metal contact of the black box and cold plate or stage skin. All common return lines are isolated from the component chassis except in a

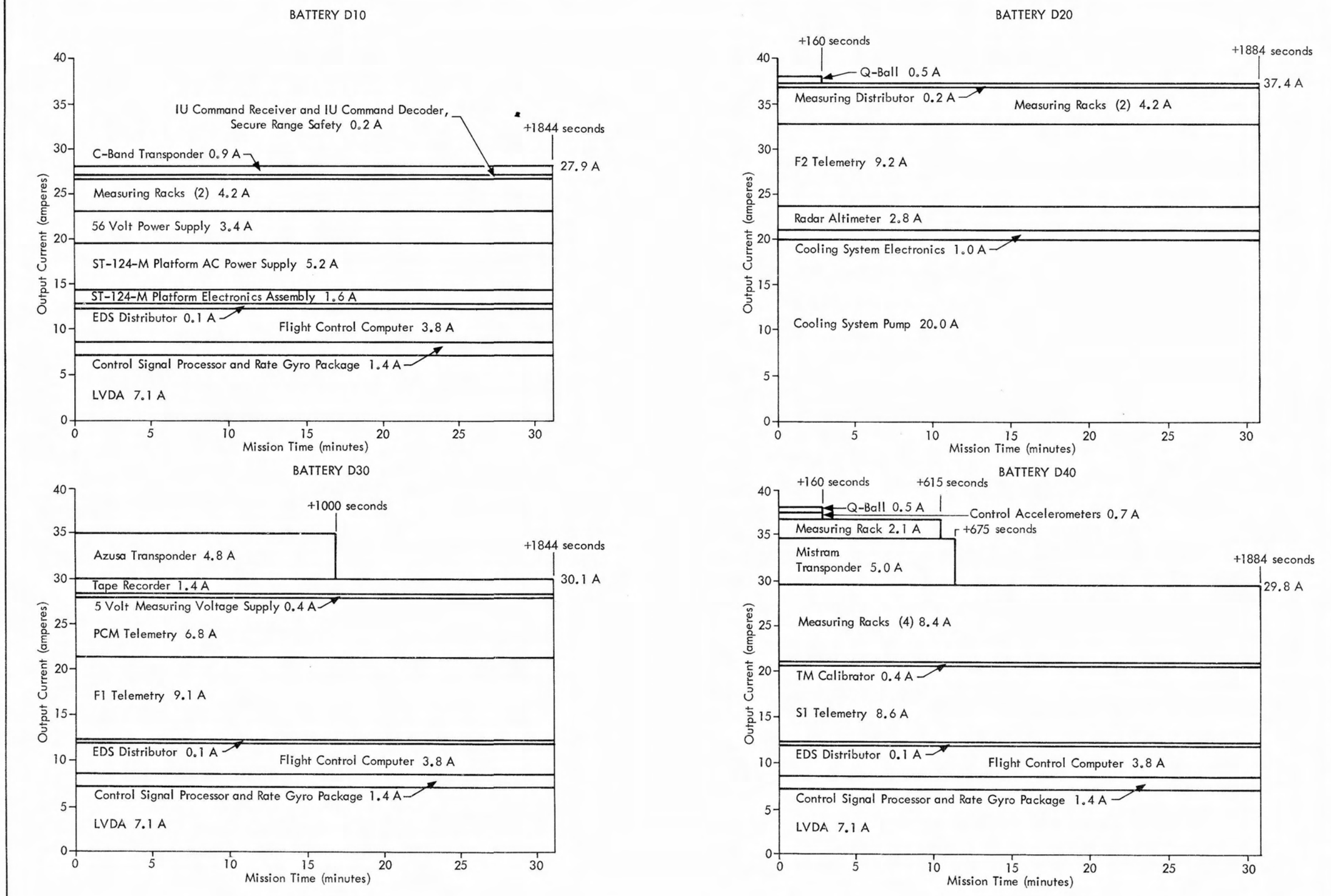

Figure 8.2-1 Battery Load Profiles for SA-IU-201

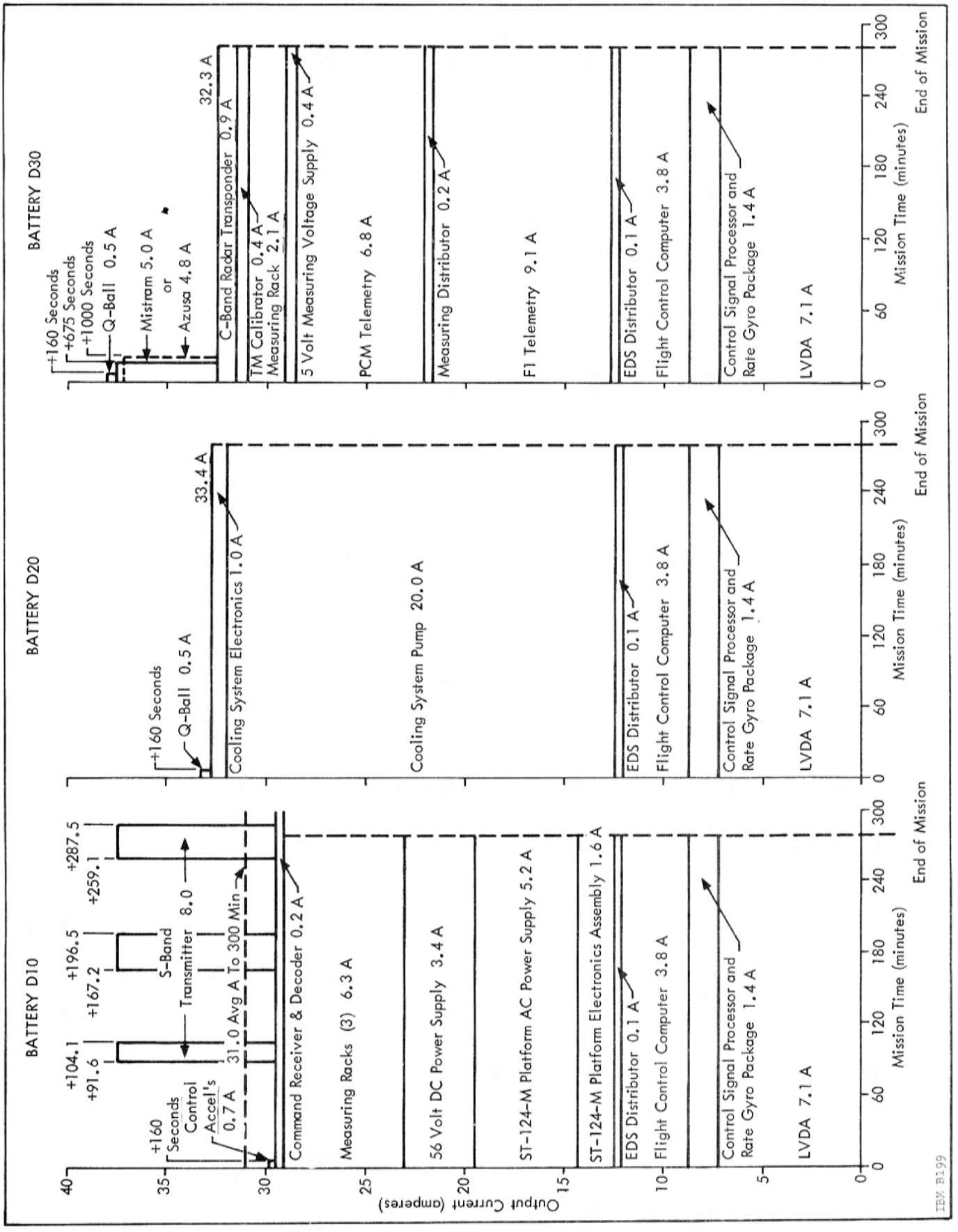

Figure 8.2-2 Battery Load Profiles for SA-IU-205 and Subsequent Vehicles

very few instances (e.g., some parts of the telemetry system).

Shield Grounds Internal to Black Boxes. Internal shields are connected directly to black box chassis where they are referenced to stage skin by means of metal-to-metal contact.

Shield Grounds for Cabling System. Cable Shields are grounded by 2 methods. They are as follows:

- Most shields are connected to the 6D COM bus in one of the distributors. This is accomplished by extending the shield through the last small contact of the distributor connector where it is routed to the 6D COM bus. Where several cables are connected in series, the cable shields are routed through the last small contact of the interconnecting connector. This method is used in order to keep the cable shielding continuous from the black boxes through each interconnecting cable to the distributor.
- When the shielded cables are routed between two black boxes and do not terminate at a distributor, a second method of terminating cable shielding must be utilized. In this case, only one end of the shield is grounded. The shield is routed through the last small connector contact on one of the components and terminated at the chassis. The black box chassis is grounded normally (as outlined earlier). Where several shielded cables are connected in series from black box to black box, the cable shield is made continuous by routing the shield through the last small contact of the interconnecting connectors.

RF Grounding. RF grounding of components is effected by means of metal to metal grounding. Refer to the paragraph on electrical or black box grounding. RF connectors and cables are grounded through the shell of the connector to the black box.

PRELAUNCH GROUNDING

The IU and ESE common systems are referenced to earth ground prior to launch. Shortly after engine ignition, the umbilicals are ejected. To assure the IU remains at earth potential until all umbilicals are ejected, two single-wire grounding cables are connected to the IU. They are the final conductors to be disconnected from the IU Stage. One of these cables is connected to the ESE 6D COM bus. This cable is routed through a single-conductor connector located below the umbilical plate and is terminated at

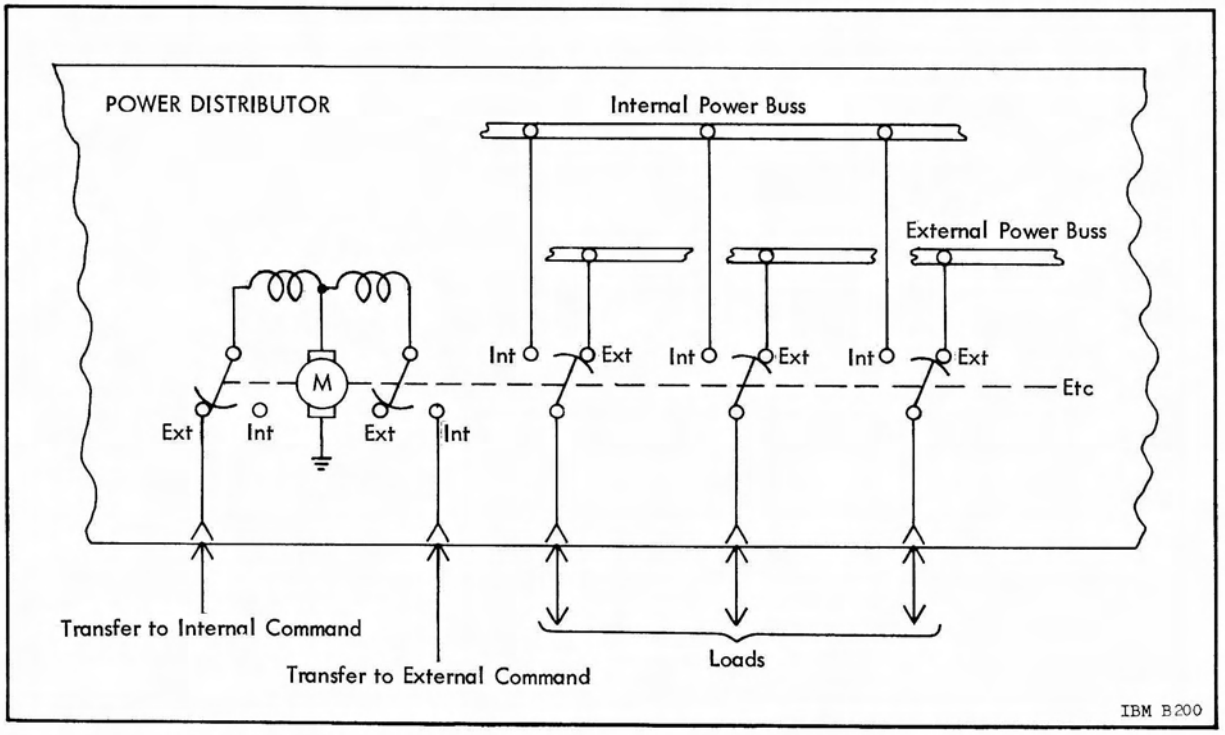

Figure 8.2-3 Partial Schematic of the IU Power Transfer Switch

stage single-point ground terminal, 601E1. Cables routed from the ESE across the swing arms to the stage umbilical have an overall RF shield to avoid induced signals from local tracking antennas. These shields are terminated by a second single-conductor cable which is routed from the ESE side of the umbilical through a one-pin connector to stage skin terminal 601E2. This connector is also located below the umbilical plate.

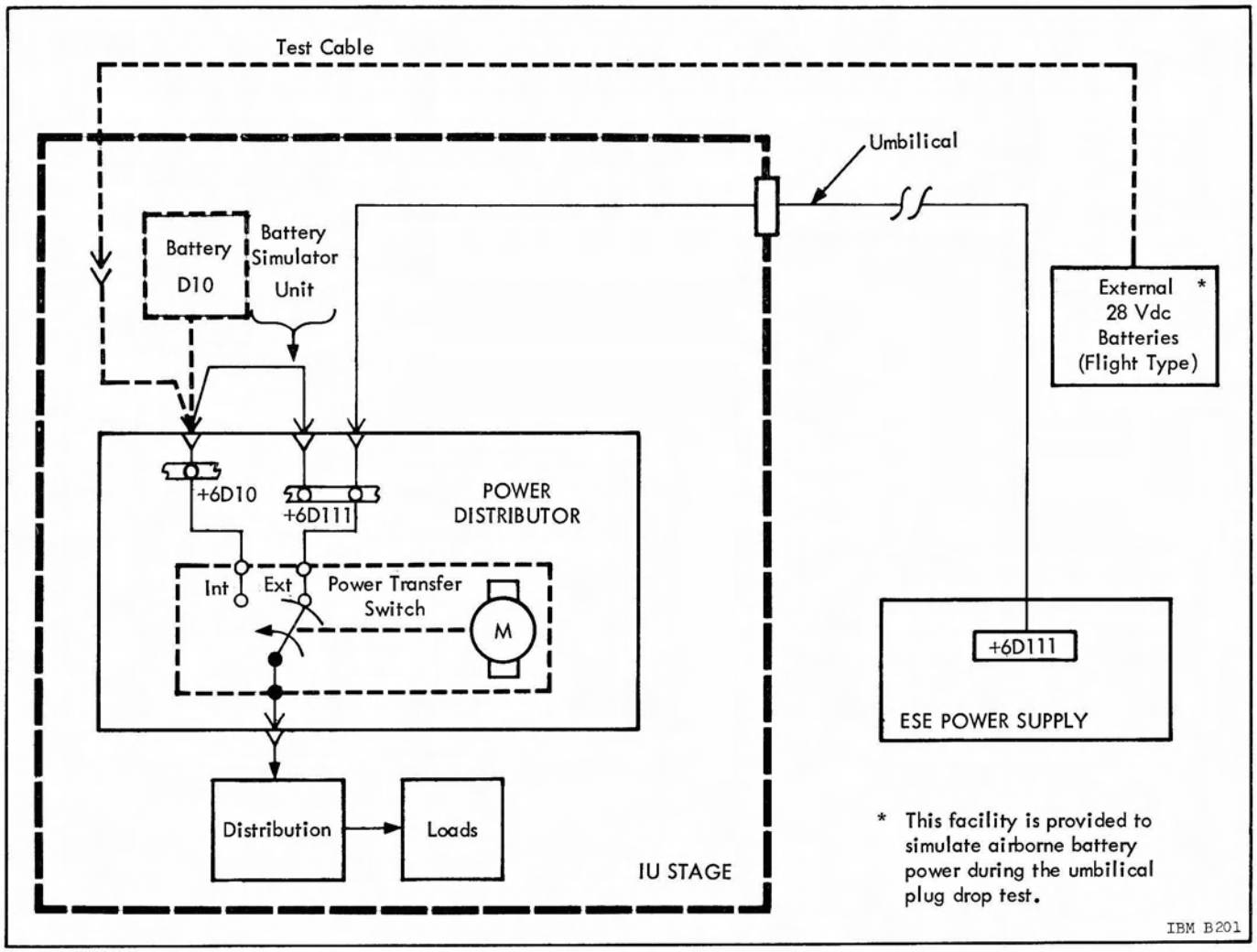

Figure 8.2-4 Ground Checkout Configuration of IU Power Derivation

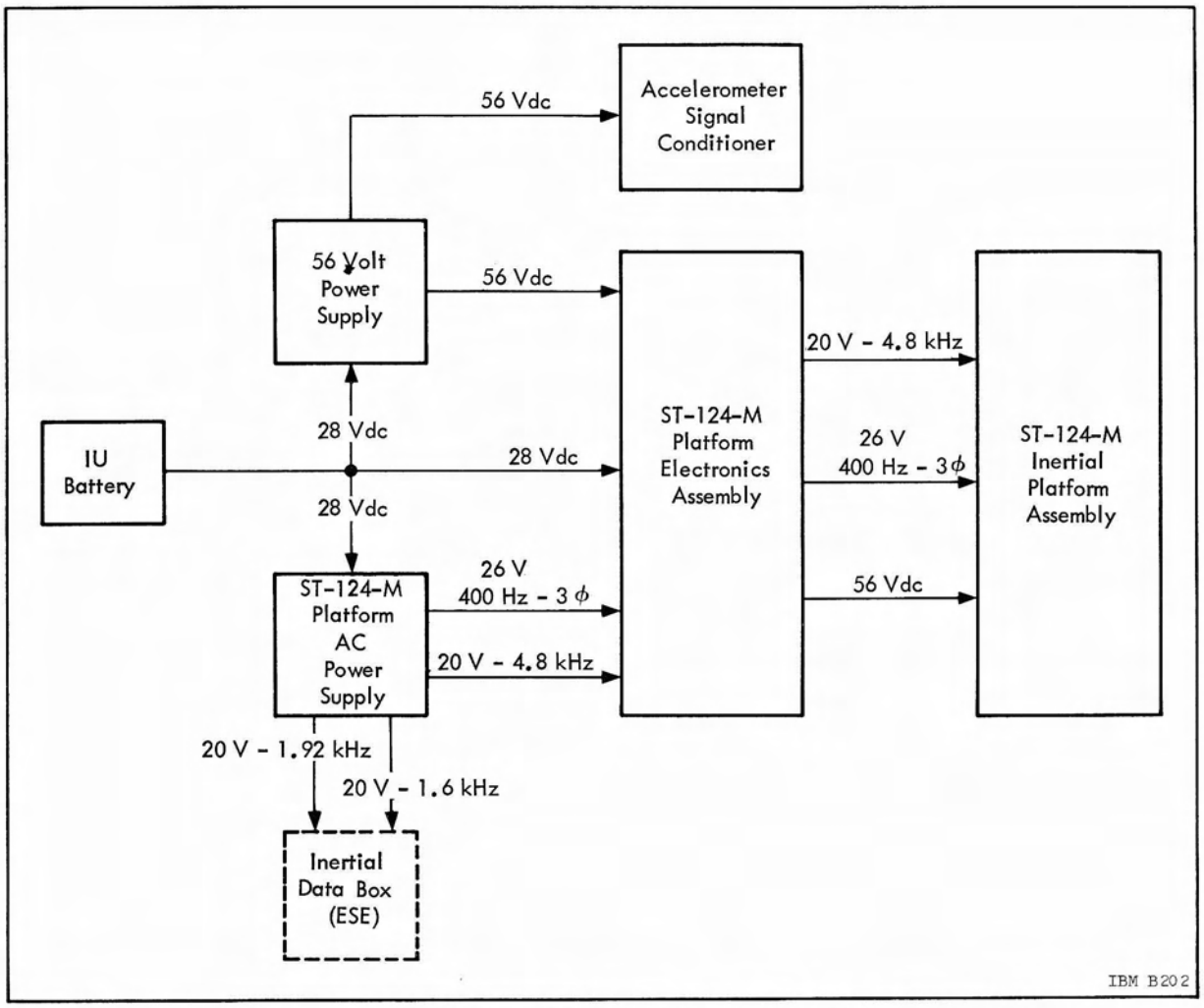

Figure 8.2-5 Inertial System Power Flow

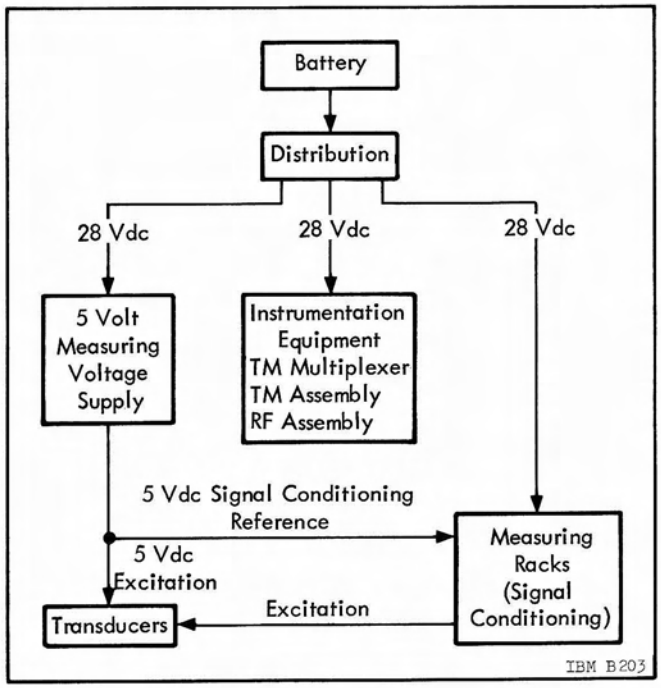

Figure 8.2-6 Instrumentation System Power Distribution

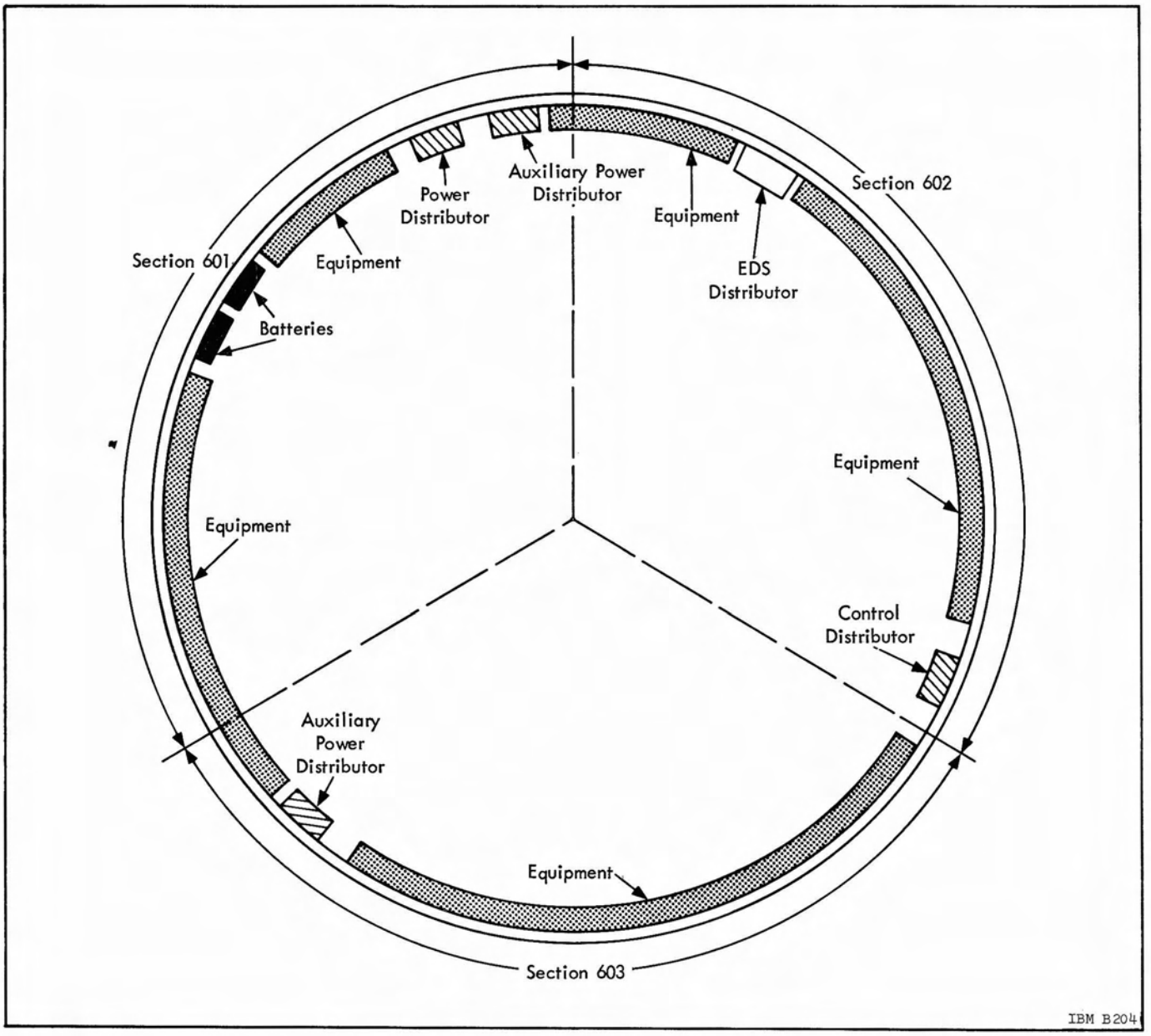

Figure 8.2-7 IU Distribution Equipment Layout

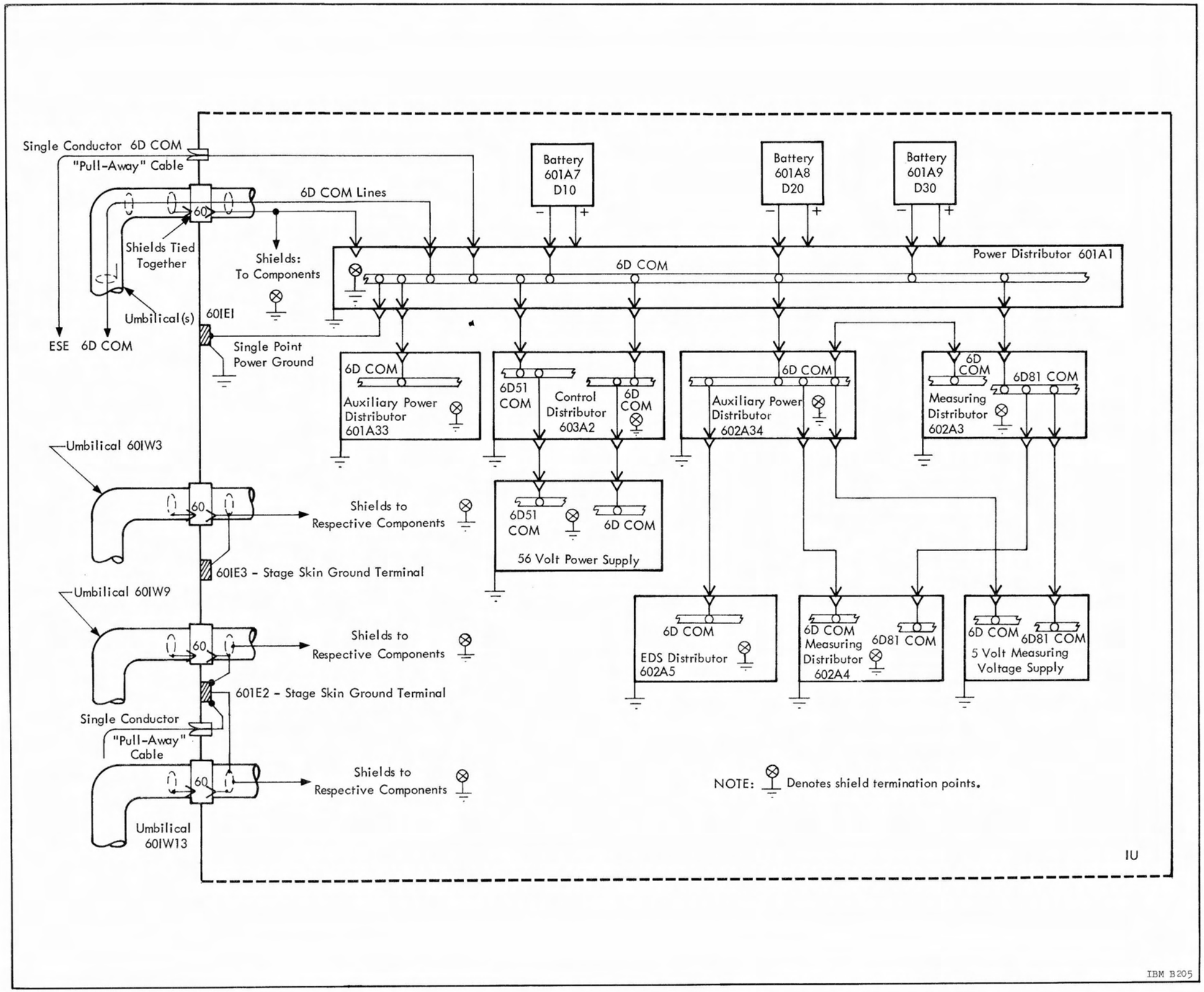

Figure 8.2-8 IU Grounding System for Saturn IB and V Vehicles

SECTION 8.3

BATTERIES

Three or more 28 Vdc batteries are used in the IU to provide the primary power for all electrical components. Each source is a dry-charged, alkaline silver-zinc, primary battery. During launch countdown, the batteries are activated by adding a potassium hydroxide (KOH) electrolyte.

A primary battery contains 20 series-connected cells, each producing a nominal 1.5 volts. Occasionally, the full 20-cell output voltage may exceed the specified tolerance. In such cases, 18 or 19 cells may be selected by varying the configuration of battery connector J/P3.

To prevent an excessive internal pressure buildup, a relief valve is provided. The valve vents internal pressures in excess of 69,000 N/meter^2 g (10 psig).

Table 8.3-1 summarizes the major IU battery characteristics.

Table 8. 3-1 IU Battery Characteristics

Battery Type	MAP 4240 - Dry charged
Cells	
Number	20 (with provisions for selecting 18 or 19 cells if required)
Nominal voltage per cell	1. 5 Vdc
Material	Alkaline silver-zinc
Electrolyte	Potassium hydroxide (KOH)
Output	
Voltage	+28 ± 2 Vdc
Current	35 amperes for a 10-hour load period (if used within 72 hours after activation)
Measurements available	Current output Internal temperature
Cooling System	Cold plate
Ambient Temperature Range	+10°C to +48. 9°C (+50°F to +120°F) for proper operation
Heat Transfer Characteristics	
Dissipation	0. 07 W/cm^2 (0. 47 W/in.^{2})
Surface area	2074 cm^2 (321. 4 in.^{2})
Total dissipation	150 watts
Physical Characteristics	
Activated weight	75 kg (165 pounds)
Dimensions	
Length	65. 5 cm (25. 4 in.)
Width	26. 9 cm (10. 6 in.)
Depth	23. 1 cm (9. 1 in.)
Volume	40, 164 cm^3 (2450 in.^{3})

SECTION 8.4

56 VOLT POWER SUPPLY

The 56 Volt Power Supply provides operating voltage to the ST-124-M gyro and accelerometer servoloops. The voltage is also used in the Accelerometer Signal Conditioner.

Figure 8.4-1 illustrates the technique used to develop a regulated 56-volt output. A 2-kilohertz blocking oscillator develops a square wave which is transformer coupled to a magnetic control amplifier. The signal is then passed through 2 stages of amplification to a rectifier bridge and filter network which provides a low-ripple, 56 Vdc output. The reference bridge regulates the output voltage by changing the amplification in response to voltage variations sensed at the output.

A summary of performance characteristics of the power supply is presented in Table 8.4-1.

Table 8.4-1 56 Volt Power Supply Electrical Characteristics

Input Voltage	24 to 32 Vdc
Output Voltage	
0 to 1 A load	56 ± 0.5 Vdc
1.1 to 8 A load	56 ± 2.5 Vdc
8.1 to 10 A load	56 ± 3.5 Vdc
Output Load	
Minimum continuous load	0.5 A
Maximum continuous load	3.0 A
Output Ripple	
0 to 5 A load	0.25 V peak-to-peak
Range of Output Setting	56 ± 0.5 Vdc
Efficiency	75 percent
Warm up Requirement	2 minutes
Operating Temperature Range	-25°C to +100°C (-13°F to +212°F)

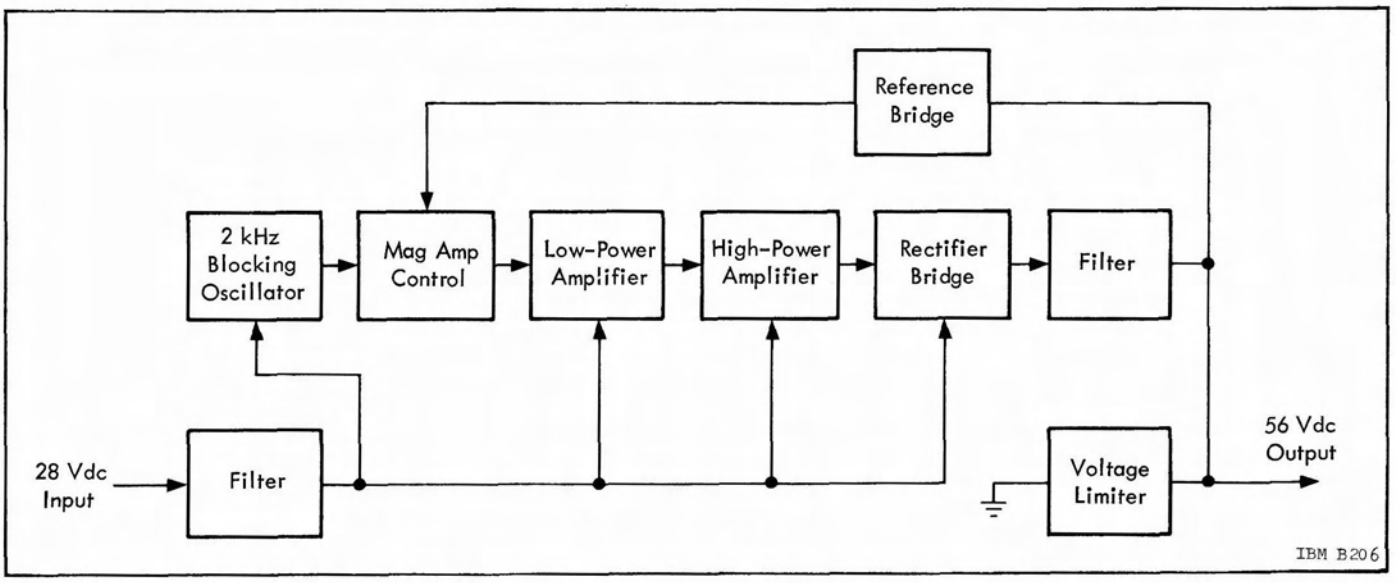

Figure 8.4-1 56 Volt Power Supply Block Diagram

SECTION 8.5

5 VOLT MEASURING VOLTAGE SUPPLY

The 5 Volt Measuring Voltage Supply provides excitation voltage for the various vibration, temperature, pressure, and engine position tranducers within the IU instrumentation system. The measuring supply is also used to provide a reference voltage for in-flight calibration of certain telemetry channels.

The power supply consists of the following major elements:

- Preregulator circuitry
- Square-wave oscillator
- Stepdown transformer - rectifier
- Series regulator - output filter

Figure 8. 5-1 is a block diagram of the 5 Volt Measuring Voltage Supply. The preregulator operation is analogous to a servo amplifier. The filter output is compared with a constant reference voltage and the resulting error voltage is applied to an amplifier which varies the duty cycle of the pulse-width modulator. The output of the pulse-width modulator is a square wave whose period is a function of the error voltage detected in the comparator. A filter circuit follows the pulse-width modulator to provide an average dc value of the modulator output The square-wave oscillator output voltage is reduced in the stepdown transformer and is rectified and filtered prior to entering the series regulator. The final stage of regulation is accomplished by varying the conduction across the series regulator control element which is a transistor. The conduction of this transistor is controlled by the magnitude of the error voltage sensed by the comparator.

An overload protection circuit is provided to limit the series regulator current to a safe level in the event of an overload at the output.

The characteristics of the 5 Volt Measuring Voltage Supply are presented in Table 8. 5-1.

Table 8. 5-1 5 Volt Measuring Voltage Supply Characteristics

Physical Characteristics	
Weight	0. 7 kg (1. 5 pounds)
Dimensions	
Length	11. 5 cm (4. 5 in.)
Width	12. 6 cm (4. 9 in.)
Depth	5. 1 cm (2. 0 in.)
Input Characteristics	
Voltage	28 ± 4 Vdc
Current	0. 6 A (max)
Power	14. 4 W (max)
Output Characteristics	
Voltage	5. 000 ± 0. 005 Vdc
Range of output adjustment	± 0. 050 Vdc
Current	0 to 1 A
Power	5 W (with 1 A output)
Cooling Characteristics	
Cooling	Cold plate
Heat transfer surface area	142. 6 cm^2 (22. 1 $in.^2$)
Heat transfer of mounting area	0. 05 W/cm^2 (0. 32 $W/in.^2$)

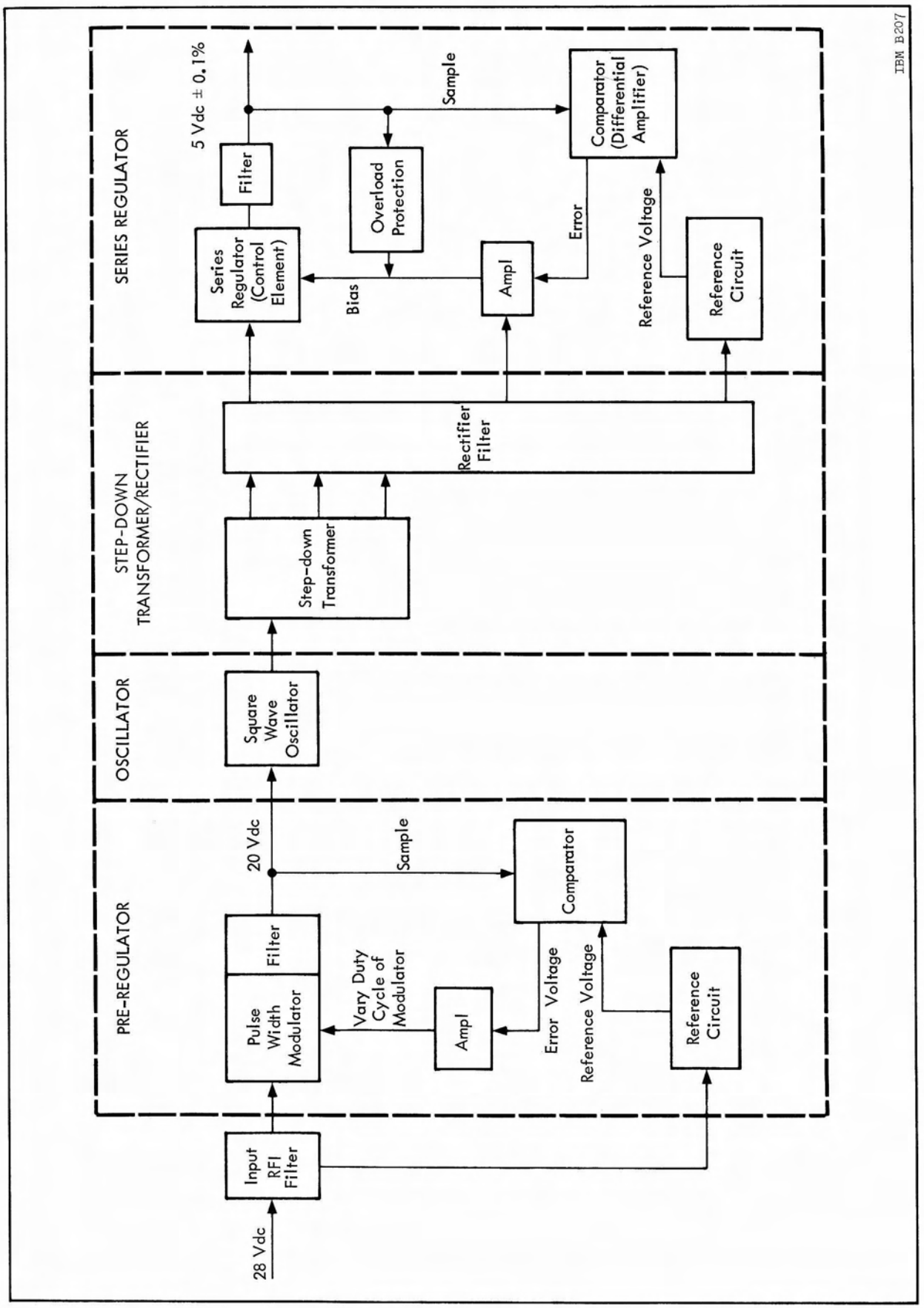

Figure 8.5-1 5 Volt Measuring Voltage Supply Block Diagram

CHAPTER 9

EMERGENCY DETECTION SYSTEM

TABLE OF CONTENTS

SECTION 9.1

CREW SAFETY SYSTEM

The emergency detection system detects malfunctions in the launch vehicle which lead to emergency situations. The EDS is one part of the crew safety system. The other part of the crew safety system is the launch escape system which removes the flight crew from the vicinity of the malfunctioning vehicle. Essentially, there are two kinds of emergency situations: explosion of the vehicle propellants and breakup of the vehicle by aerodynamic forces.

The crew safety system for Saturn/Apollo Vehicles is semiautomatic. The system can sense failure modes that slowly lead to catastrophic conditions and indicate these failures on a display panel to the flight crew to allow them to make the abort decision.

The system can also automatically initiate an abort when it senses a failure mode that will lead to a rapid vehicle breakup. Studies of many failure modes have shown that despite the tremendous mass and inertia of the Saturn Launch Vehicles, the time from occurrence of a malfunction until the vehicle reaches a "breakup" angle of attack can be very short. Therefore, a fast responding automatic capability must be included in the crew safety system.

The Saturn V Apollo crew safety system is very similar to the Saturn IB system but has 3 stages to monitor. Because of increased loading, the system must also monitor propellant tank pressures in the S-II and S-IVB Stages.

9.1.1 GUIDELINES FOR CREW SAFETY

The EDS must be as simple as possible because of space and weight limitations of flight hardware and because any detection equipment has a possibility of malfunctioning and causing the abort of an otherwise successful mission. For this reason the number of sensors in the detection system must be kept to a minimum. This decrees that the effect of a malfunction is sensed rather than the malfunction itself. As an example, the EDS can be simplified by monitoring the angle of attack and attitude rates of the vehicle rather than the position of each engine actuator. (Engine actuator failures lead to loss of control and eventual vehicle breakup because of an excessive angle of attack.) Since other vehicle failures lead to this same effect (excessive angle of attack and/or attitude rates), the monitoring of failure effects yields a considerable simplification of the crew safety system. This method of simplification is possible only when the time between failure sensing and catastrophic vehicle loss is enough to allow a safe escape distance from the vehicle.

An important guideline used in the development of the Saturn/Apollo crew safety system is that, whenever enough time is available, the abort decision will be left to the flight crew rather than automatically initiated. It is felt that no matter how reliable the automatic abort system is made, it can never replace the logic, judgement, and observation powers of the flight crew. However, many of the failure modes of the vehicle do not allow sufficient time for the flight crew to make a decision and react to the emergency; in these cases, the crew must rely on the automatic abort system.

Since a falsely initiated abort could ruin an otherwise successful mission, the system has been designed to reduce the probability of a false automatic abort to an insignificant level. It is extremely important that the crew safety system does not degrade the mission success probability.

Table 9.1-1 shows some of the more important design guidelines.

9.1.2 FAILURE ANALYSIS

The design of the emergency detection system is based on failure mode and effect analysis. This is a complete analysis of each stage, system, subsystem,

Table 9.1-1 Important Guidelines for the Crew Safety System for Saturn Apollo Vehicles

Simplicity	- Use minimum number of sensors and sense effect of failure rather than cause — when time permits.
Abort Decision	- Made by flight crew whenever time permits — manual rather than automatic.
Mission Degradation	- Probability of false automatic abort reduced to insignificant level.

- Initiation of manual abort will be based on at least two separate and distinct indications.
- In the event of conflicting information from the onboard crew safety system and telemetered data relayed to the Spacecraft from the ground, the onboard information shall always take precedence.
- Triple redundant electrical circuits utilizing majority voting logic will be used for all automatic abort signals.
- As a design objective, redundant circuitry will be used for manual abort indications from the Saturn Launch Vehicle to the Spacecraft.
- It shall be a design objective that no single point electrical failure in the onboard crew safety system will result in an abort.

and component within the vehicle to determine which component failure modes can cause a failure of the subsystem, which subsystem failures can cause failure of the system, and which system losses can cause loss of the stage and/or vehicle. A failure mode and effect analysis begins at the component level and investigates each possible way in which the component can fail (i.e., open, short, rupture, leak). The effect of the particular failure is analyzed on higher levels of assembly until the effect of that particular component failure on the space vehicle is determined.

Once the failure analysis of a component is completed, a criticality number is assigned to the component. For example, a number 10 indicates that this component can be expected to cause a vehicle loss about 10 times out of 1 million flights.

After the criticality number has been derived for each component, the numbers are summarized for each subsystem, system, and stage of the vehicle—vehicle dynamics must be analyzed and structural limits determined. For example, a failure mode and effect analysis shows that a particular group of control component failures can cause the engines to gimbal "hardover"; this would mean vehicle loss and a criticality number could be derived to show the expected frequency of this failure.

The criticality numbers are summarized on a summary chart which is referred to as a "failure tree". Figure 9.1-1 represents the latest failure tree summary of the IU Astrionics system of the Saturn IB Vehicle. In this figure, the failure is traced back only 3 or 4 levels and does not reach the component mode in most cases.

Beyond this analysis of failures, the length of time between the occurrence of the failure and the time of reaching the critical angle of attack must be known. This is a function of the time of flight. If the failure occurs about maximum Q, we may have the worst case condition and less time is available between the occurrence of the failure and structural breakup of the vehicle. To determine these limits, the structural limit curves must be drawn for each type of failure (control engines hardover, engines null, engines out, etc.). These curves show the various combinations of vehicle angle of attack and engine gimbal angle at which the structural limits of the vehicle are exceeded, as a function of time of flight. As an example of these curves, refer to Figure 9.3-1. Curves must also be drawn of the actual expected excursions of vehicle angle of attack and engine gimbal angle during each of these vehicle failure modes. The two sets of curves must then be analyzed to determine whether (and at what time)

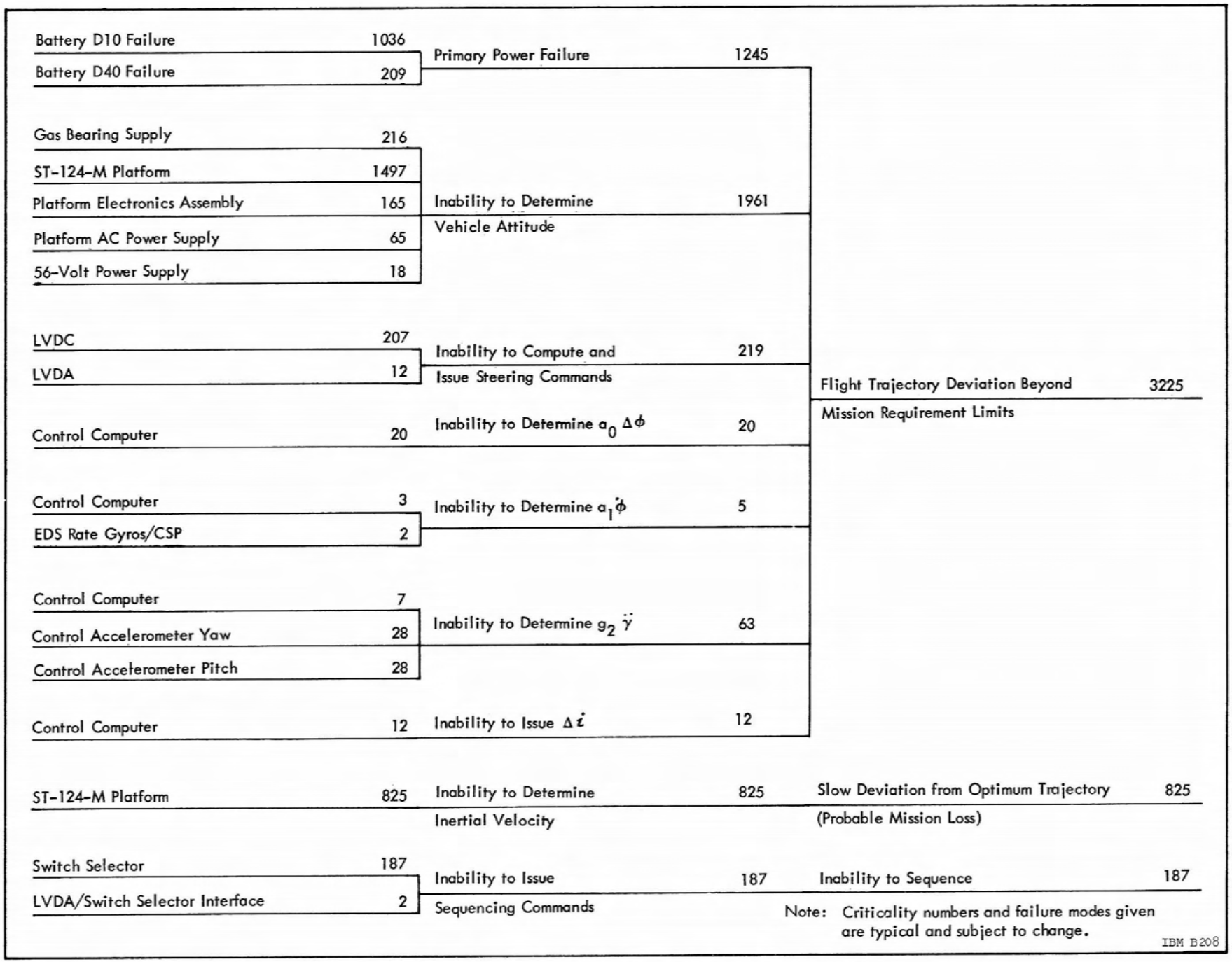

Figure 9.1-1 Saturn IB IU Astrionics System Failure Modes

the structural limits of the vehicle will be exceeded for each particular failure condition.

From the information on the effect of these failures and the information on the vehicle dynamics or structural limits, the time available between occurrence of the failure and catastrophic loss of the vehicle can be derived. This time will indicate the response time required of the detection mechanism. The time will determine whether the crew has sufficient time to recognize the emergency warning and make a decision as to when to abort. If human response would be too slow, the abort or escape must be automatically initiated. A range of safe limits is assigned to each parameter selected for monitoring. Performance within these limits assumes the parameter to be functioning normally. Generally, the selected parameter could have a range of acceptable tolerance bounded by both an upper and lower level of safety (e.g., over pressure and under pressure in a pressurized tank). However, in some conditions only one safety limit is needed (e.g., high angles of attack). As long as conditions of the measured parameter stay within the safety zone, it is assumed that all components are operating satisfactorily. If the measured value approaches the danger level, a catastrophic failure is imminent.

The problem is to decide at what level to place the abort level. If the abort level is placed too close to the tolerance limit, an abort might be needlessly triggered. If, on the other hand, it is moved too close to the danger level (to hedge against a needless abort), there may not be time enough for a safe escape because of various systems delays. The task is often complicated because the danger levels, as well as the tolerance zone, of certain parameters may change as a function of time. Other factors that further complicate the problem are transients which momentarily exceed the danger level but offer no catastrophic threat. These must be taken into account during crew safety systems design.

SECTION 9.2

EMERGENCY DETECTION SYSTEM

The Saturn/Apollo emergency detection system has triple redundant sensors and majority voting logic for all the automatic abort parameters. Dual redundancy is used for most of the manual abort sensors. The redundancy is so arranged that the predominant failure mode of the sensing system has been protected against. The guideline rule of having at least two separate and distinct indications of failure before initiating a manual abort is a protection against any inadvertent aborts from malfunctioning sensor systems. The displays used in the Spacecraft are "fail safe" wherever practical. Where possible, the meters used for display of analog signals are "zero offset". This means that the predominant failure modes of the sensing system (loss of power, etc.) will indicate off scale conditions (either high or low) rather than readings within the scale of interest. The indicator lights used for discrete indications to the flight crew are dual-bulb lights and so arranged that the crew cannot distinguish whether one or both lights are on. A failure of one light will not be noticed by the flight crew. The other failure mode (inadvertent light) is protected against by requiring two separate and distinct indications of failure.

The Saturn IB/V crew safety system is shown in the functional diagrams, Figures 9.2-1 and 9.2-2. Monitored parameters are: stage thrust for both stages, guidance computer status, angular attitude rates, attitude error, and angle of attack for Spacecraft display. Automatic abort is initiated for S-IB and S-IC two-engine-out or for excessive angular rates in pitch, roll, or yaw; these automatic abort limits are switched out either automatically by the flight programmer or manually by the crew according to mission rules. Provision is also made for an abort request light to be energized from the ground control center. At the ground control center, all of the various crew safety system parameters are monitored by using telemetry information from the vehicle. Other telemetered data is available at the MCC so that the flight director can scan all flight critical data and warn the flight crew by voice communication of any impending danger. This facility provides an early warning to the flight crew by giving information on trends of various vehicle parameters, thereby alerting them to certain types of failure indications which may appear on their display panel. The flight crew will not abort on the telemetry information alone but they may use it as backup data for an abort decision.

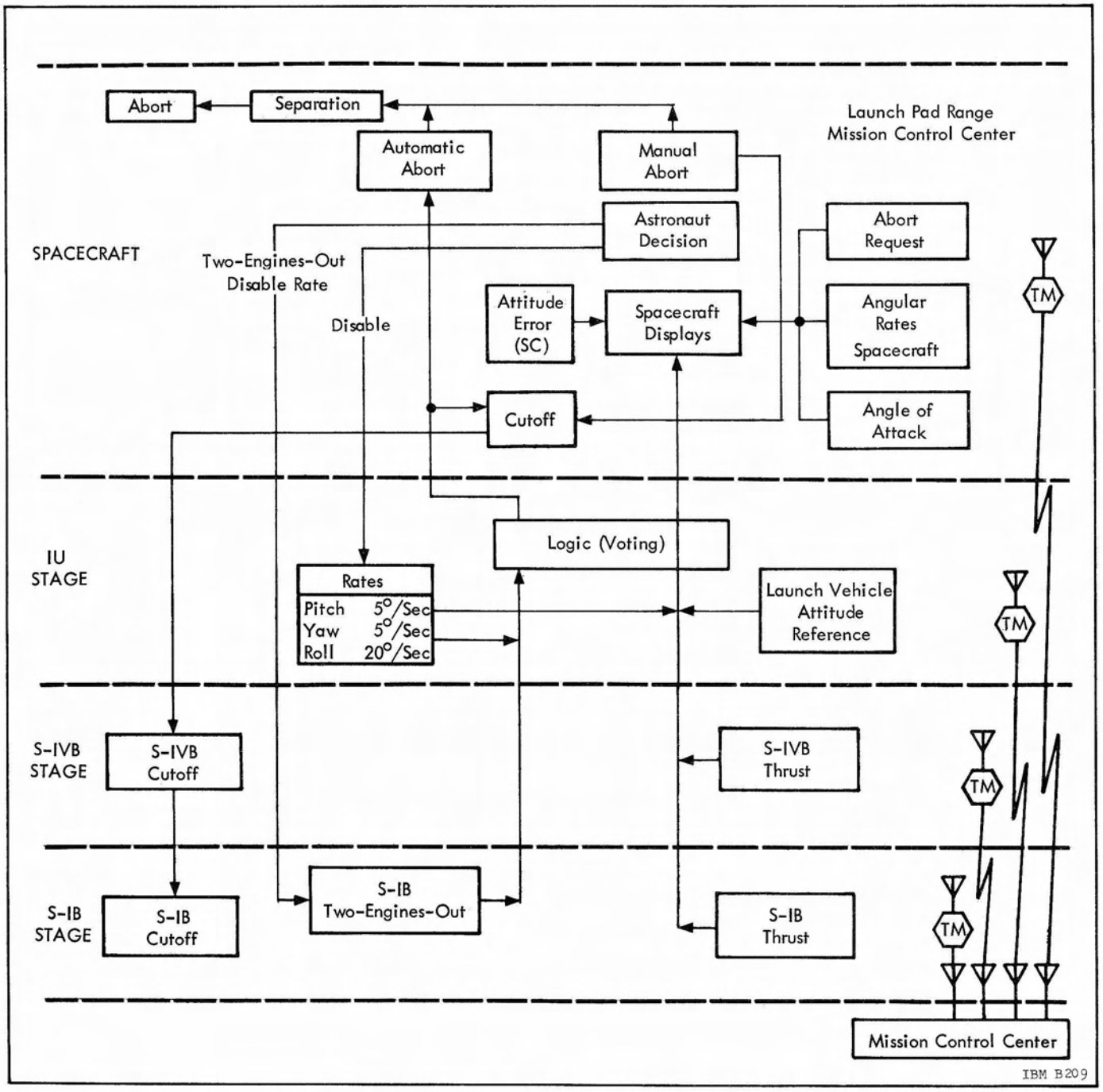

Figure 9.2-1 Crew Safety System (Saturn IB)

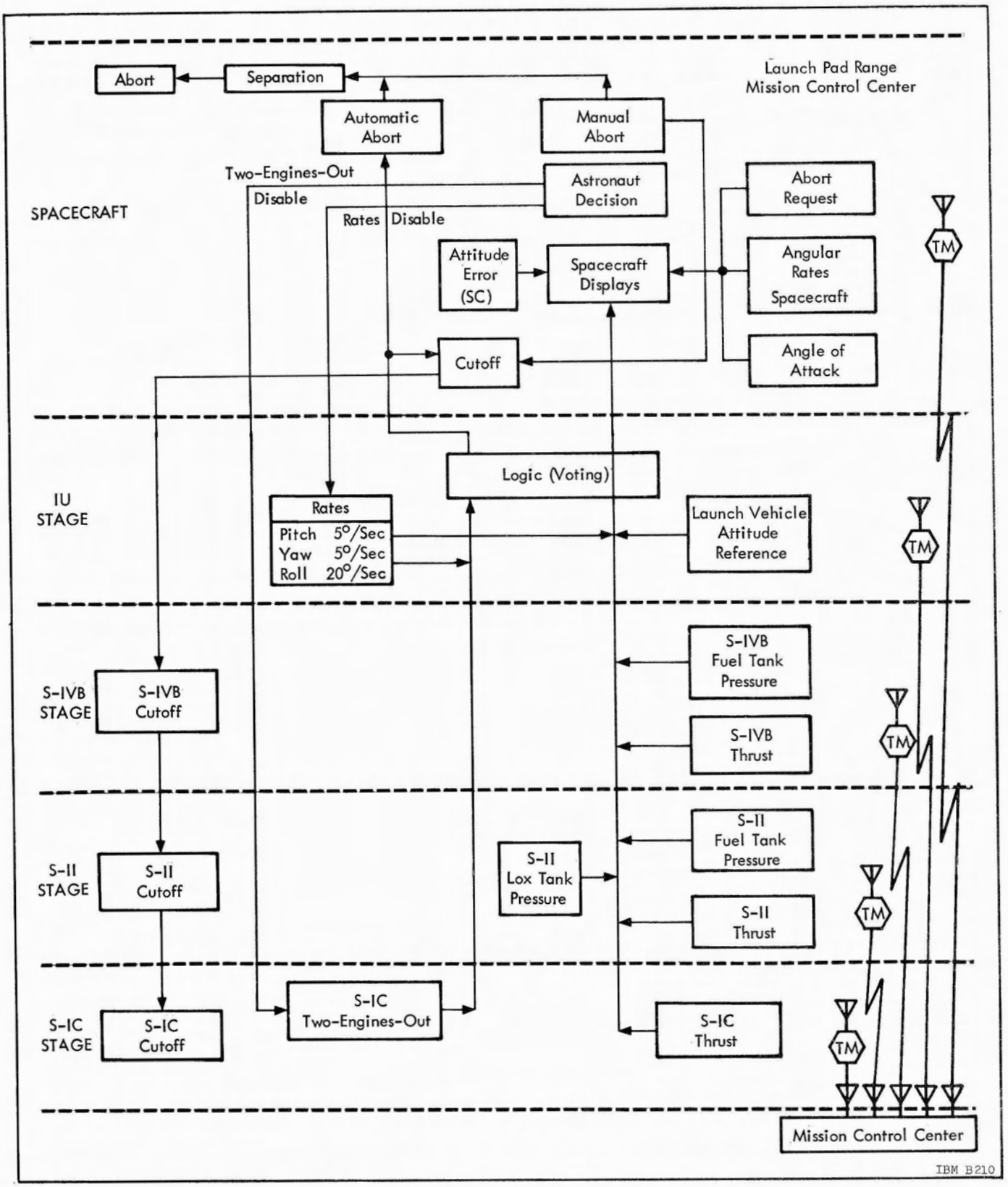

Figure 9.2-2 Crew Safety System (Saturn V)

SECTION 9.3

EDS SYSTEM OPERATION FOR SATURN V VEHICLES

9.3.1 GENERAL CONSIDERATIONS

A signal from the Spacecraft to the ground will indicate that no automatic abort signal is active prior to launch release. A signal at lift-off will automatically activate the EDS automatic abort mode. Provisions will also be made to manually interrupt the entire automatic abort signal in the Spacecraft.

An automatic abort will initiate engine shutdown on the active stage and the Spacecraft abort sequence.

Initiation of a manual abort will be based on at least two separate and distinct indications. These may be a combination of EDS sensor displays, physiological indications, and ground information to the Astronaut. In some cases, the two indications may come from the same parameter, but the indication and sensor systems will be independent.

In the event of conflicting information from the onboard EDS and telemetered data relayed to the Spacecraft from the ground, the onboard information will always take precedence.

Prior to a certain flight time (to be determined by range safety constraints), abort commanded engine shutdown capability will be locked out by provisions in the launch vehicle circuitry.

A signal will be provided to the Spacecraft to energize the abort request indicator light when the range safety officer commands destruct system arming. This command also terminates engine thrust.

Triple redundant electrical circuits utilizing majority voting logic will be used for all automatic abort signals. Redundant circuitry will be used for manual abort indication from the launch vehicle to the Spacecraft. Batteries used for EDS will be electrically isolated from each other. No single-point electrical failure in the onboard EDS will result in an abort.

Provision is made to manually shut down the engines on any stage from the Spacecraft without initiating an abort. A redundant means for accomplishing EDS-commanded engine shutdown is provided.

Provision is also made in the Spacecraft and launch vehicle for a manual initiation of staging (S-II and S-IVB). These provisions will enable abort into orbit.

9.3.2 EMERGENCY DETECTION PARAMETERS FOR AUTOMATIC ABORT (SATURN V)

Angular Overrates. This automatic abort parameter covers all control failures which rapidly lead to an excessive angle of attack and subsequent vehicle breakup. Information will be supplied by the control EDS Rate Gyro package which consists of three rate gyros for each control plane. These gyros are located in the Instrument Unit. An automatic abort will be initiated when 2 out of 3 gyros in any plane indicate that permissible angular rates are exceeded.

Provisions are made to manually deactivate the automatic abort signal for all 3 planes simultaneously with 1 switch located in the Spacecraft. Manual deactivation time is to be established by mission rules. Capability for deactivating either the roll or pitch/yaw/roll signals by sequencing, prior to first stage inboard engine cutoff, will be available within launch vehicle circuitry.

Adjustable sensor limit settings are provided in pitch and yaw within 2 to 10 degrees/second and in roll within 5 to 20 degrees/second. Sensing hardware must be removed from the launch vehicle to accomplish these adjustments.

S-IC Two-Engines-Out. The loss of thrust on two or more engines will initiate an automatic abort. This automatic abort mode covers failures occurring near the pad and possible range safety action. Deactivation of the automatic abort capability prior to inboard

engine cutoff arming is provided by the launch vehicle sequencer.

This automatic abort capability may be manually deactivated from the Spacecraft. Manual deactivation times will be established by mission rules.

A minimum of two thrust sensors are used on each S-IC engine to provide inputs into the EDS circuitry. Action of at least 2 sensors are required to indicate loss of engine thrust.

9.3.3 EMERGENCY DETECTION PARAMETERS FOR MANUAL ABORT (SATURN V)

S-IC Stage Thrust. The status of each engine of the S-IC Stage is displayed in the Spacecraft (five indicator lights). Upon loss of engine thrust, these engine status lights are energized by a discrete signal.

- An abort for one-engine-out will be governed by mission rules.
- A minimum of two thrust sensors are used on each S-IC engine to activate the engine-out status lights.

S-II Stage Thrust. The status of each engine of the S-II Stage is to be displayed in the Spacecraft (five indicator lights). Upon loss of engine thrust, these engine status lights are energized by a discrete signal.

- Abort on one-engine-out will be governed by mission rules.
- A minimum of two thrust sensors are used on each S-II engine to activate the engine-out status lights.
- Transition from S-IC monitoring to S-II monitoring at staging is accomplished within the launch vehicle circuitry.

S-IVB Stage Thrust. The status of the S-IVB engine thrust is displayed in the Spacecraft (one indicator light). Upon loss of engine thrust, the engine-out status light is energized by a discrete signal.

- Engine thrust is monitored throughout S-IVB burn.
- Abort because of thrust loss is governed by mission rules.
- A minimum of two thrust sensors are used on the S-IVB engine to activate the engine-out status light.
- Transition from S-II monitoring to S-IVB monitoring at staging is accomplished with the launch vehicle circuitry.

Staging Sequence. Physical separation of stages including the S-II second plane separation, are indicated in the Spacecraft by lights, or other suitable discrete indications. In case of no separation, abort will be governed by mission rules.

Launch Vehicle Attitude Reference Failure. Improper operation of the launch vehicle attitude reference (sensed by the IU guidance and control system) will energize an indicator light in the Spacecraft.

Abort or switchover to Spacecraft guidance will be governed by mission rules.

Angle of Attack. An angle-of-attack function is displayed by an analog indicator in the Spacecraft. This parameter is an indication of slow control failures which lead to excessive angles of attack.

The measured pitch and yaw components are combined in vector form into a total angle-of-attack indication.

The type of measurement to be displayed and the limit settings (if necessary, as a function of flight time) will be determined later. Limit settings will govern abort action.

S-II Propellant Tank Pressures. LO_2 and LH_2 tank pressures in the S-II Stage are displayed in the Spacecraft by means of an analog display. This parameter requires a redundant sensor and display system.

S-IVB Propellant Tank Pressures. LO_2 and LH_2 tank pressures in the S-IVB Stage are displayed in the Spacecraft by means of an analog display. This parameter requires a redundant sensor and display system.

Attitude Error (Spacecraft). Attitude errors from the Spacecraft guidance and navigation system are displayed in analog form on the flight director attitude indicator. This parameter is an indication of slow control failures leading to excessive angles of attack or excessive attitudes.

The Spacecraft guidance and navigation system will be preprogrammed with the launch vehicle tilt program for the S-IC flight period. Limit settings as a function of flight time (to be determined later) will govern abort actions.

Angular Rates. A single launch vehicle overrate indicator light in the Spacecraft is energized by the IU Control EDS Rate Gyro package when permissible angular rates are exceeded in any plane. This indication primarily covers the flight period in which the overrate automatic abort capability is deactivated.

Spacecraft angular rates are presented by analog display on the flight director attitude indicator. The sensing device for this information is the Apollo rate gyro package. Limit settings, as a function of flight time, determine abort actions.

9.3.4 SATURN IB EDS OPERATION SYSTEM

The EDS operation for Saturn IB is different only in the following areas:

- In the S-IB Stage, eight engines are monitored (five in Saturn V).
- Since the Saturn IB has no S-II Stage, any function connected with this stage does not exist in Saturn IB EDS.
- The S-IVB fuel tank pressure is not monitored in Saturn IB Vehicles.

Figure 9. 3-1 is a plot of the critical angle of attack (α) versus flight time for the Saturn IB Vehicle. Various engine deflection angles (β) are included. Limits for the critical angle of attack (during the time of maximum dynamic pressure) are shown in Figure 9. 3-2. Abort criteria is summarized in Table 9. 3-1 and EDS design ground rules are listed in Table 9. 3-2.

Table 9. 3-1 Abort Criteria and Ground Rules

Auto-Abort Parameters:

- Angular overrates
- Loss of thrust on two or more S-IB Engines

Indications for Manual Abort:

- S-IB thrust (eight indicator lights)
- S-IVB thrust (one of the eight S-IB indicator lights)
- Staging sequence (use of S-IB thrust indicator lights)
- Launch vehicle attitude reference fail (one indicator light)
- Angle-of-attack (Q-ball on meter)
- Attitude error (SC-G&N system on flight director attitude indicator)
- Angular overrates (one indicator light)
- Abort request (one indicator light for range safety cutoff and destruct arming signal path is either through Spacecraft up-data RF link or through launch vehicle hardwire prior to lift-off)

Manual Abort Ground Rules

Manual abort will be governed by mission rules within the following ground rules:

- Manual abort will be initiated based on at least two separate and distinct indications.
- No abort will be initiated over RF; an abort request will be given based on telemetered data but the onboard information shall always take precedence.

Table 9.3-2 Saturn IB EDS Design Ground Rules

EDS Design Ground Rules:

- Reliability goals:

  Probability of detecting failure - 0.9973
  Probability of not detecting false failure - 0.9997

- No single failure in EDS circuits will cause a true failure from being detected or a false failure being detected.
- All failures that jeopardize crew safety will be designed out if possible.

How Design Ground Rules are Being Achieved:

- Use of 2 out of 3 voting circuits in the automatic abort capability
- Use of redundancy in the indications for manual abort capability
- Complete EDS checkout during countdown
- Interlocking EDS-ready in lift-off circuits
- Interlocking J-2 engine-ready with ignition
- Interlocking separation with S-IVB ignition

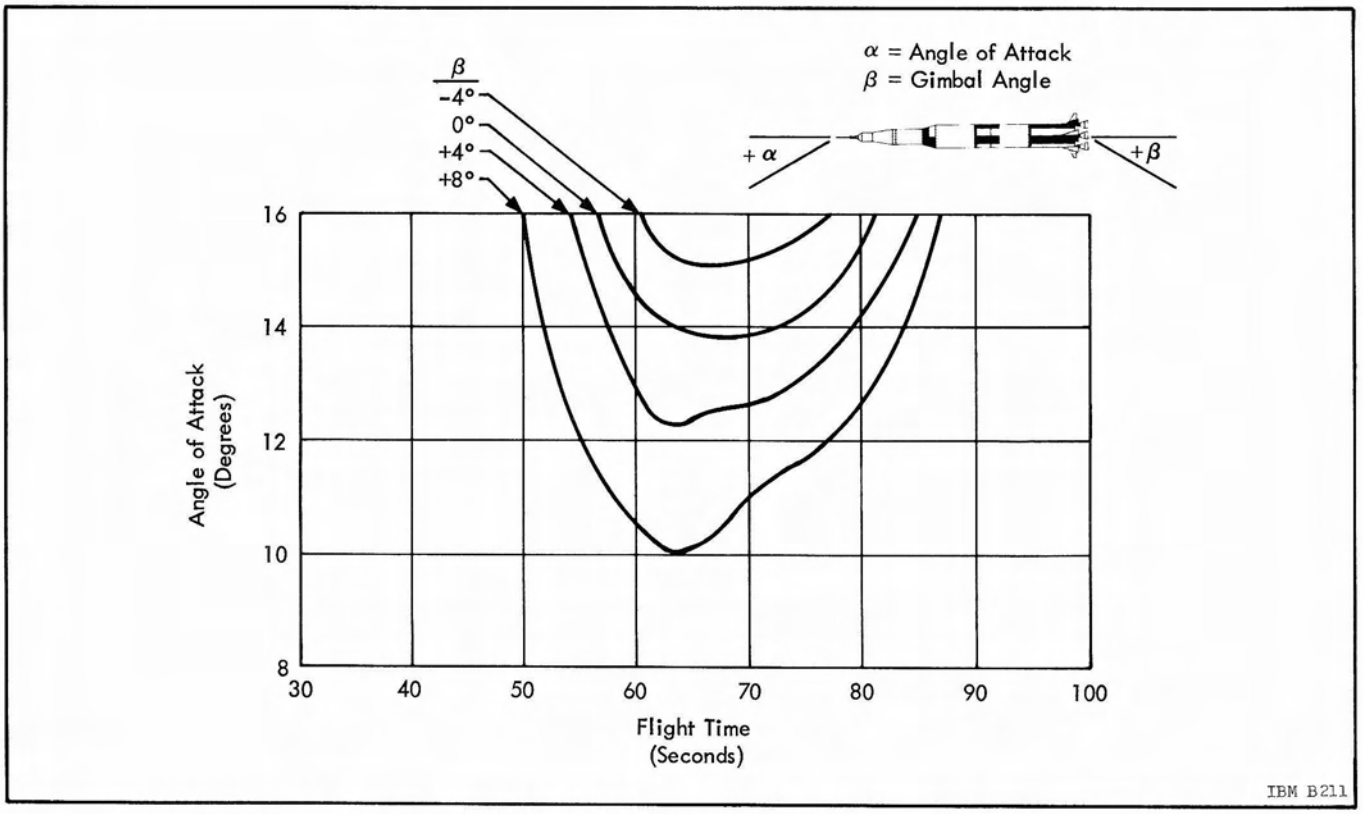

Figure 9.3-1 Saturn IB Critical Angle of Attack Versus Flight Time

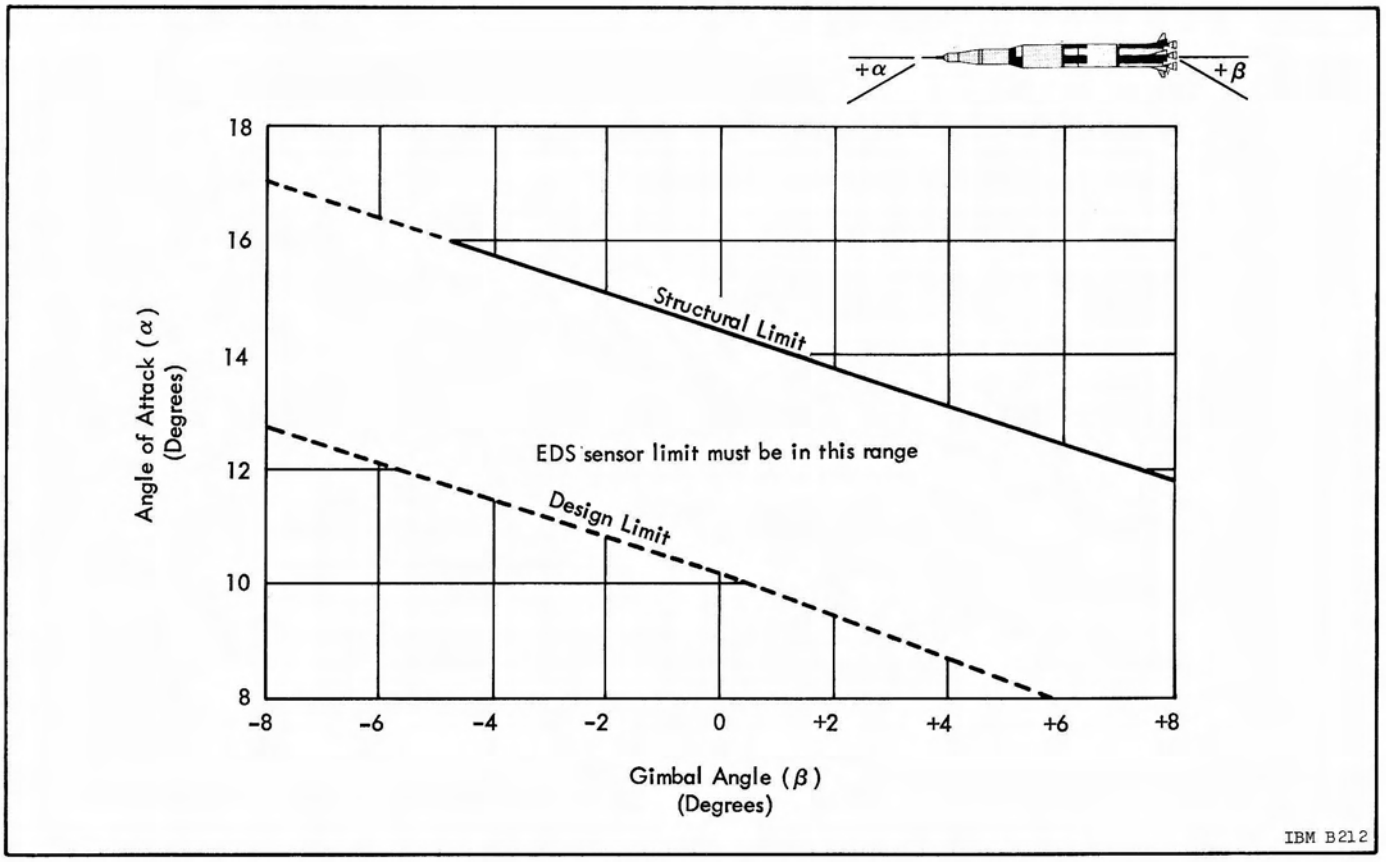

Figure 9.3-2 Saturn IB Critical Angle of Attack Versus Gimbal Angle (76 Seconds)

CHAPTER 10

LAUNCH SITE SUPPORT SYSTEMS

(To be supplied at a later date)

CHAPTER 11
OPERATIONAL PHASES OF THE ASTRIONICS SYSTEM

(To be supplied at a later date)

PART II

HARDWARE DESCRIPTION

CHAPTER 12

INSTRUMENT UNIT

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SECTION 12.1

INSTRUMENT UNIT

The Instrument Unit is a cylindrical structure 6. 6 meters (260 inches) in diameter and 0. 9 meters (36 inches) in height, mounted on top of the S-IVB Stage as illustrated in Figure 12. 1-1.

The electronic equipment boxes of the Saturn Astrionics System are mounted on cold plates which are attached to the inner side of the cylindrical structure. The electronic equipment in the S-IVB Stage is mounted in a similar way (Figure 12. 1-1). This arrangement provides clearance for the landing gear of the Lunar Excursion Module sitting on top of the IU and for the bulkhead of the S-IVB tank extending into the IU.

The structure of the IU consists of three 120-degree segments of aluminum honeycomb sandwich-joined to form a cylindrical ring. After assembly of the IU, a door provides access to the electronic equipment inside the structure. This access door has been designed to act as a load carrying part of the structure in flight. In addition, the structure contains an umbilical door which is spring-loaded and will close after retraction of the umbilical arm at lift-off. The IU structure provides a path for static and dynamic loads resulting from the payload above the IU.

Typical arrangement of the equipment in the IU for operational and R & D Saturn Vehicles is illustrated on Figures 12. 1-2 through 12. 1-7.

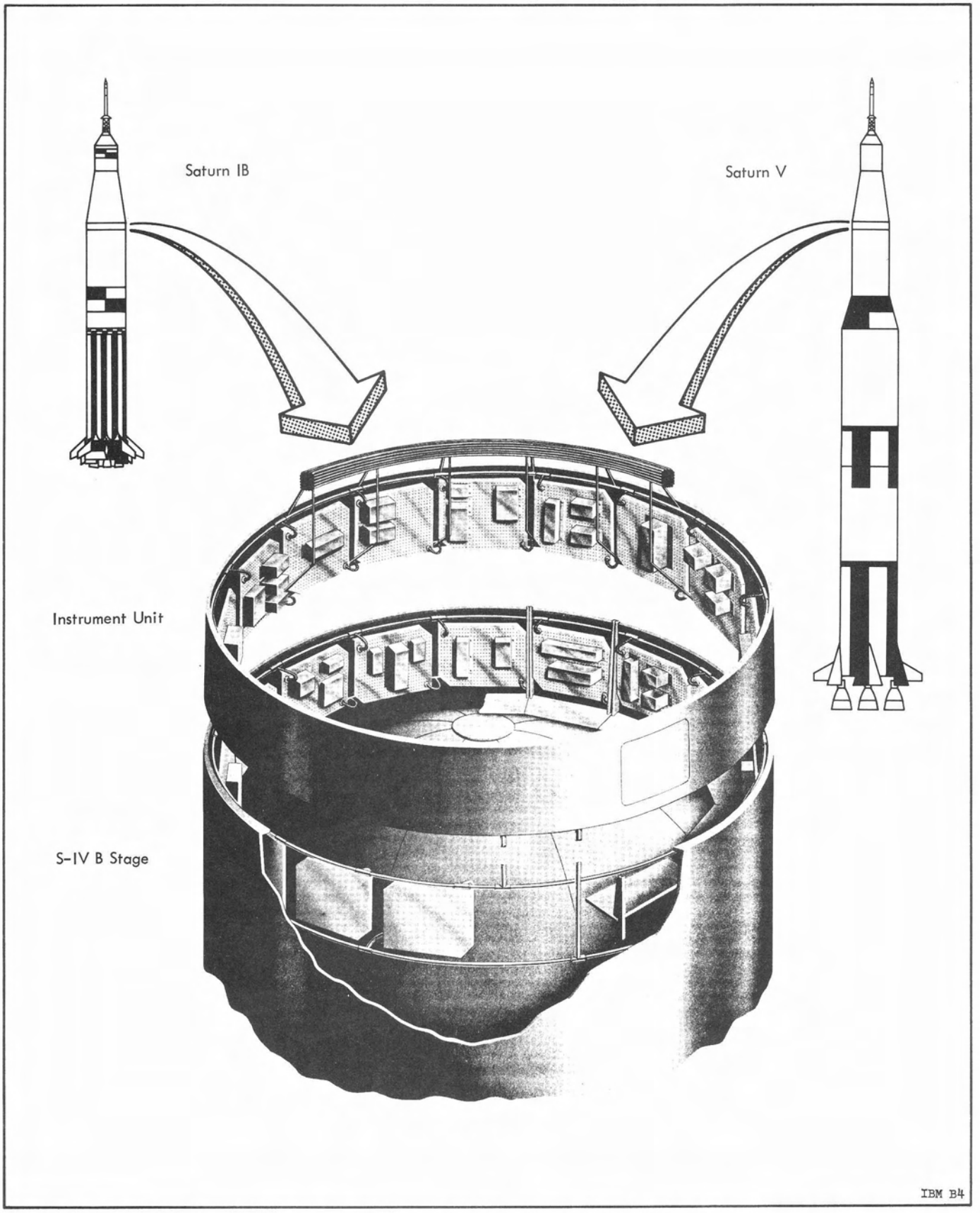

Figure 12.1-1 Saturn IB and V Instrument Unit Physical Location

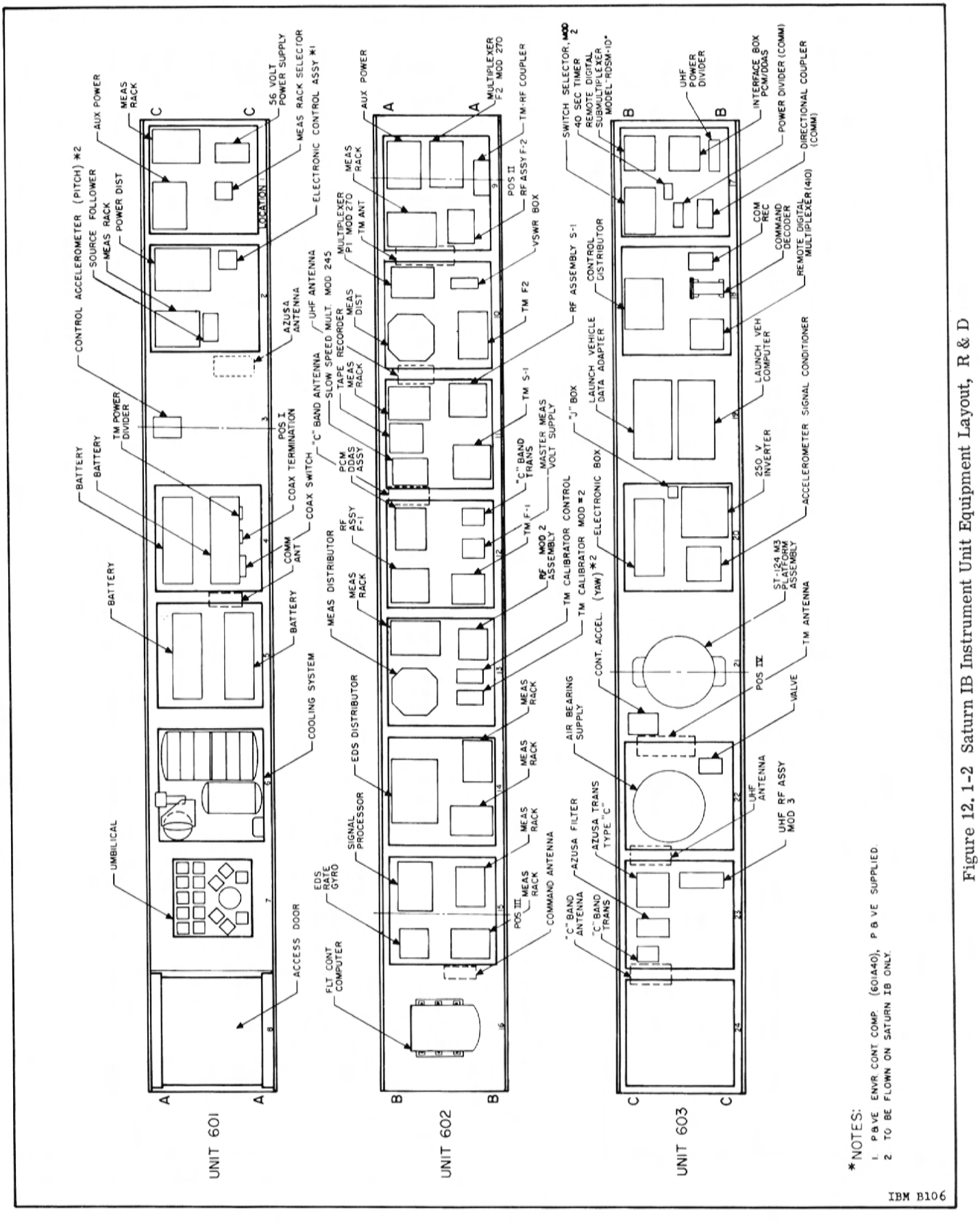

Figure 12.1-2 Saturn IB Instrument Unit Equipment Layout, R & D

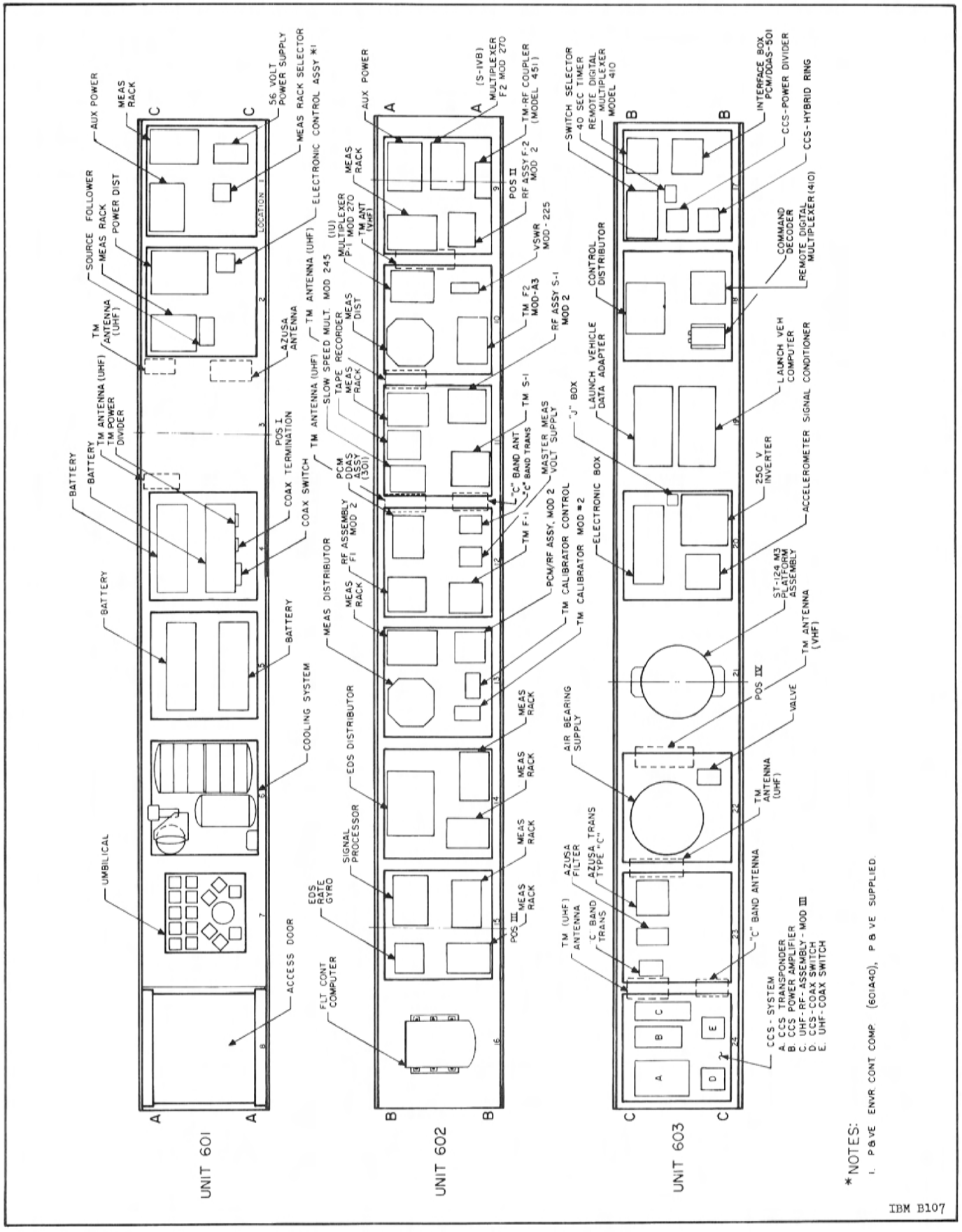

Figure 12.1-3 Saturn V Instrument Unit Equipment Layout, R & D

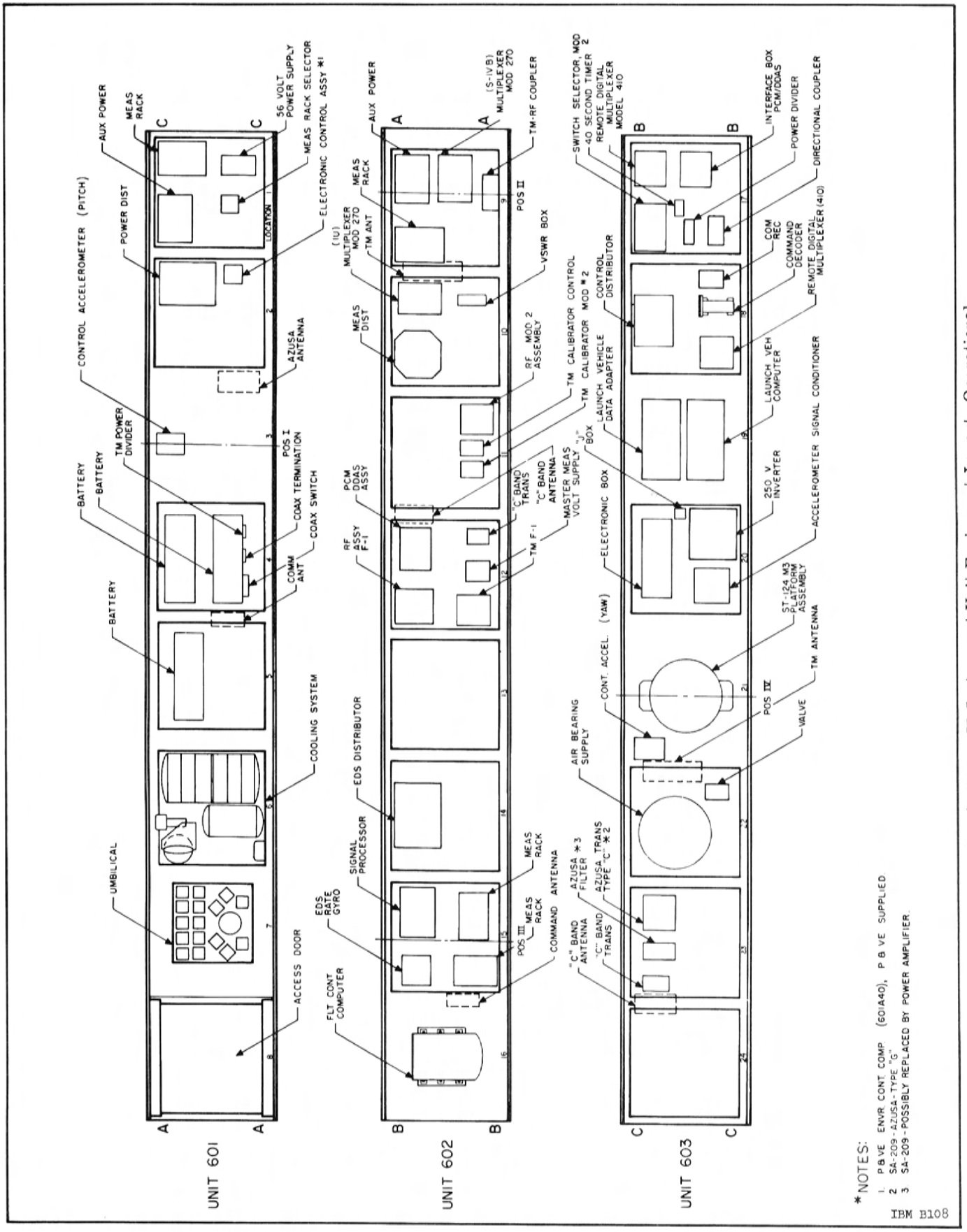

Figure 12.1-4 Saturn IB Instrument Unit Equipment Layout, Operational

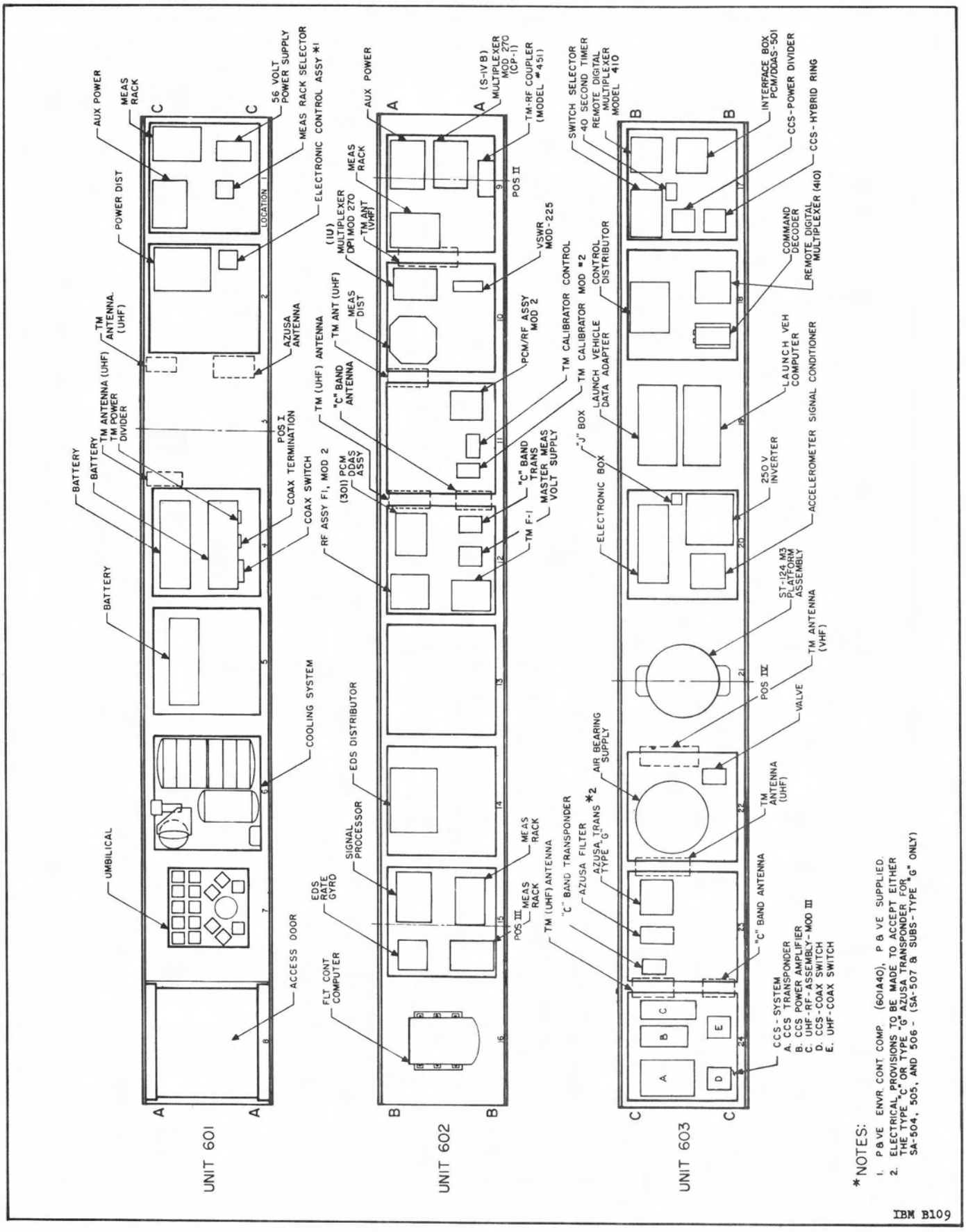

Figure 12.1-5 Saturn V Instrument Unit Equipment Layout, Operational

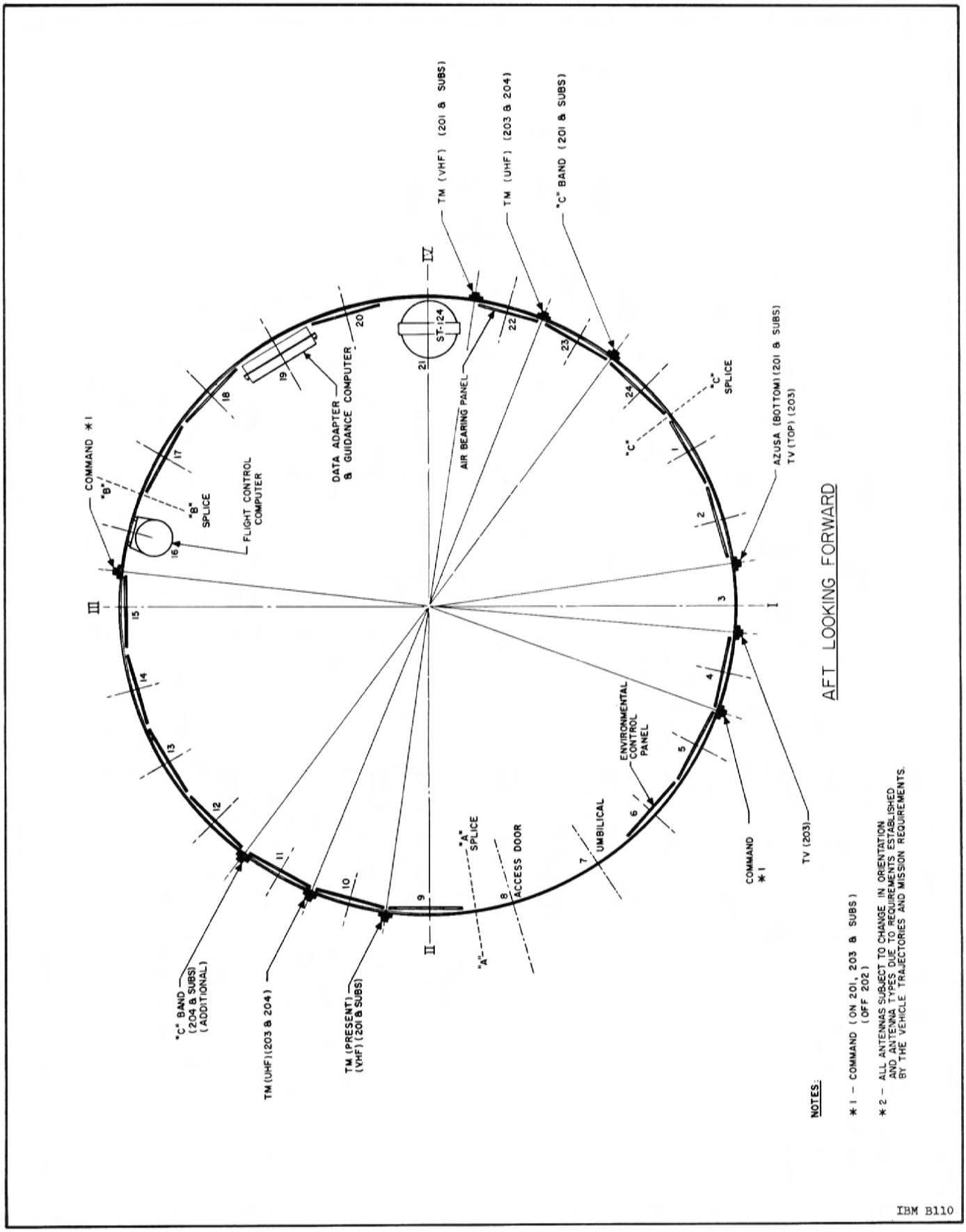

Figure 12.1-6 Saturn IB Instrument Unit Equipment Layout, Antenna Orientation

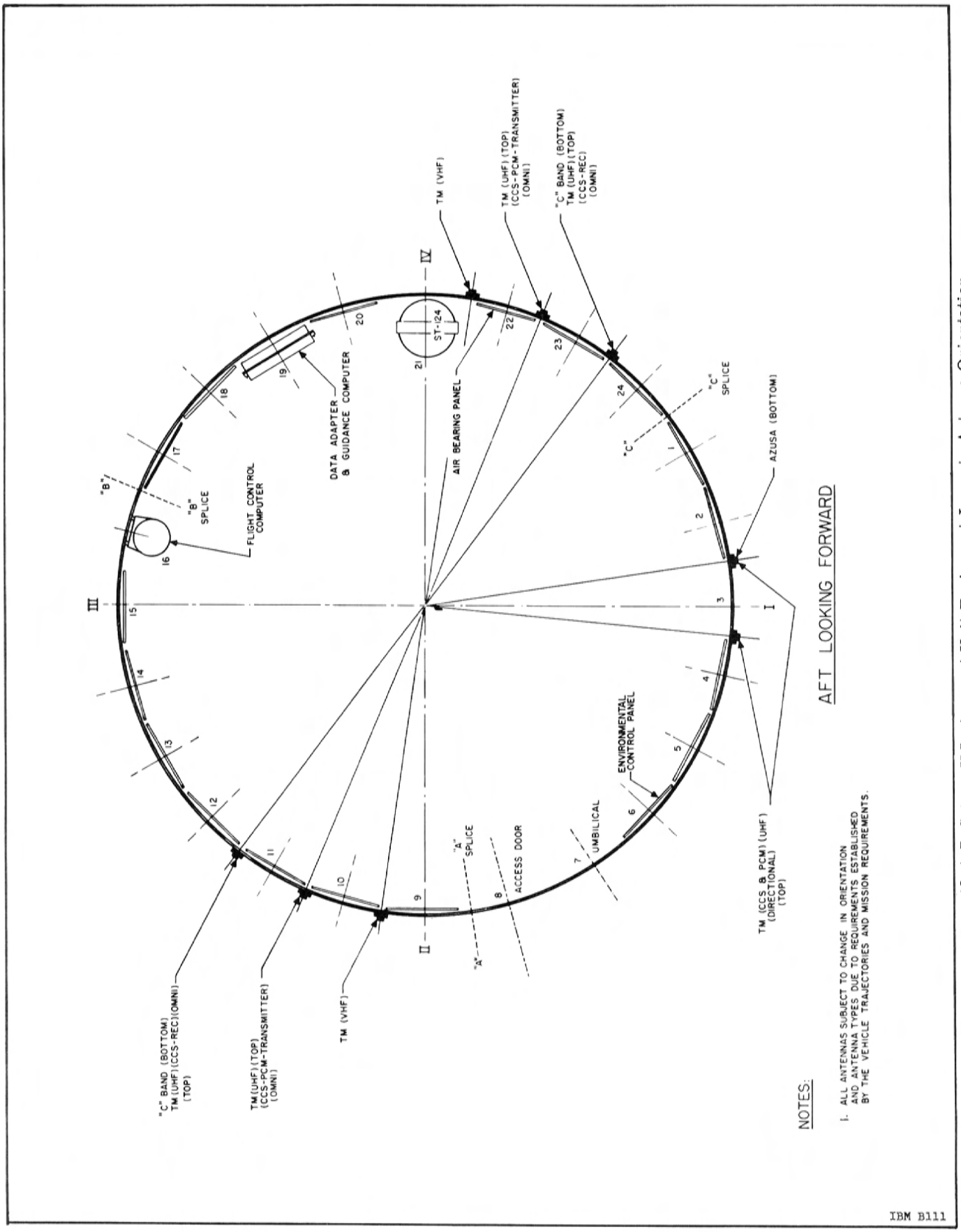

Figure 12.1-7 Saturn V Instrument Unit Equipment Layout, Antenna Orientation

CHAPTER 13

ENVIRONMENTAL CONTROL SYSTEM

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SECTION 13.1

THERMAL CONDITIONING SYSTEM

A thermal conditioning system is provided in the S-IVB Stage and Instrument Unit of the Saturn IB and V Launch Vehicles. This system is required since cooling of the Astrionics equipment by radiation is inadequate. The thermal conditioning system furnishes cooling during prelaunch and flight.

The thermal conditioning system contains 16 thermal conditioning panels (cold plates) in the S-IVB Stage and 16 in the Instrument Unit. Most of the equipment which requires cooling is mounted on the cold plates; however, some equipment such as the Launch Vehicle Digital Computer and Data Adapter have integral cooling passages and are not mounted on cold plates. Each cold plate measures 76.2 centimeters by 76.2 centimeters (30 inches by 30 inches) and contains tapped bolt holes positioned on a 5.1-centimeter (two-inch) square grid. (A cold plate is illustrated in Figure 13.1-1.) This hole pattern permits maximum flexibility of component mounting on the cold plates.

A coolant fluid of 60 percent methanol and 40 percent water by weight is circulated through the cold plates and equipment having integral cooling passages. Each cold plate is capable of dissipating approximately 420 watts.

A diagram of the environmental control system is shown in Figure 13.1-2. The manifold and methanol-water accumulator are filled with coolant through either of the quick disconnects at the S-IVB/IU interface. Also, any air which may be trapped during filling is bled out through these disconnects. The methanol-water accumulator provides damping of pressure fluctuations, a constant pump inlet pressure, compensation for thermal expansion of the coolant, and will supply additional coolant should any be lost.

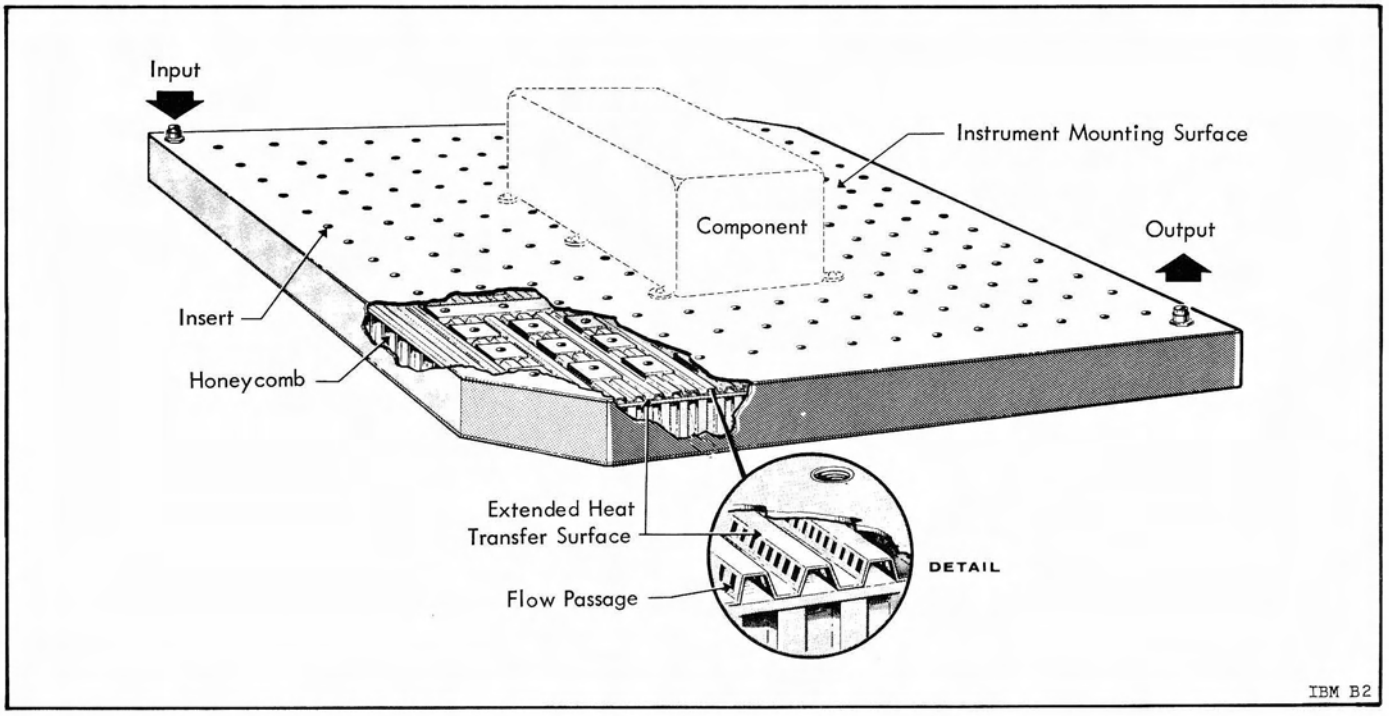

Figure 13.1-1 Thermal Conditioning Panel Details

The methanol-water accumulator and water accumulator are pressurized with gaseous nitrogen (GN_2) that is stored at 20.7 x 10^6 N/m^2g (3000 psig) in the two 819.4-cubic centimeter (50-cubic inch) storage spheres. The gaseous nitrogen is filtered by filter A, reduced to approximately 103.5 x 10^3 N/m^2a (15 psia) by the pressure regulator, and then applied to the methanol-water accumulator. The orifice assembly reduces the 103.5 x 10^3 N/m^2a (15 psia) gaseous nitrogen to 34.5 x 10^3 N/m^2a (5 psia) and this pressure is used to pressurize the water accumulator. The orifice assembly also vents excess pressure into the Instrument Unit compartment to prevent overpressurizing the water accumulator. A flexible membrane is contained within both accumulators and provides a barrier that prevents mixing of the gaseous nitrogen and liquid.

The bleeder assembly is opened during filling of the accumulators. This provides an escape port for air which could otherwise be trapped and allows the flexible membranes in the accumulators to retract.

Filling of the water accumulator is accomplished manually by pouring water into the accumulator through the water fill port. The flow of water from the water accumulator to the sublimator is controlled by solenoid valve C. This valve is energized (closed) during prelaunch operations since cooling of the methanol-water coolant is accomplished by the preflight heat exchanger.

Filling of the two 50-cubic inch storage spheres with gaseous nitrogen is controlled by pressure switch A and solenoid valve A. A high pressure source of gaseous nitrogen is applied to the GN_2 supply & emergency vent quick disconnect. Pressure switch A, calibrated through the calibrate quick disconnect, indicates when the pressure in the spheres is approximately 20.7 x 10^6 N/m^2g (3000 psig). At that time solenoid valve A is closed and the gaseous nitrogen source can be removed.

During prelaunch operations, the methanol-water coolant is circulated by the electrically driven pump through a closed-loop system. The coolant flows through the coolant temperature sensor, orifice B, and then through the cold plates and integrally cooled equipment within the Instrument Unit. A decrease in diameter of the coolant piping causes a portion of the coolant to flow through the gas bearing heat exchanger while orifice B diverts a portion of the coolant to the cold plates in the S-IVB Stage. The coolant in the return line either passes through the sublimator and preflight heat exchanger to the pump or flows through the bypass line to the pump, thus completing the closed loop.

The coolant temperature sensor, located at the pump outlet, senses the coolant temperature and supplies an electrical signal to the electronic control assembly which controls the modulating flow control valve. The modulating flow control valve diverts varying amounts of coolant through the sublimator and preflight heat exchanger if the coolant requires cooling, or if no cooling is required, the coolant is bypassed around the sublimator and heat exchanger.

As previously mentioned, during prelaunch operations the sublimator is inactive and the preflight heat exchanger cools the closed-loop coolant. A temperature controlled methanol-water mixture, supplied by the ground support equipment, is circulated through one section of the preflight heat exchanger, thus cooling the closed-loop coolant that flows through the other section.

During flight, the operation is the same except that the sublimator is active and the preflight heat exchanger in inactive. However, the sublimator does not operate until approximately 200 seconds after lift-off, at which time the ambient pressure is low enough to sustain sublimation. Calculations indicate that during the transient phase, the thermal capacity of the electronic equipment and thermal conditioning system is sufficient to prevent over-heating of the equipment.

When the ambient pressure is low enough for sublimation, solenoid valve C is de-energized (opens) allowing water to flow from the water accumulator to the sublimator. Water under pressure enters the sublimator and flows into the pores of the porous plate. As the water in the pores encounters the space vacuum at a temperature and pressure below the triple point of water, an ice layer forms at the outer water surface and continues to build-up back towards the water passage. As heat is transferred through the water passage and ice layer, the outer surface sublimes overboard. As the heat level is increased, the ice sublimes at a faster rate, increasing the water flow rate. The converse is also true.

In addition to the previous description of sublimator operation, a theory exists that two modes of heat transfer occur in the sublimator. This theory—sublimation and evaporation—is as follows:

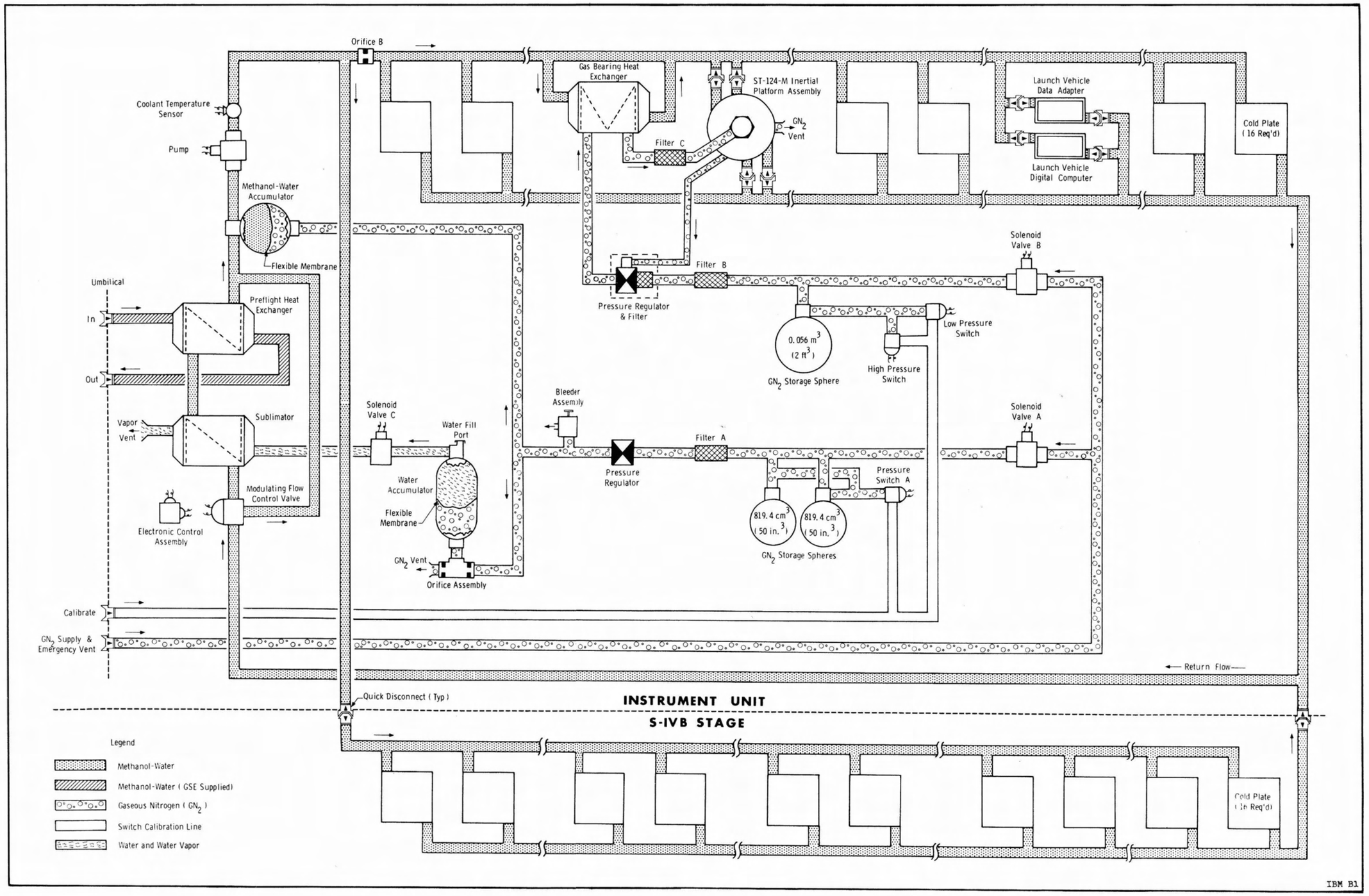

Figure 13.1-2 Environmental Control System Mechanical Diagram

Water under pressure enters the sublimator (refer to Figure 13.1-3) and flows into the pores of the porous plates. As the water in the large pores encounters the space vacuum, freezing occurs and an ice plug is formed. In the small pores which are non-wetted and can retain water by surface tension, the water fills the pores to a distance where the restriction is small enough to retain water at the inlet pressure. As the heat flux increases, the ice in the large pores sublimes at the solid-vapor interface and is formed at the liquid-solid interface. The vapor or steam is vented overboard. When the heat flux becomes great enough to prevent all ice from existing, any further increase in the heat load will raise the evaporation temperature. The heat load reaches a maximum when no ice exists and the heat sink temperature is zero degrees centigrade (32 degrees fahrenheit).

As can be seen the sublimator has an advantage over a heat exchanger in that the flow of water is self-regulating—as the heat flux decreases ice plugs are formed in the pores and the flow of water also decreases.

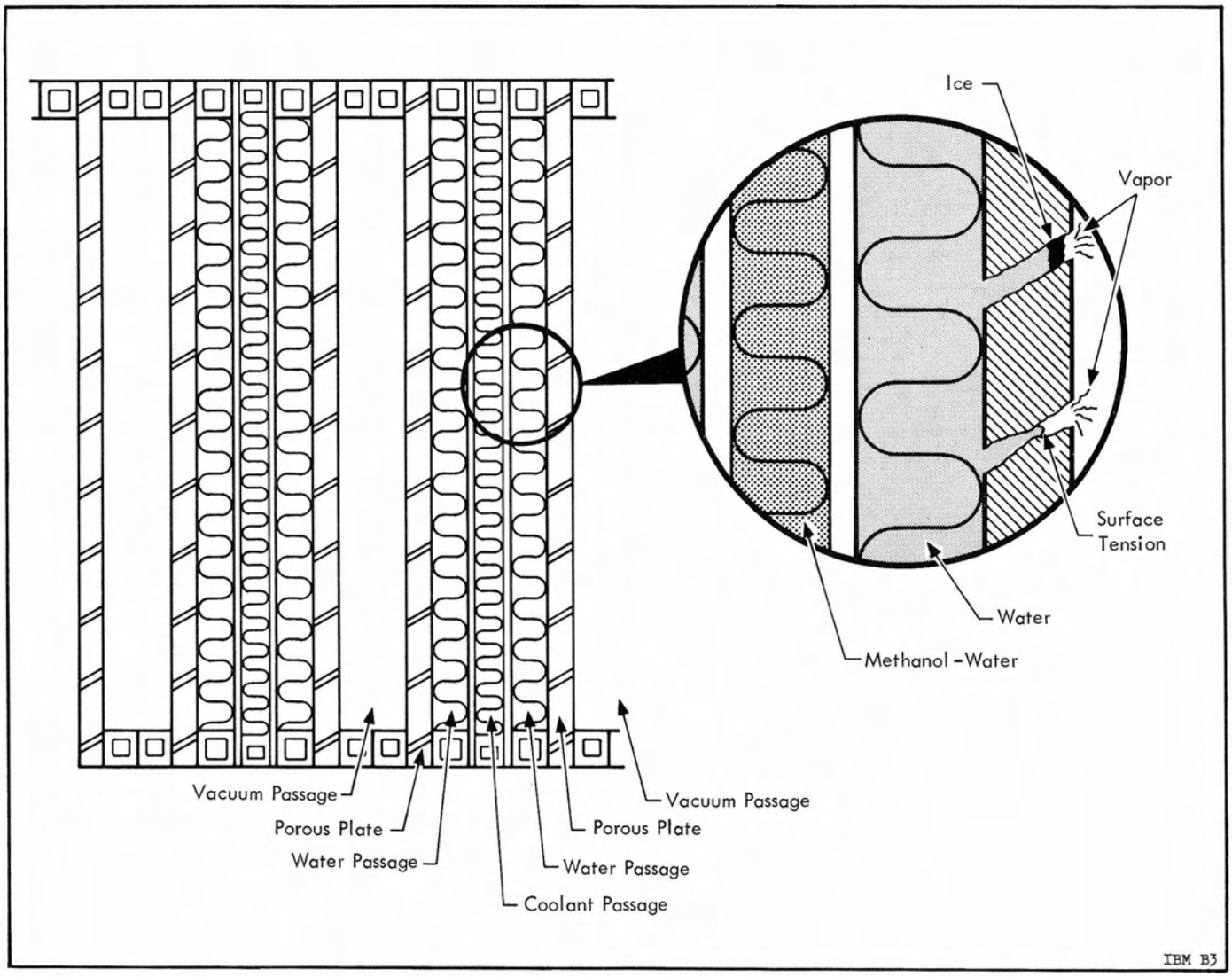

Figure 13.1-3 Sublimator Details

SECTION 13.2

GAS BEARING SUPPLY SYSTEM

The gas bearing supply system furnishes gaseous nitrogen at a regulated temperature and pressure for lubrication of the gas bearings in the ST-124-M Inertial Platform Assembly.

The gas bearing supply is filled by connecting a high pressure source of gaseous nitrogen to the GN_2 supply & emergency vent quick disconnect (refer to Figure 13.1-2). The high pressure switch, calibrated through the calibrate quick disconnect, indicates when the pressure in the 0.056-cubic meter (2-cubic foot) storage sphere is approximately 20.7×10^6 N/m^2g (3000 psig). At that time solenoid valve B is closed and the gaseous nitrogen source can be removed.

The gaseous nitrogen flows from the storage sphere, is filtered by filter B, and reduced to a pressure suitable for lubrication of the gas bearings by the pressure regulator and filter. The gaseous nitrogen is cooled or heated as required as it passes through the gas bearing heat exchanger, is filtered by filter C, and then applied to the gas bearings in the platform. After lubricating the gas bearings, the gaseous nitrogen is vented into the Instrument Unit compartment.

A reference pressure is fed-back from the platform to the pressure regulator and filter. This feed-back reference pressure maintains the pressure in the gas bearings constant by controlling the pressure regulator and filter output pressure; i.e., a decrease in pressure in the gas bearings causes the pressure regulator and filter output to increase.

The low pressure switch, which is also calibrated through the calibrate quick disconnect, indicates when the pressure in the 2-cubic foot sphere decreases below approximately 6.9×10^6 N/m^2g (1000 psig). Should an indication of a pressure decrease occur during prelaunch operations, the platform would be shutdown until the 0.056-cubic meter (2-cubic foot) sphere could be repressurized. Under normal in-flight conditions, this should not happen unless a leak or malfunction is present in the system.

CHAPTER 14

STABILIZED PLATFORM

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SECTION 14.1

INTRODUCTION

The ST-124-M Inertial Platform system [1] (see Figures 14.1-1 and 14.1-2) provides the inertial reference coordinates, integrated acceleration data, and vehicle attitude measurements with respect to these coordinates for navigation, guidance, and control of the Saturn Launch Vehicles.

The platform system consists of 6 assemblies:

- ST-124-M Inertial Platform Assembly [2]
- Platform Electronic Assembly
- Accelerometer Signal Conditioner
- Platform AC Power Supply
- 56 Volt Power Supply
- Gas Bearing Supply

The Inertial Platform subsystem is self-contained and requires only inputs from the environmental conditioning system and the 28-volt dc power source.

The interface between the Platform system and other components of the Saturn navigation, guidance, and control system is shown in Figure 14.1-3. The accelerometer output signals are shaped by the

1 For the purpose of brevity, the ST-124-M Inertial Platform system will hereinafter (within Chapter 14) be referred to as the Platform system.

2 For the purpose of brevity, the ST-124-M Inertial Platform Assembly will hereinafter (within Chapter 14) be referred to as the Inerial Platform.

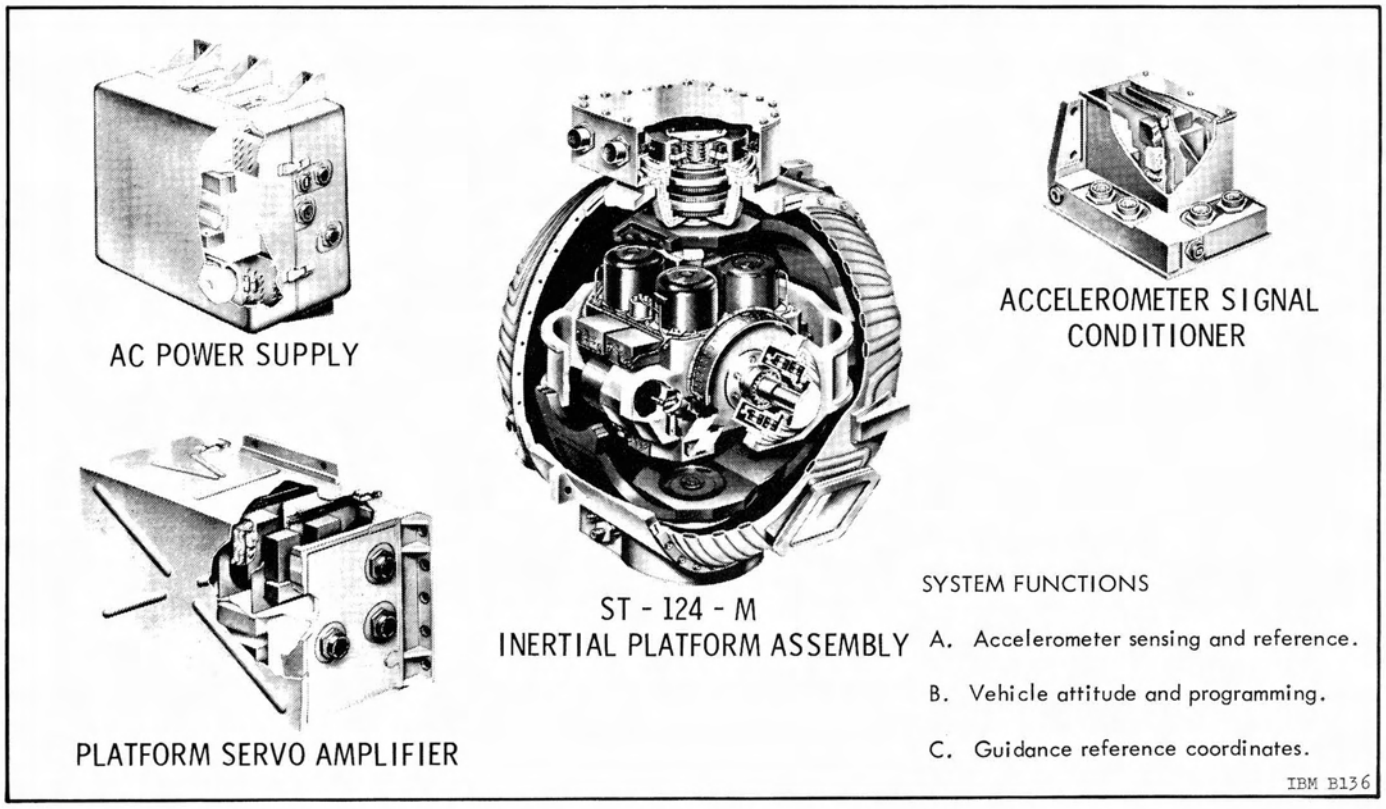


Figure 14.1-1 ST-124-M Inertial Platform System (Saturn IB and V)

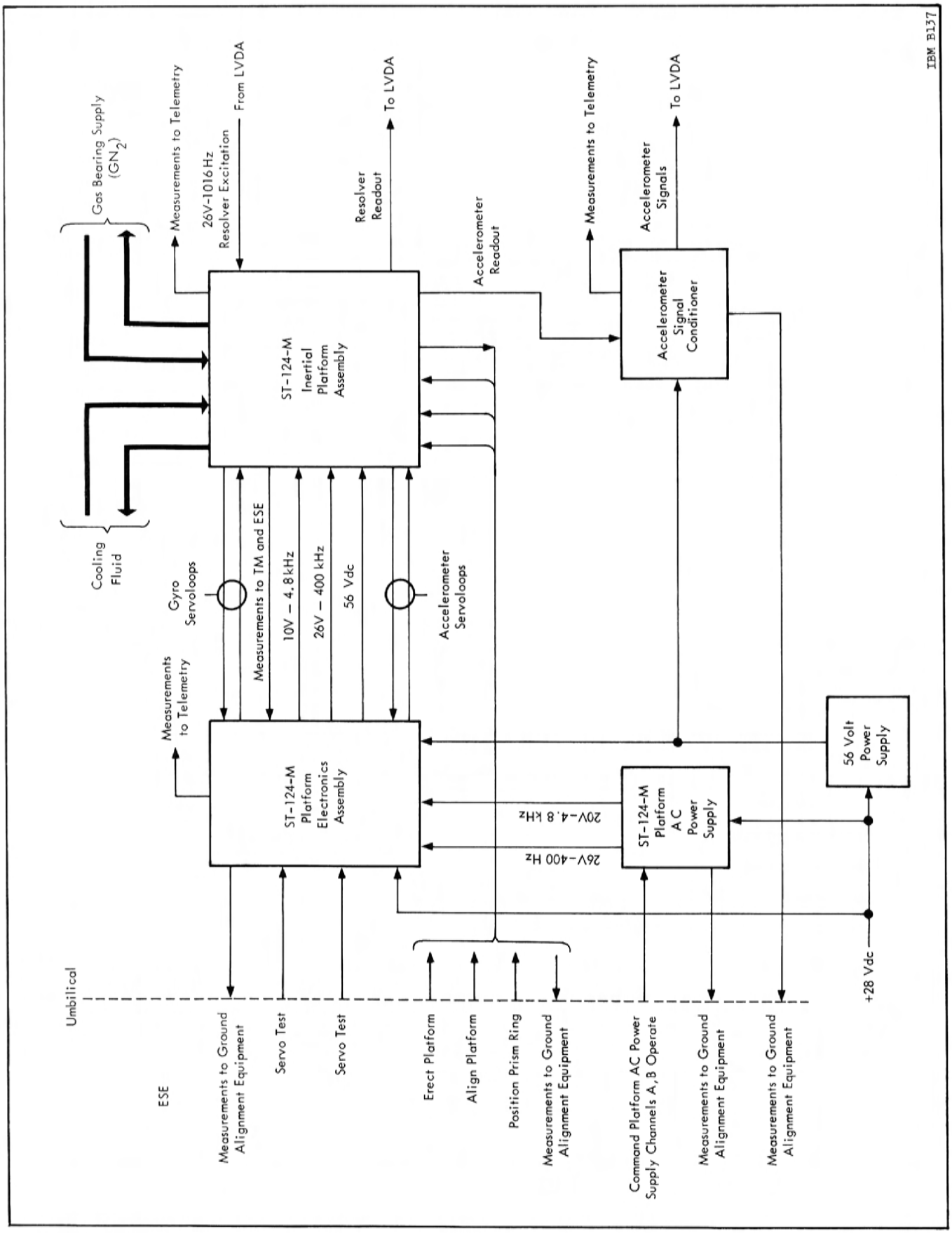


Figure 14.1-2 Inertial Platform Subsystem Block Diagram

accelerometer Signal Conditioner and then converted into a digital code by the accelerometer signal processor in the LVDA. The signals from the gimbal resolvers are converted to binary numbers in the crossover detector in the LVDA. The resolver chain output is used for prelaunch checkout only.

The Inertial Platform servo amplifier contains the solid state electronics to close the platform gimbal servoloops, the accelerometer servoloops, and an impulse function generator for automatic checkout of each servoloop.

ESE associated with the Platform system is located at the launch site and the launch control center. At the launch site, the azimuth-laying theodolite is located approximately 700 feet from the base of the vehicle. The theodolite installation transmits signals via underground cables to the platform ESE located in the launch umbilical tower. Platform system ESE in the launch umbilical tower consists of an inertial data box, an alignment amplifier panel, an azimuth control panel, a theodolite amplifier panel, and accelerometer monitor panels. The equipment contained in the launch umbilical tower interfaces with the onboard Inertial Platform sybsystem, the RCA-110A launch umbilical tower computer, and the data link. In the launch control center additional Inertial Platform ESE interfaces with the launch control center RCA-110A Computer and data link. This equipment consists of a platform checkout and monitor panel, a platform control panel, an azimuth laying panel, and an azimuth laying video monitor panel. Total remote control and automation of the Inertial Platform subsystem is accomplished from the launch control center by use of the Platform system ESE, the launch control computer, and the data link.

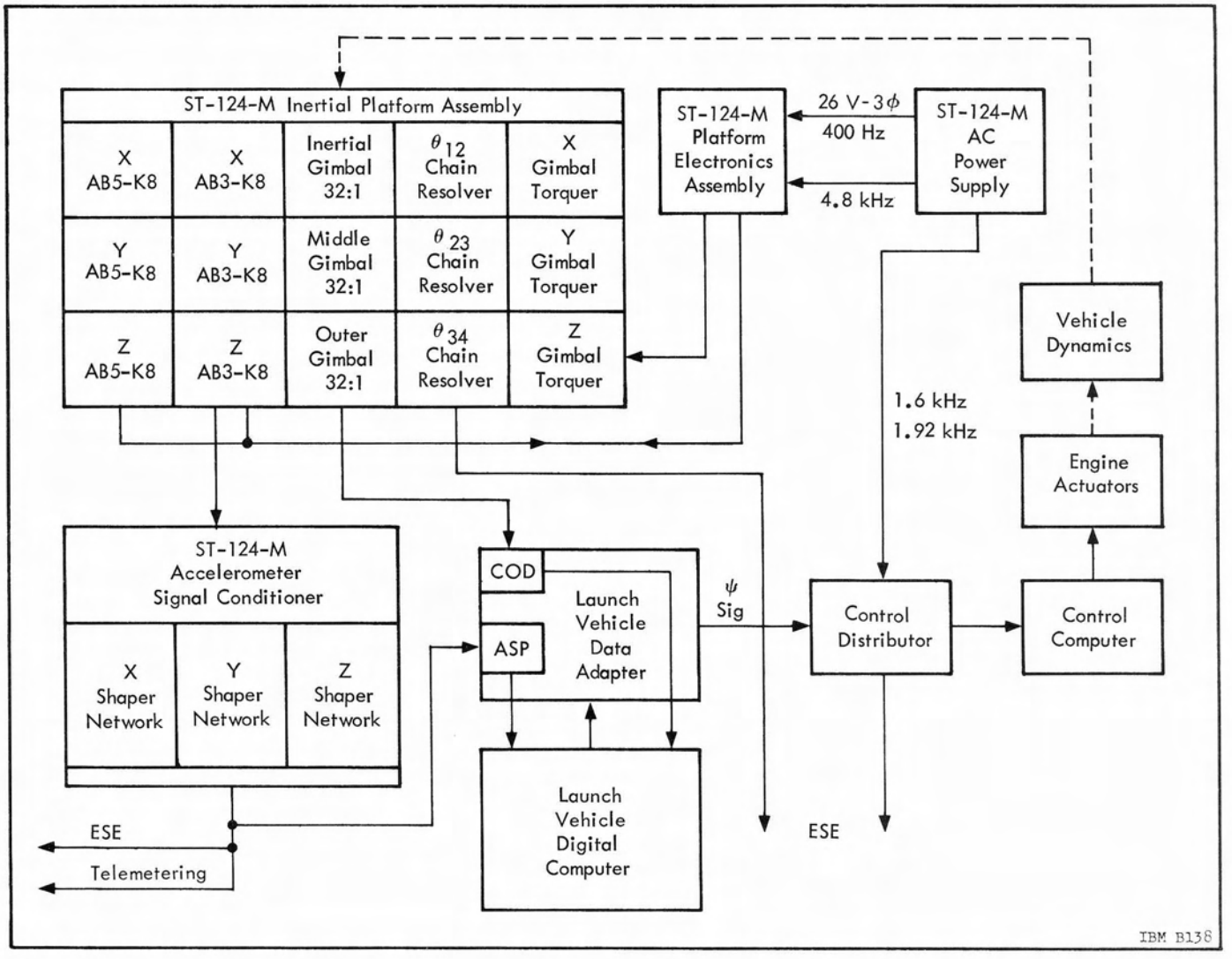


Figure 14.1-3 Platform System Signal Interface

SECTION 14.2

ST-124-M INERTIAL PLATFORM ASSEMBLY

The Inertial Platform Assembly, used in Saturn IB and V Vehicles, can take either of two configurations. These two configurations are designated ST-124-M3 and ST-124-M4 and are three- and four-gimbal systems, respectively. In the basic design of the Inertial Platform, the outer, middle, and inertial gimbals are identical in both models. The ST-124-M4 has a fourth, or redundant, gimbal and a larger base structure; it also requires a different mounting frame. The IU intercabling and wiring for these two systems are identical.

The gimbal configuration of the ST-124-M4 offers unlimited freedom about all three inertial reference axes, while the ST-124-M3 is limited to ± 45 degrees about its X axis (vehicle yaw at launch). For the Apollo mission, the ST-124-M3 configuration is used (Figure 14.2-1).

The inertial, or inner, gimbal provides a rotationally-stabilized table upon which three integrating accelerometers are mounted. The gimbal system allows the inertial gimbal rotational freedom. Three single-degree-of-freedom gyroscopes provide the reference for the stabilized table. The gyros have their input axes aligned along an orthogonal coordinate system x_I, y_I, and z_I of the inertial gimbal as shown in Figure 14.2-2. The signal generator, which is fixed to the output axis of the gyro, generates electrical signals proportional to torque disturbances. These signals are transmitted to the servoelectronics which terminate in the gimbal pivot servotorque motors. The servoloops maintain the inner gimbal rotationally-fixed in inertial space.

The inner gimbal has three pendulous integrating gyro accelerometers oriented along the inertial coordinates x_I, y_I, and z_I (Figure 14.2-3). Each accelerometer measuring head contains a pendulous single-degree-of-freedom gyro; the rotation of the measuring head is a measure of integrated acceleration along the input axis of the accelerometer. The Z accelerometer measures acceleration perpendicular to the thrust vector (crossrange acceleration). The outputs of the X and Y accelerometers are used to compute the pitch angle of the vehicle acceleration vector and the required cutoff velocity.

The coordinate erection and orientation system of the Inertial Platform aligns the y_I coordinate along the launch local vertical parallel to the gravity vector and aligns the z_I coordinate perpendicular to the desired flight plane. The coordinate orientation is accomplished by use of an automatic alignment system which is a part of the ESE on the ground. The leveling alignment servoloops (X and Z) generate torquing voltages which are a function of the earth's angular velocity, the latitude of the launch site, and the azimuth of the x_I coordinate (launch azimuth). These voltages are applied to the X and Z gyro torquers and cause the gyros to torque its respective gimbal until the servos are nulled. Inertial Platform coordinates are established in azimuth with the roll alignment servoloop. The output of the roll alignment servoloop is a function of the earth's angular velocity and the latitude of the launch site. Azimuth alignment being a commanded function, is accomplished by injecting azimuth alignment signals directly into the roll alignment loop and torquing the roll gimbal with the Y gyro. The azimuth alignment position can be updated at any time by the launch control computer.

The reference coordinate frame of the Inertial Platform maintains a fixed relationship to the inner gimbal. This coordinate frame is accurately positioned prior to vehicle lift-off and remains space-direction fixed after vehicle lift-off. The gimbals of the Inertial Platform allow the inner gimbal rotational freedom with respect to the vehicle. The gimbal pivots are the axes about which the gimbals turn with respect to each other. The ± Z pivots couple the inner (stabilized) gimbal to the middle gimbal; the Z pivot axis is normally along the vehicle pitch axis. The ± X pivots couple the middle gimbal to the outer gimbal; the X pivot axis is normally along the vehicle yaw axis. The ± Y pivots couple the outer gimbal to the platform

mounting base; the Y pivot axis is along the vehicle roll axis. The Inertial Platform pivot scheme is shown in Figure 14.2-4. The X, Y, and Z pivots are controlled by dc torque motors; the Y pivot torquer has approximately twice the torque capacity of the other pivot torquers. This accommodates the reflected torque when the middle gimbal is not orthogonal with the outer gimbal. For transfer of electrical signals across the ± Y and ± Z pivots, slip-ring capsules are used. A flex cable is used on the ± X pivot because of its limited freedom.

Dual-speed resolvers (32:1) are used as shaft angle encoders on the +X, +Y, and +Z pivots. The output of these resolvers is converted into a digital code in the LVDA. The system also has an analog resolver chain which utilizes single-speed resolvers on each pivot and three program resolvers in the

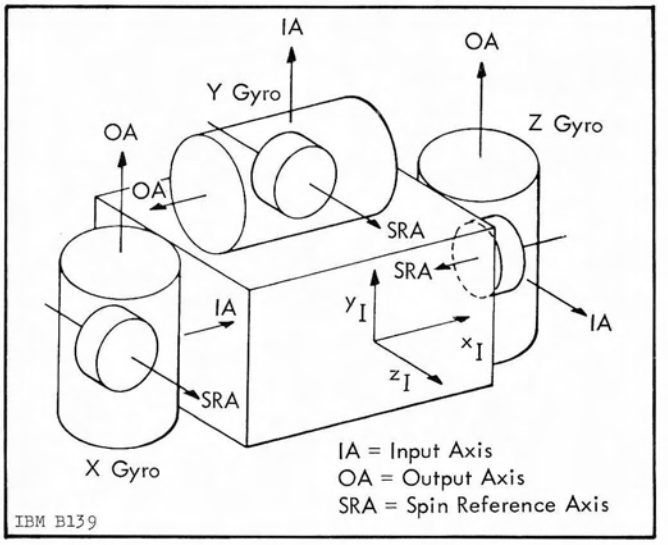


Figure 14.2-2 Orientation of Gyro Axes

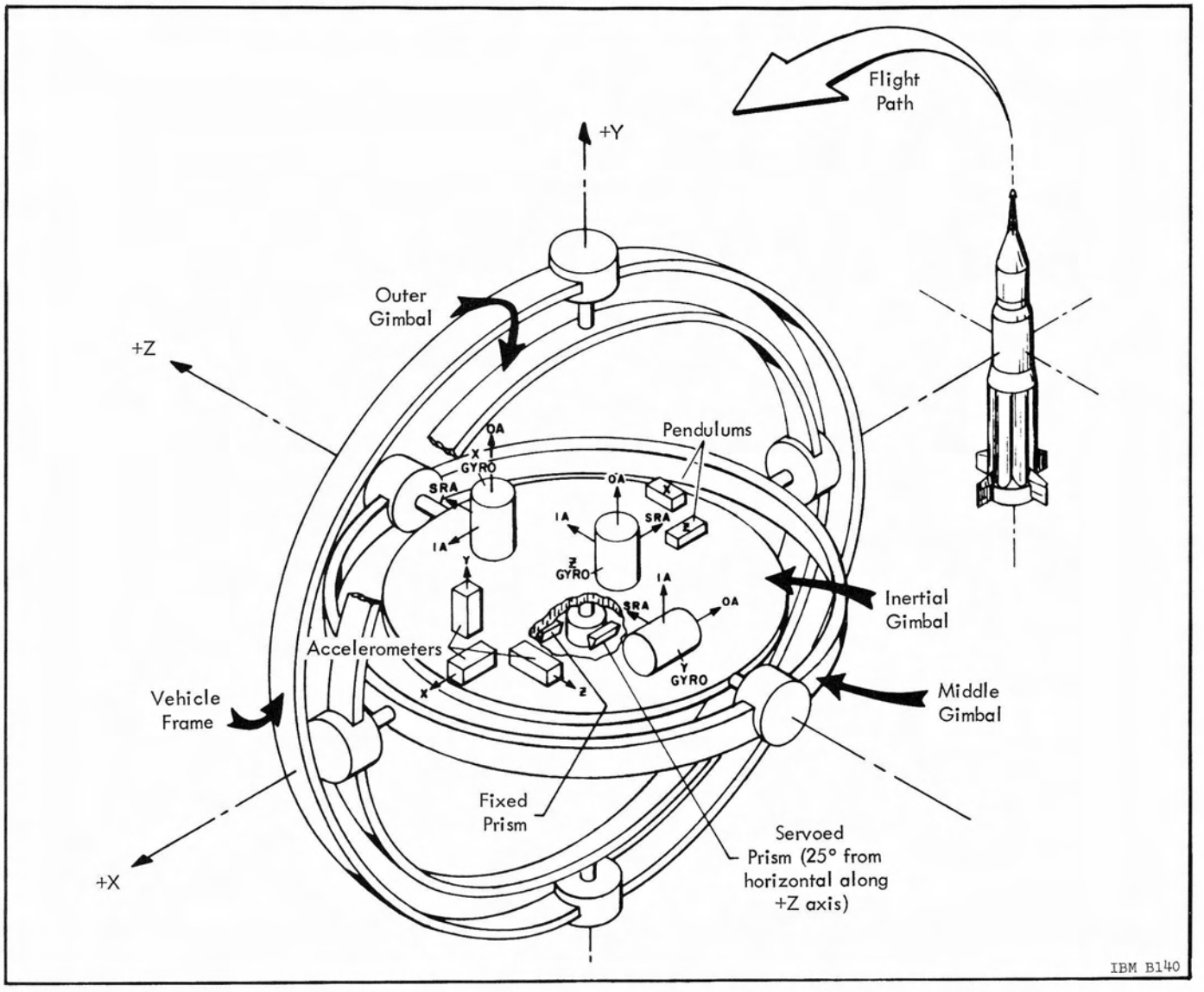


Figure 14.2-1 ST-124-M Gimbal Configuration

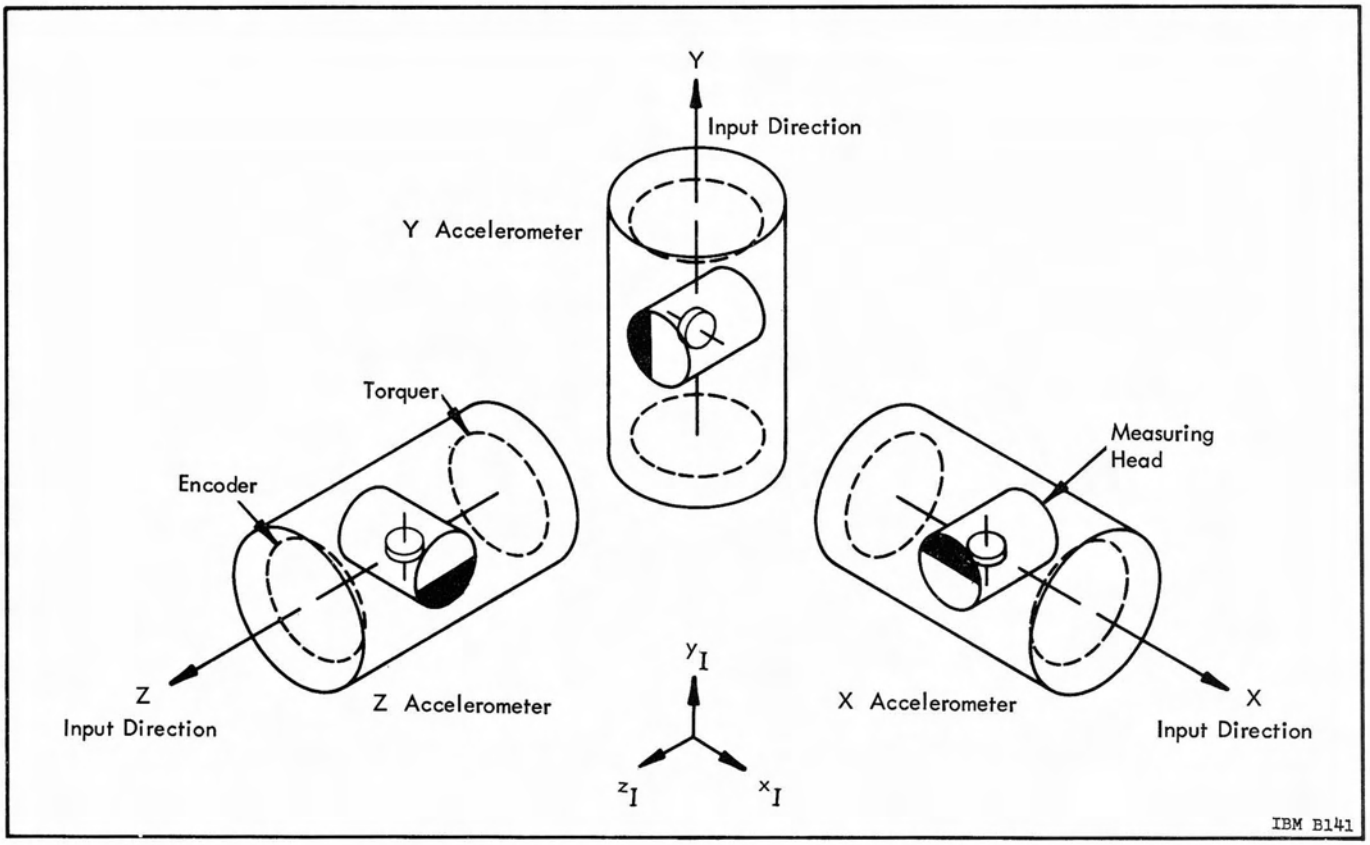


Figure 14.2-3 Orientation of Accelerometer Axes

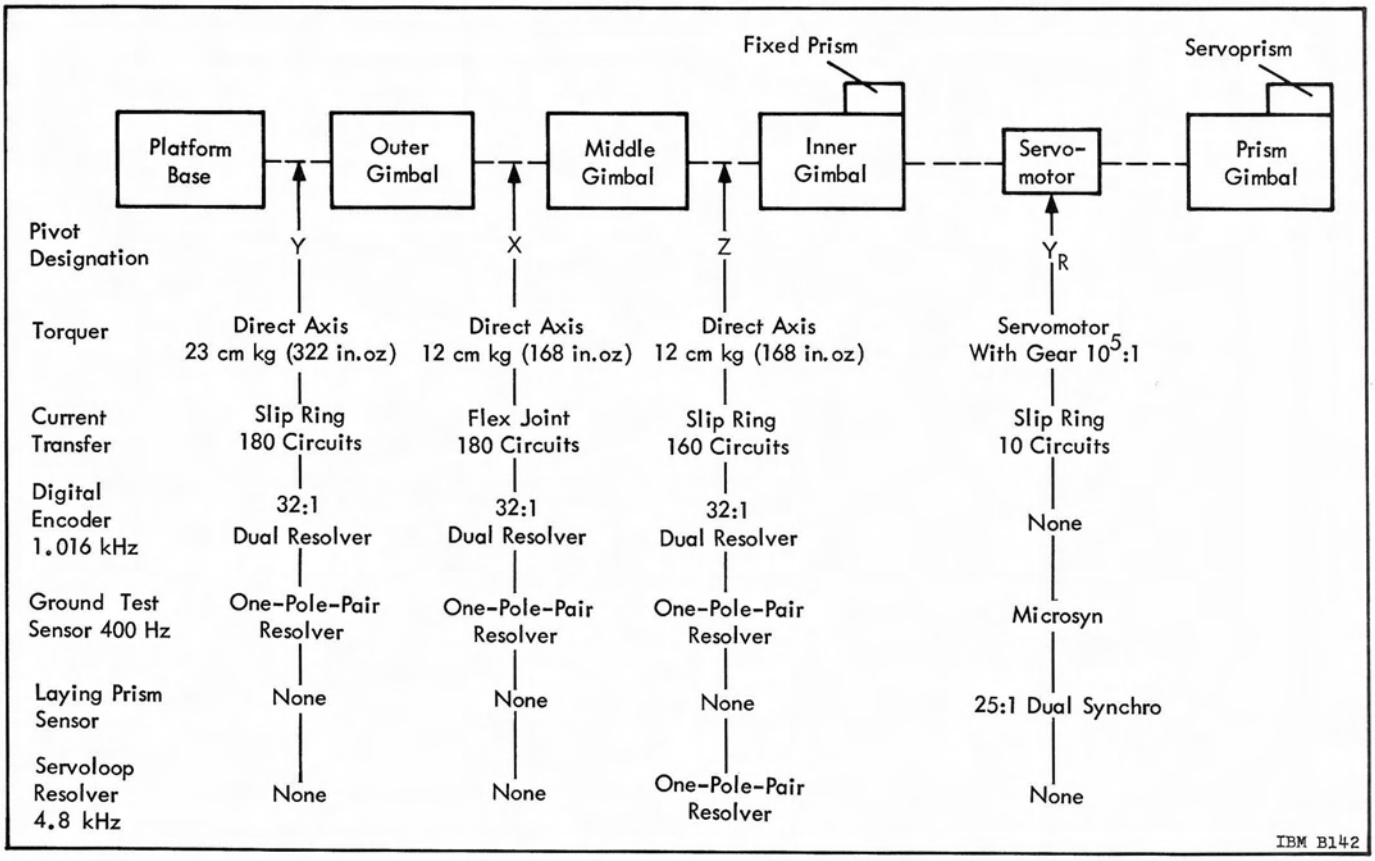


Figure 14.2-4 Platform Gimbal Pivot Scheme

inertial data box. This is used with the ground electrical support equipment only to facilitate checkout and test. If required, the resolver chain system can be used as flight equipment to measure the gimbal angles and to provide the vehicle attitude signals.

The + Z and +Y pivots each contain a 100-circuit slip-ring cartridge for passing electrical signals across the pivots. The -Z and -Y pivots each contain an 80-circuit slip-ring cartridge. All critical signals are routed through the plus pivots while all power transmission is over the minus pivots. The slip rings are built up by electrodeposition of 0.015 inch of copper base with a flashing of nickel to prevent gold migration and electrodeposition of 0.015 inch of gold on the outside. The rings are dielectrically isolated and supported with a filled epoxy. A one-piece stainless steel cross-spline along the center serves as the main structural member of the ring subassembly (Figure 14.2-5). The leadwire is fastened to the ring by electrodeposition and is routed along the spline to the mounting flange.

A 90-degree V-groove is machined into the rings to serve as a guide for the brushes. Dimensional tolerance on the ring assembly is controlled by a grinding process where the V-groove in all rings are ground in a single operation. A set of miniature precision bearings and the brush blocks' mounting frame complete the ring assembly.

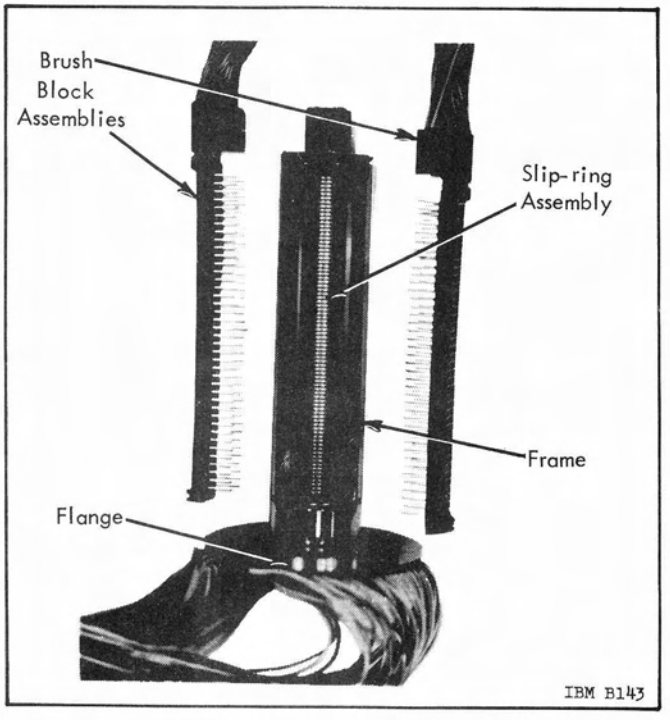


Figure 14.2-5 Slip-ring Capsule

The two brush block subassemblies allow complete redundancy for each brush. The brushes are preformed and prestressed Ney-ORO-28A (75% gold, 22% silver, and 3% nickel) material. The brush blocks are a filled epoxy structure aligned with dowel pins and secured with screws to the frame. The leadwire is an unpigmented teflon-insulated nickel-plated copper, 19/42, size 30 AWG, stranded wire.

Acceptance testing of each unit includes 100-hour run-in time, temperature cycling, noise tests, and an X-ray of the completed assembly.

Table 14.2-1 lists the slip-ring cartridge characteristics:

The Y_R prism gimbal pivot is controlled through a gear reduction of 10^5:1 by a servomotor mounted to the inertial gimbal. The angle between the prism gimbal and the inertial gimbal is accurately sensed by a dual synchro (25:1) and controlled with a followup servo. A microsyn is also mounted on the Y_R pivot for initial alignment of the prism gimbal to the inertial gimbal and to facilitate laboratory checkout and test.

Table 14.2-1 Slip-ring Cartridge Characteristics

Current Rating		1 A at 125 V, 400 Hz continuous per circuit
Noise Limit		10 uV/mA
Contact Resistance		0.125 ohm per circuit
Breakaway Friction		2 g cm/circuit
Environmental		
	Temperature	-55°C to +100°C (67°F to +212°F) storage 0°C to +60°C (32°F to +140°F) operation
	Vibration	15 g, 20-2000 Hz 3-hour test time per axis
	Shock	30 g, 3 milliseconds 20 g, 11 milliseconds
	Acceleration	20 g
Life		
	Useful Life	8760 hours (storage and operating)
	Operating Life	1000 hours will meet noise specification 5000 hours with maximum of 100% increase in noise specification

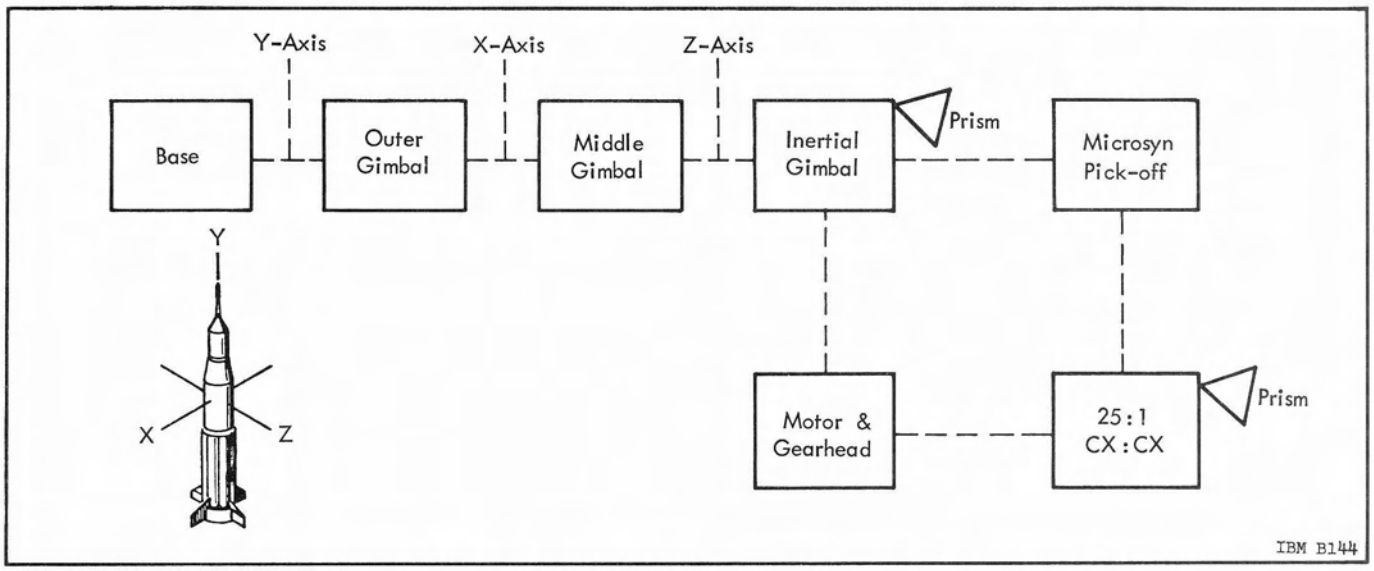


Figure 14.2-6 Platform Gimbal Arrangement

The three-gimbal ST-124-M3 Inertial Platform Assembly, as described, is the normal launch pad configuration and is illustrated in Figure 14.2-6.

The weight of the ST-124-M3 Inertial Platform Assembly is 48 kilograms (107 pounds). The platform is mounted in the Saturn IB and V IU at control position IV on accurately machined surfaces which are qualified to the IU coordinates to ± 3 arc minutes. A window in the IU at control position IV provides a line-of-sight to the platform azimuth laying prisms for penetration of the azimuth laying theodolite light source (Figure 14.2-7).

The electrical connectors and hemispherical covers of the Inertial Platform are sealed so that ex-

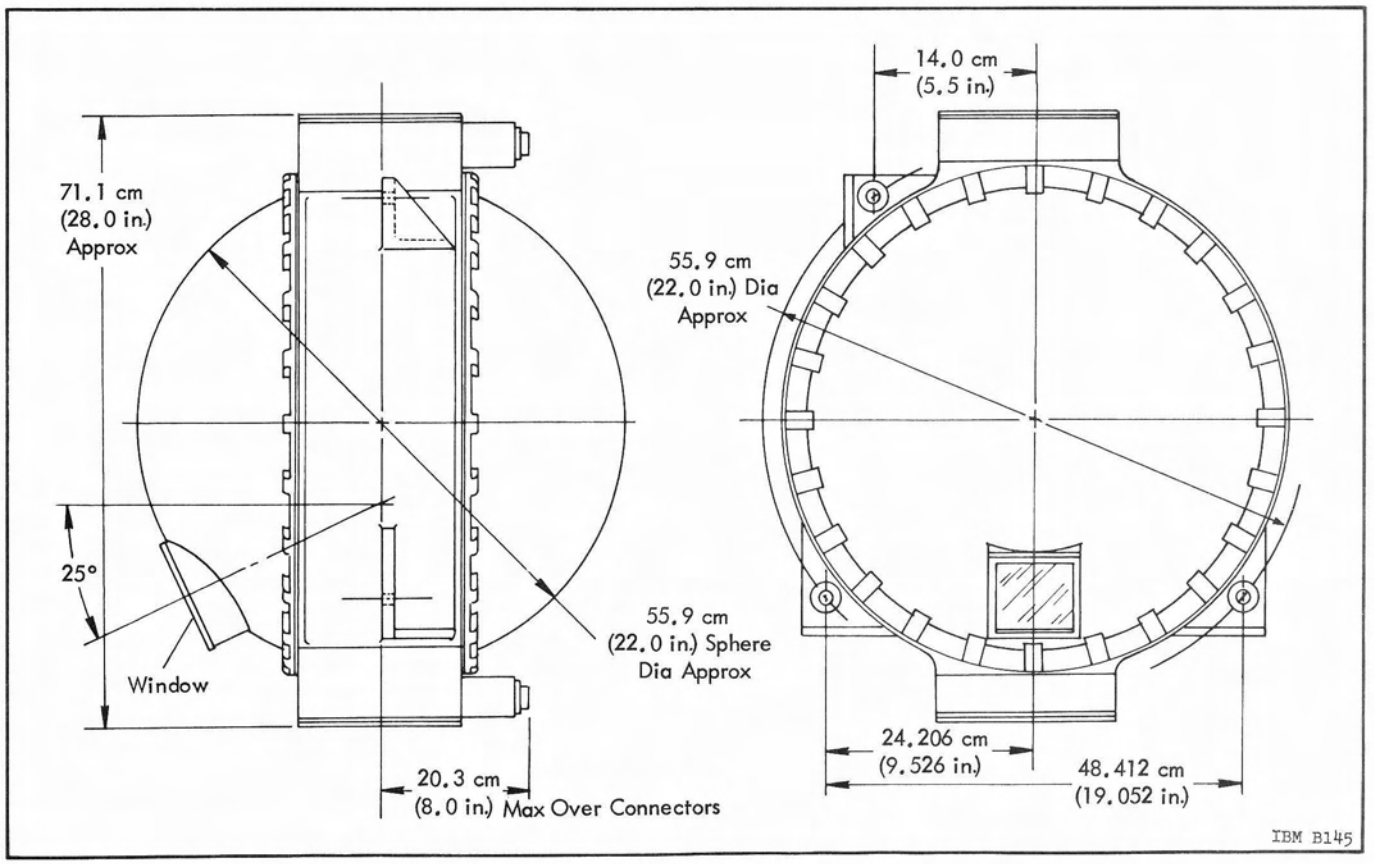


Figure 14.2-7 ST-124-M Inertial Platform Assembly

haust gas from the gas bearing components must pass through a special orifice in its base. This orifice is a pressure-regulating device which stabilizes the internal ambient pressure at 8.3 N/cm^2a (12 psia). Because of the characteristics of this orifice, the internal pressure will rise to approximately 11.75 N/cm^2a (17 psia) in a one atmosphere ambient and will drop to the controlled pressure of 8.3 N/cm^2a (12 psia) as the vehicle ascends in approximately one minute after lift-off.

The covers also serve as heat exchangers for removing excess heat from the Platform. The water-methanol coolant from the environmental conditioning system flows through passages in the covers removing the excess heat. The water-methanol solution is maintained at 15 ± 1°C (59 ± 1.8°F) by the IU environmental conditioning system. The mass temperature of the platform stabilizes at approximately 42°C (107.6°F). The hemispherical covers are fabricated of aluminum and are secured to the platform base with cap screws and sealed with full volume "0" rings.

The platform gimbals, pivot housings, and the base are machined from beryllium which provides the greatest stiffness-to-weight ratio, stability after machining, and excellent heat transfer characteristics.

The inner gimbal is geometrically the most complicated gimbal and the most difficult to fabricate (Figure 14.2-8). This gimbal supports the three stabilizing gyros, three accelerometers, two pendulums, the inertial prism, the synchro prism assembly, and electronic modules. The mounting surfaces for the gyros, accelerometers, pendulums, and prisms are precision-machined surfaces. Orthogonality of the accelerometers' mounting surfaces is ± 3 arc seconds; the gyros' is ± 2 arc minutes. The pendulums are matched to the accelerometers to ± 3 arc seconds, and the prisms are matched to the inertial coordinates to ± 3 arc seconds. Gas supply passages are machined inside the inertial gimbal, and special fittings on the gas bearing components allow them to be plugged directly into the gas supply passages.

The gimbal rings are designed as spherical sections. This geometry was chosen to give maximum mechanical rigidity and stability and to provide symmetrical moments of inertia for servoloop design.

Gimbal load bearings are designed so that minimum sheer is placed on the gimbal. This is accomplished by using a pair of bearings on one pivot of each gimbal which is preloaded against each other with a 36.3 kilograms (80 pounds) load. The other pivot of each gimbal has a single gothic arch type bearing loaded with a 2.27 kilograms (5 pounds) preload.

Gimbal pivot resolvers are assembled in separate beryllium housings and attached to the pivots with stiff diaphragms. This allows a minimum eccentricity between resolver rotor and stator, bench testing of the assembled resolver, and easy replacement without disassembly of the gimbal structure at the load bearings.

Nitrogen gas is transported across the pivots through an annulus with "0" ring seals. The total leak rate of the pivot annulus will be less than 1400 cm^3/min STP (0.05 cfm).

Structural resonance of the outer and middle gimbals is 265 hertz and 330 hertz, respectively. The structural resonant frequency of 120 hertz is obtained on the inner gimbal because of the stiffness of the beryllium gimbal rings. There is a secondary resonant frequency of the inertial gimbal at 280 hertz which is obtained from the bearings and pivot trunnions. Above 280 hertz, the gimbals attenuate base vibration inputs providing a smooth support for the components.

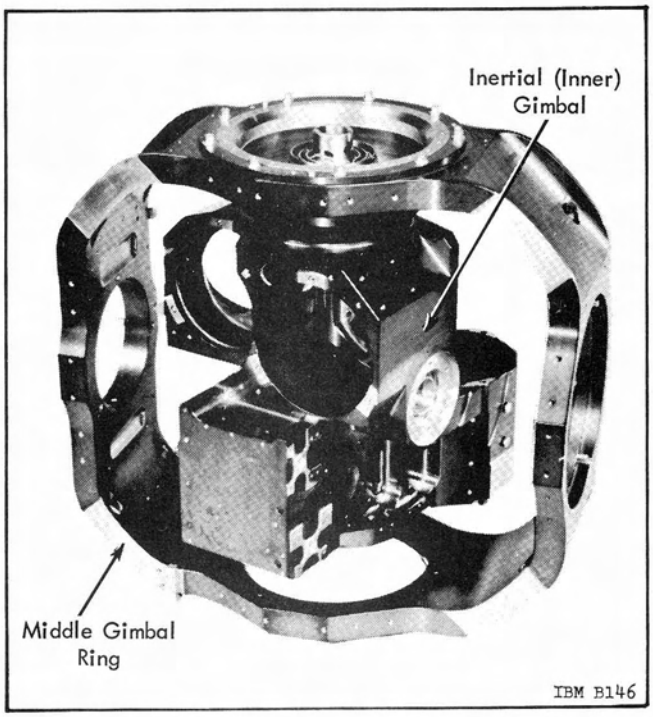


Figure 14.2-8 Gimbal Design

SECTION 14.3

GYRO AND ACCELEROMETER SERVOSYSTEM

The block diagrams of the gyro and accelerometer servoloops are shown in Figures 14. 3-1 and 14. 3-2, respectively. The servoloops use a 4. 8-kilohertz suppressed carrier modulation system with the signal generator outputs being amplified and demodulated on the gimbals of the Inertial Platform. The dc signal from the detector output is transferred from the Platform to the Platform Electronic Assembly. The dc signal is shaped by a lag-lead stabilization network, remodulated at 4. 8 kilohertz, amplified, and then demodulated prior to entering the dc power bridge. This dc power bridge provides a current source drive for the direct axis dc gimbal torquer. The 4. 8-kilohertz carrier provides sufficient bandwidth for the servoloop while the current driver for the torquer maintains the gain in the servoloop independent of torquer heating and commutator brush resistance.

The Z servoloop has the Z gyro output signal phase-shaped and amplified and sent to the Z pivot torquer. The X and Y gyro output signals are resolved along the X and Y coordinates of the middle gimbal by a resolver mounted along the -Z pivot. The outputs of the resolver are amplified and demodulated. The resolved signals are shaped and amplified and fed to their corresponding gimbal pivot dc torquer. No gain compensation such as secant θ_X is used in the outer gimbal servoloop for middle gimbal angle deviation. Figure 14. 3-3 shows the hardware which comprises a gimbal servoloop.

A block diagram of the gyro servoloop and accelerometer servoloop is shown in Figures 14. 3-4 and 14. 3-5, respectively.

The principle function of the servosystem is to maintain α near 0 in the presence of various disturbances (see Figure 14. 3-6). A logical measure of system performance is the ratio $\frac{T_\alpha}{\alpha}$ which describes the maximum angular deviation for specified inputs (T_α = torque about IA). For instrumentation reasons, $\frac{T_\alpha}{\beta}$ is used because α is very small for frequencies below ten times the resonant frequency. The angular motion β resulting from α is normally a much larger signal by the multiplication factor $\frac{H}{J_\beta s}$ (the gyro transfer function) and is easily measured at the input to the servoamplifier, F(s). In system design, the ratio $\frac{T_\alpha}{\beta}$ is made as large as possible, consistent with good transient response.

The single-axis approach to the design of the servosystem is expedient, but it ignores the effect of mechanical and electromechanical interaxis coupling. Mechanical interaxis coupling will occur if the principal axes of the inertial gimbal do not coincide with the input axes of the gyroscopes. Also, products of angular motion will occur if the moments of inertial are unequal. Fortunately, in the design and fabrication of the inertial gimbal, close tolerance controls make these effects negligible relative to other interaxis coupling.

The output signal (β) of the single-axis gyro is a measure of the angle between the gyro float and the gyro case. This is the signal used in the platform servoloop. Because the gyro case is mounted to the inertial gimbal, disturbances about its output axis are reflected into other servoloops. Therefore, motions of the gyro case about its output axis are coupled into the servoloop for that gyro.

The effect on servostability of this pickoff coupling depends on the orientation of the gyros on the Inertial Platform. A multiplicity of possible gyro orientations exists for an Inertial Platform but it is not possible to orient three single-axis gyros with mutually orthogonal input axes in such a way that there is not at least one closed loop of gyro pickoff

interaxis coupling. Additional considerations for orientation of the gyros on the inertial gimbal must be made. These include the coning or rectification drift and the unequal elasticity (anisoelasticity) in the gyro spin axis and input axis which give rise to a steady state drift rate. The effect of gyro orientation is a function of the direction of applied linear acceleration or vibration and varies sinusoidally as the acceleration vector is rotated about the gyro's output axis.

Figure 14. 3-6 is a sketch of the Inertial Platform gyro orientation. The inertial gimbal is gimbal-mounted for 3 degrees of freedom relative to the vehicle about the three mutually-perpendicular axes

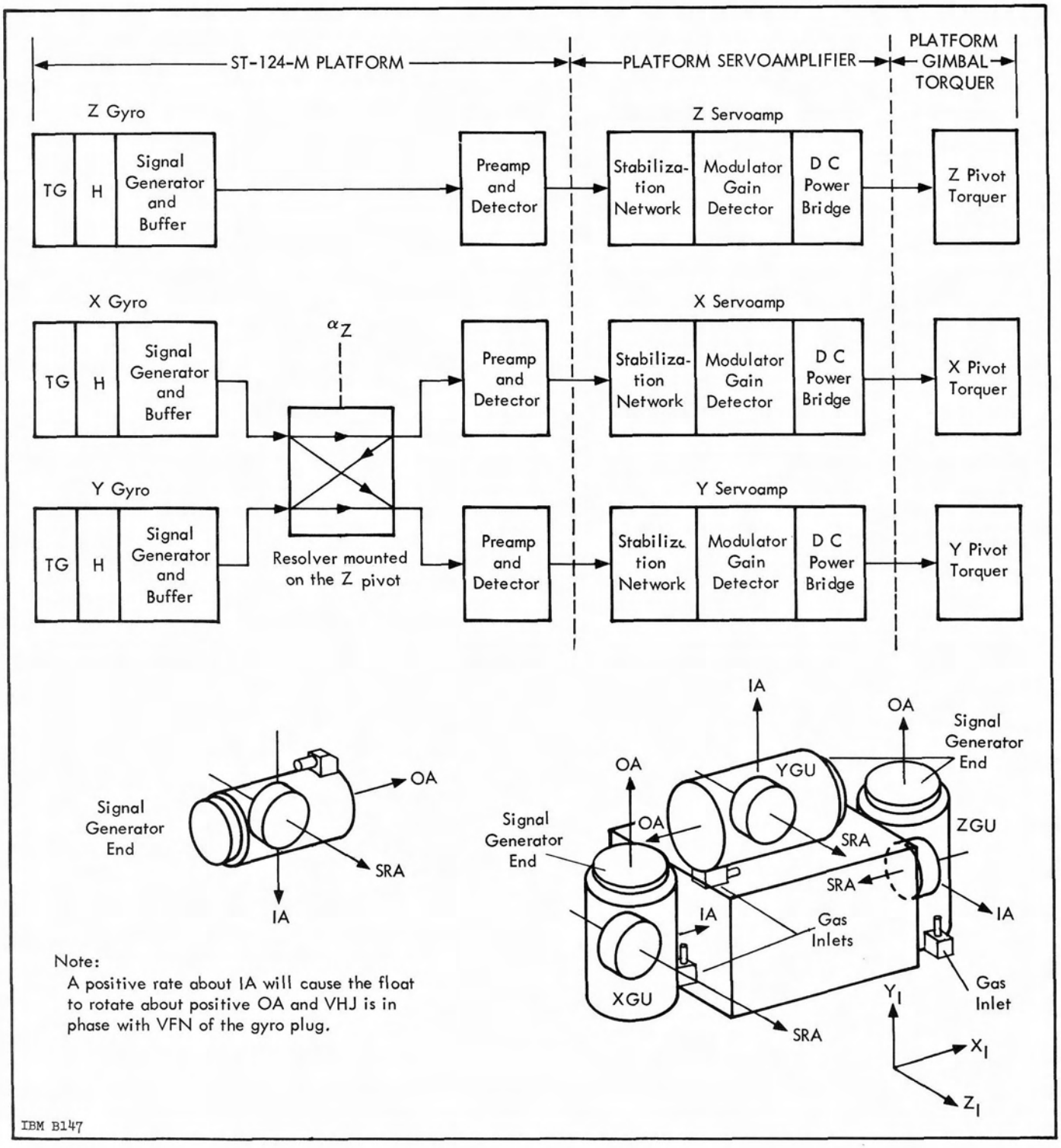


Figure 14. 3-1 Gyro Servoloops Block Diagram

identified as α_x, α_y, and α_z. Each gyroscope is represented by mutually-perpendicular vectors which define the angular momentum (H), the input angular motion (α), and the output motion (β). The gyroscopes are identified with their particular platform axes. Platform angular motion about the input axis of the Y gyro is coupled into the pickoff of the X and Z gyros, and angular motion about the input axis of the X gyro is coupled into the pickoff of the Y gyro.

The actual pickoff signals which are fed to the amplifier can be expressed as (Figure 14.3-6):

$$\sigma_x = \beta_x + \alpha_y$$

$$\sigma_y = \beta_y - \alpha_x$$

$$\sigma_z = \beta_z + \alpha_y$$

The 3-axis servosystem block diagram shown in Figure 14.3-7 illustrates this coupling through the gyro output axes. The motion about the Y axis is coupled into the Z axis servo but does not feed back into either of the other two gyro servoloops. Therefore, the Z axis servo will be disturbed by motion of the Y axis but no stability problem results. There is coupling of the input angles α_x and α_y to the output motions β_y and β_x, respectively. Therefore, a closed loop is formed which, in addition to causing cross axis disturbances, must also be considered as to its effect on servo performance. A resolver (α_z) provides continuous coupling between the inertial components and the gimbal about which compensating servotorques are applied. This effect is shown by the sinusoidal coupling between the X and Y axes.

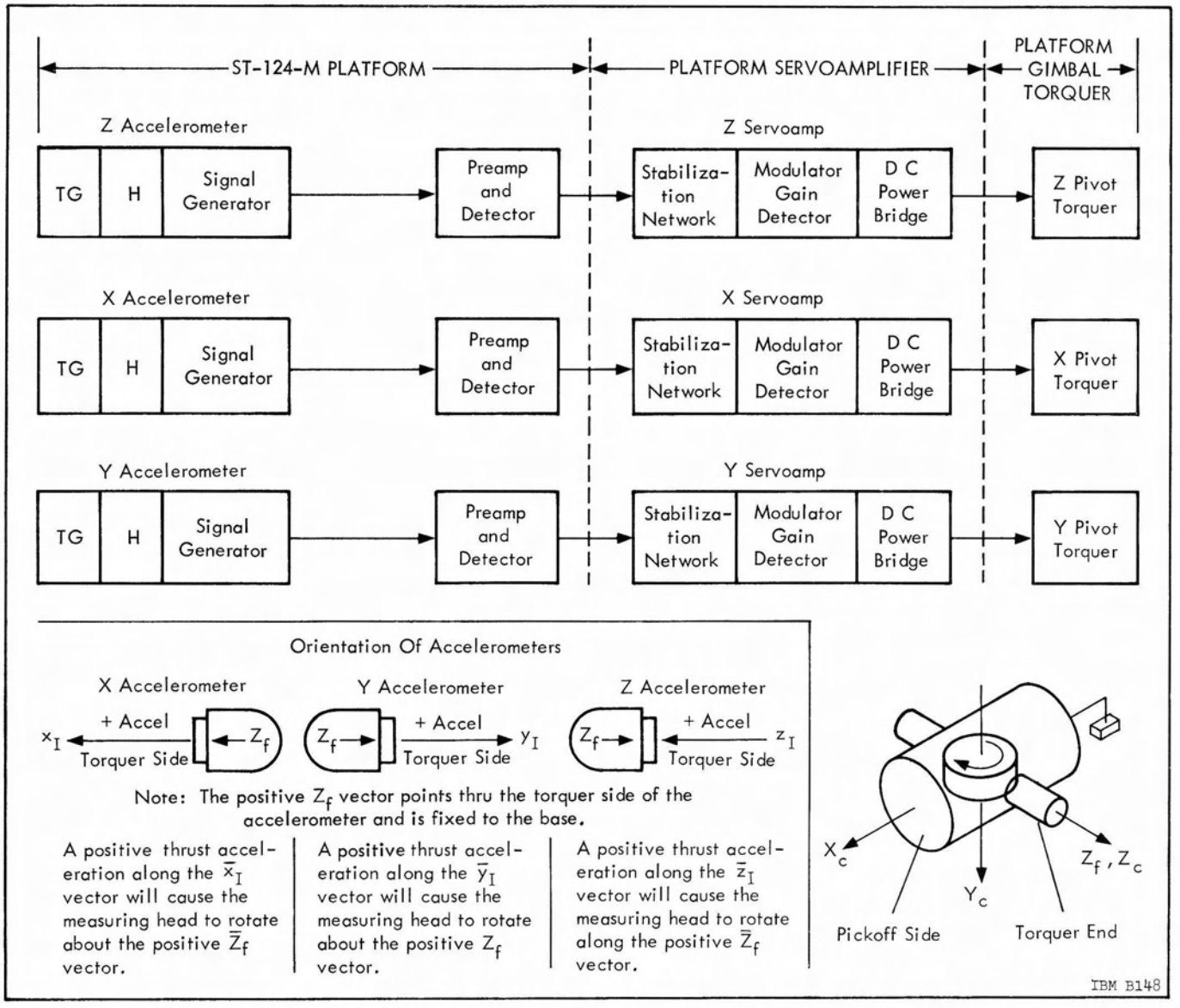


Figure 14.3-2 Accelerometer Servoloops

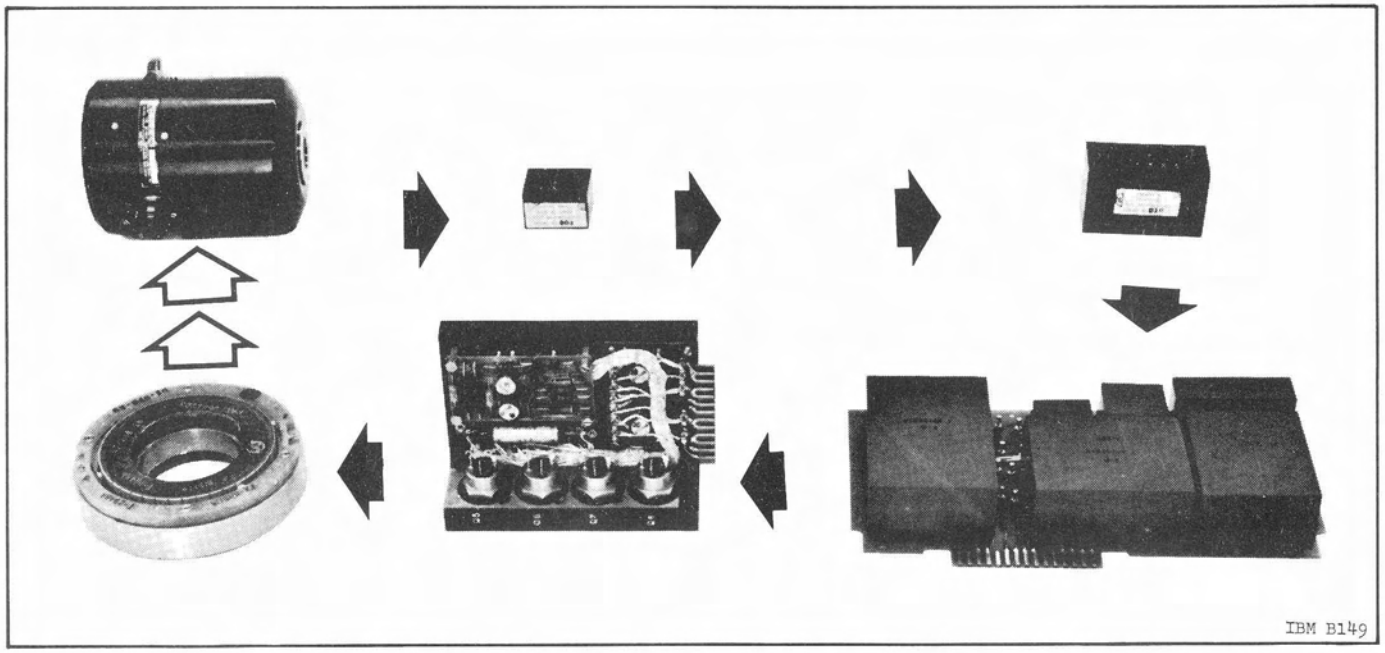


Figure 14. 3-3 Gimbal Servoloop Hardware

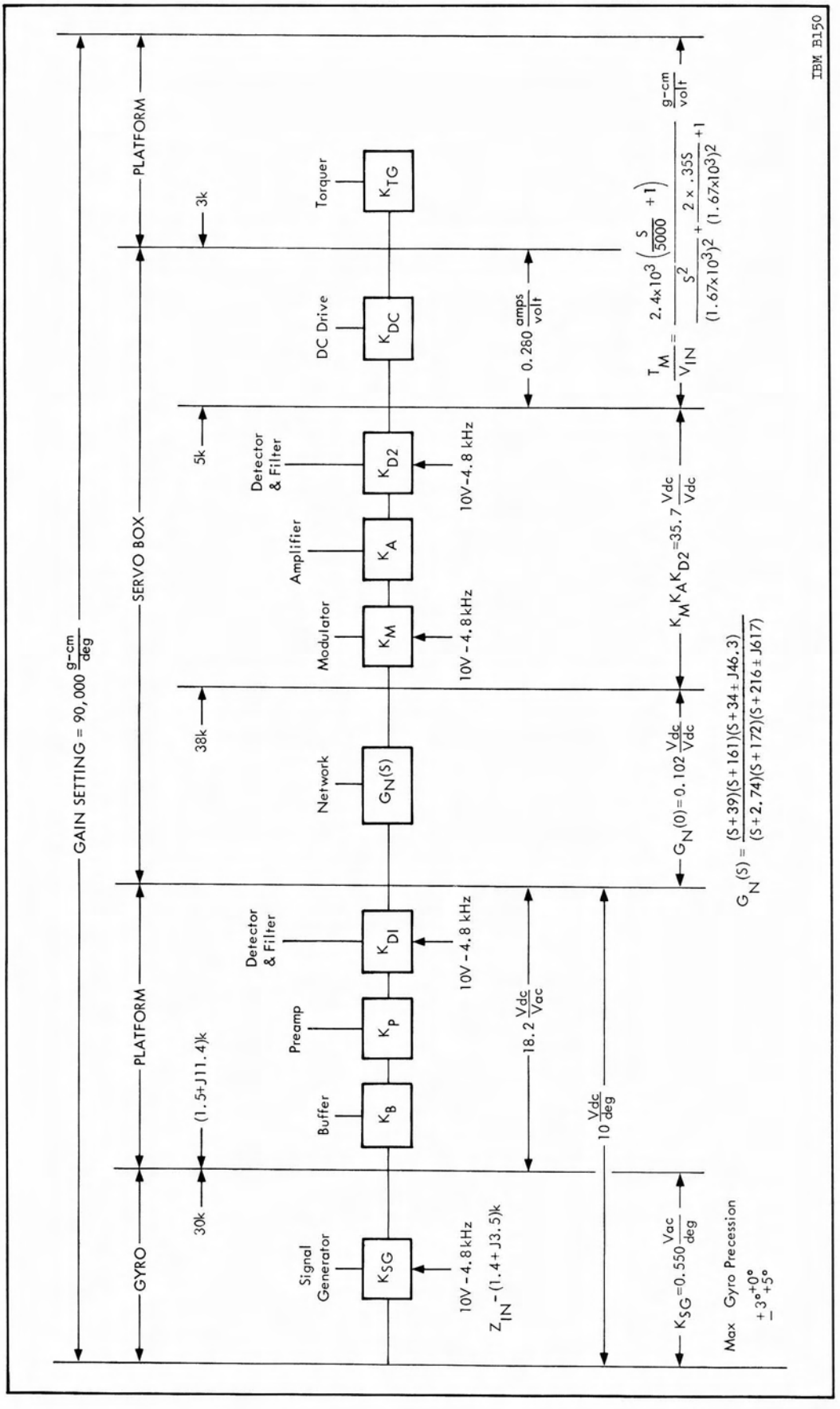


Figure 14.3-4 Gimbal Electronics Block Diagram

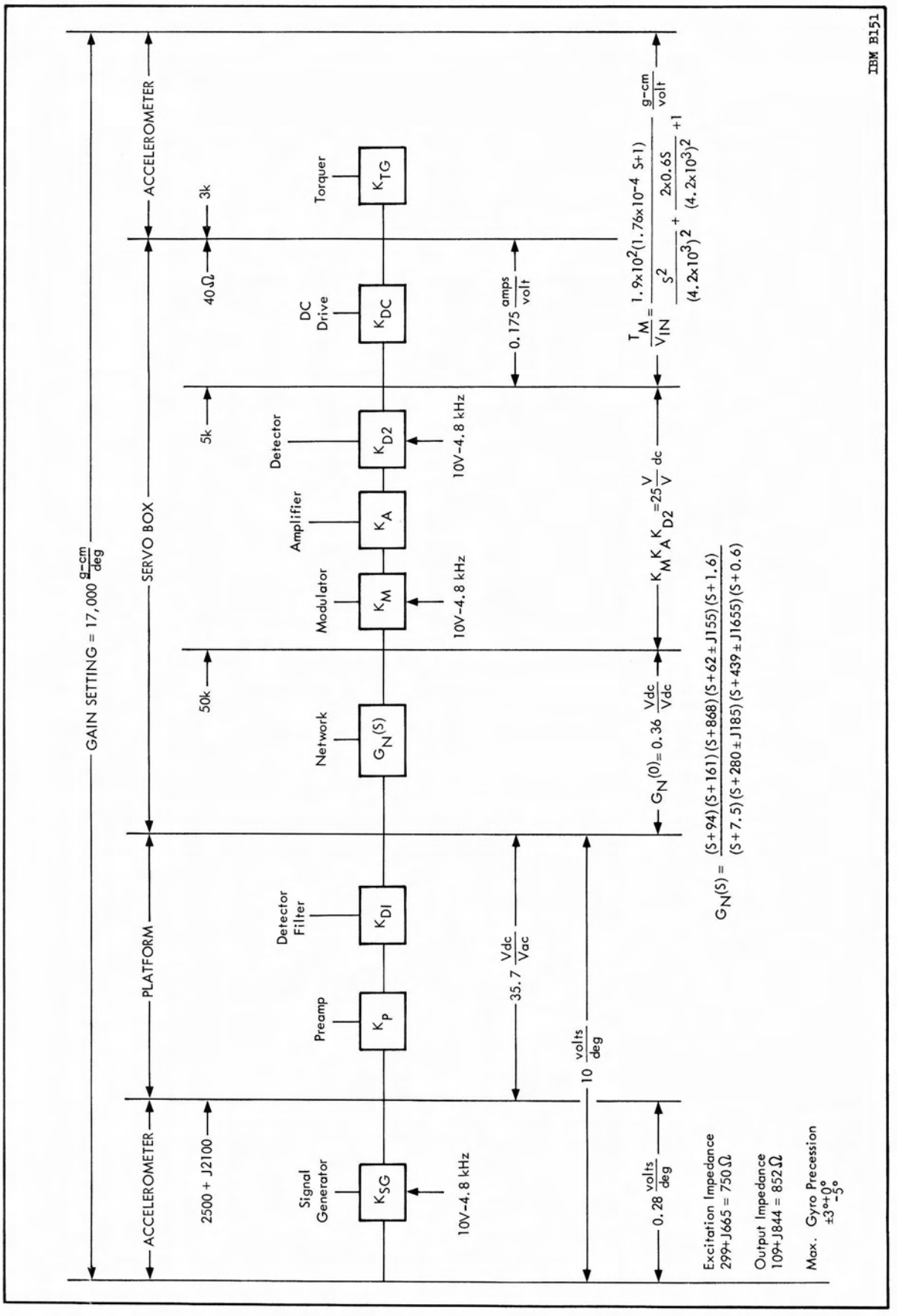


Figure 14.3-5 Accelerometer Electronics Block Diagram

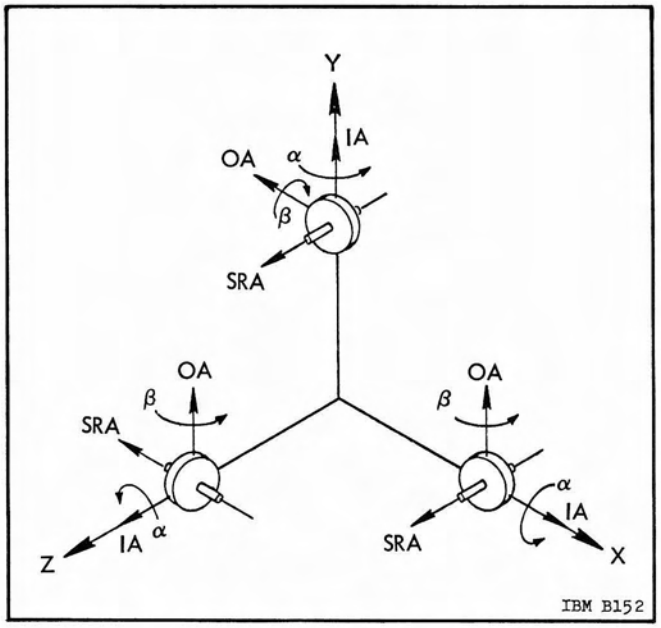


Figure 14.3-6 ST-124-M Gyro Orientation

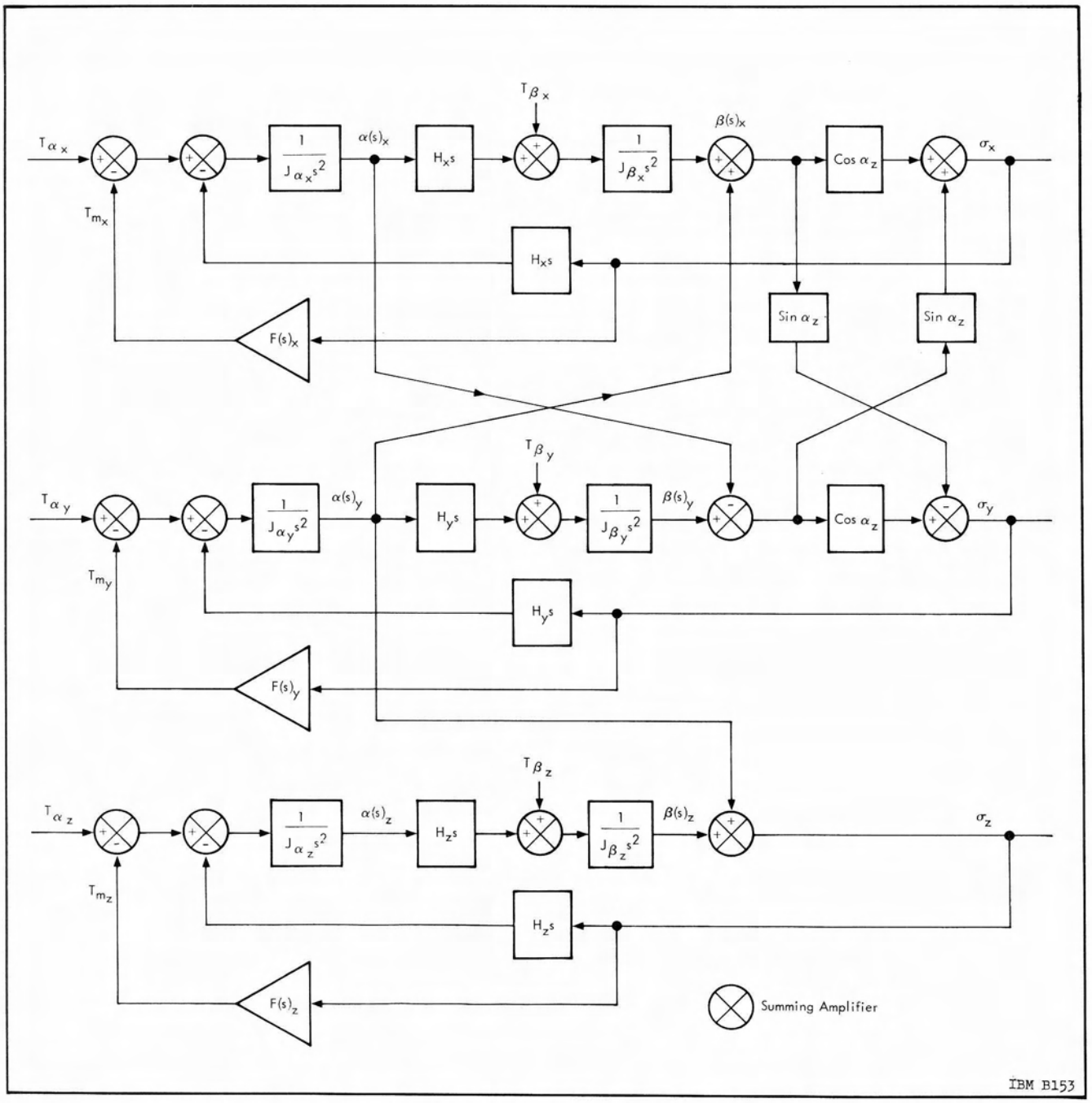


Figure 14.3-7 Three-axis Inertial Platform Assembly Block Diagram

SECTION 14.4

GIMBAL ANGLE MULTISPEED RESOLVERS

As shown in Figure 14.4-1, the +X, +Y, and +Z gimbal pivots have multispeed analogue resolvers for angular readouts. The phase shift of their output voltage is measured by digital techniques. A schematic block diagram is shown in Figure 14.4-2.

The dual resolver provides the demanded high-readout accuracy. The digital computer system processes the measured gimbal attitude signals and computes the pitch, roll, and yaw vehicle body rates for the attitude control system.

The dual resolver has both a 32-speed and a single-speed winding on the same magnetic structure. The 32-speed winding has 32 electrical rotations for one mechanical shaft rotation. The reference or the resolver excitation (V_1) is 26 volts, 1016 hertz. The output winding drives an RC bridge network as shown in Figure 14.4-2.

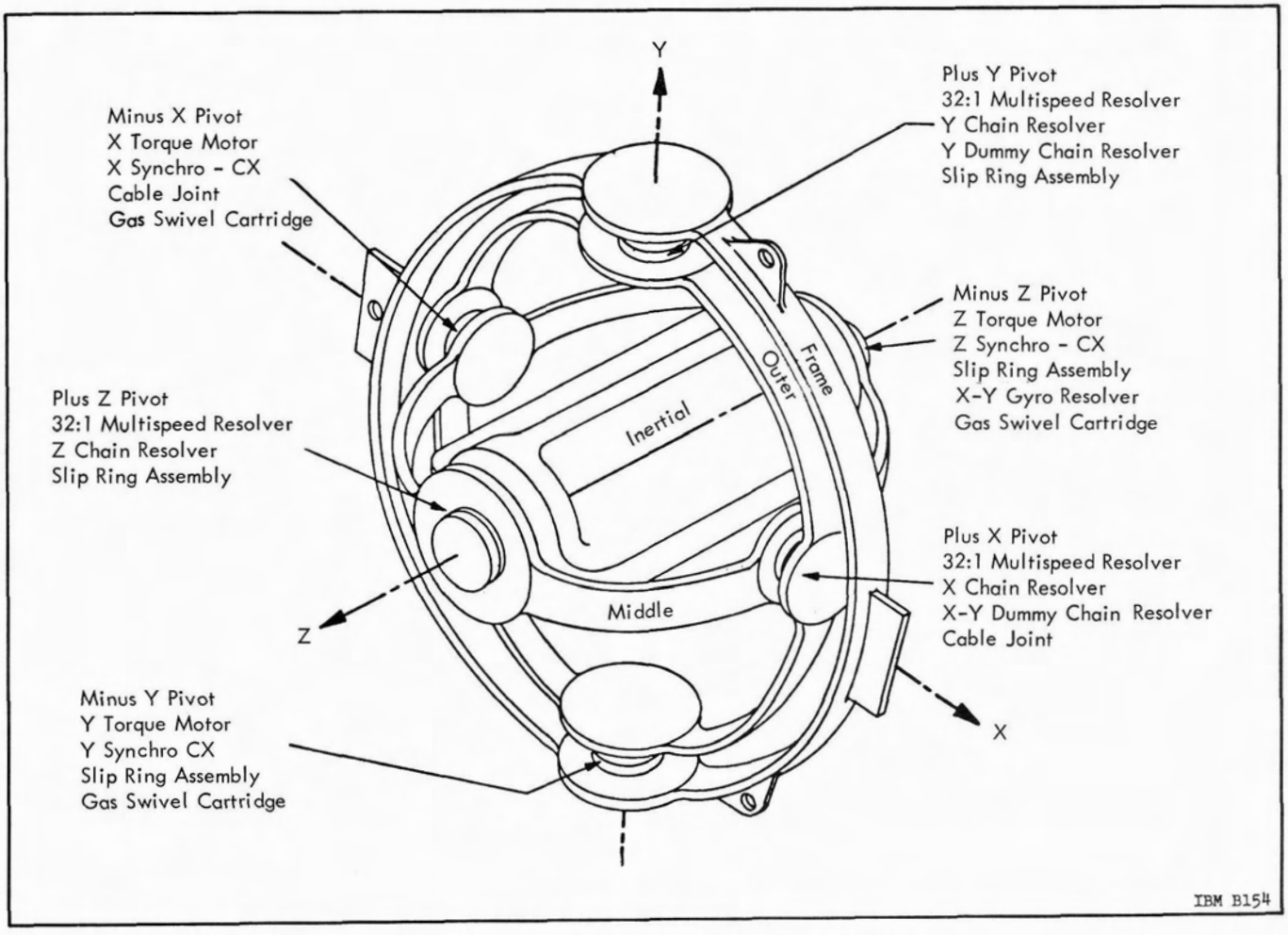


Figure 14.4-1 Three-gimbal Configuration

The voltage V_2 at the input to the start pulse generator can be expressed as

$$V_2 = \frac{E}{\sqrt{2}} e^{j(32\theta - \pi/4)}$$

and the voltage V_3 at the input to the stop pulse generator can be expressed as

$$V_3 = \frac{E}{\sqrt{2}} e^{-j(32\theta - \pi/4)}$$

where E is the open circuit resolver voltage and θ is the rotation or mechanical angle in radians.

From the ratio of $\frac{V_2}{V_3} = e^{j(64\theta - \pi/2)}$, it is seen that the phase shift of V_2, with respect to V_3, is 64 times the angle θ or a multiplication by a factor of 2 occurs in the bridge network.

As the instantaneous voltage V_2 passes through zero with a positive slope, a start pulse is generated which opens a gate and a counter counts a 2.048 megahertz clock frequency. As V_3 passes through zero with a positive slope, a stop pulse is generated which closes the gate and stops the counter. The number of cycles counted is a measure of the gimbal angle (Refer to the vector diagram in Figure 14.4-3).

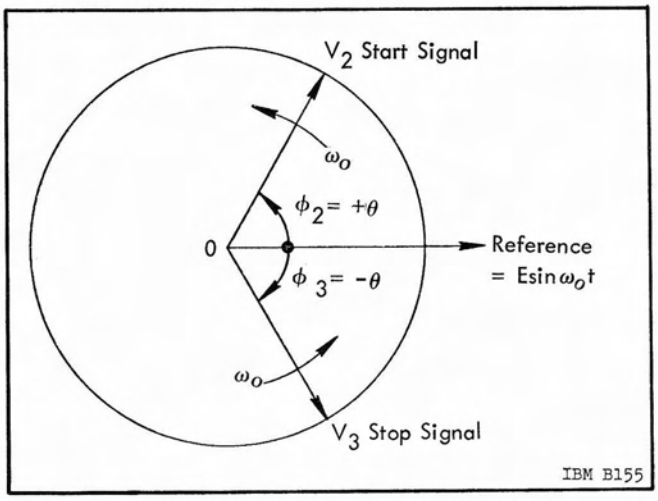


Figure 14.4-3 Gimbal Angle Vector Diagrams

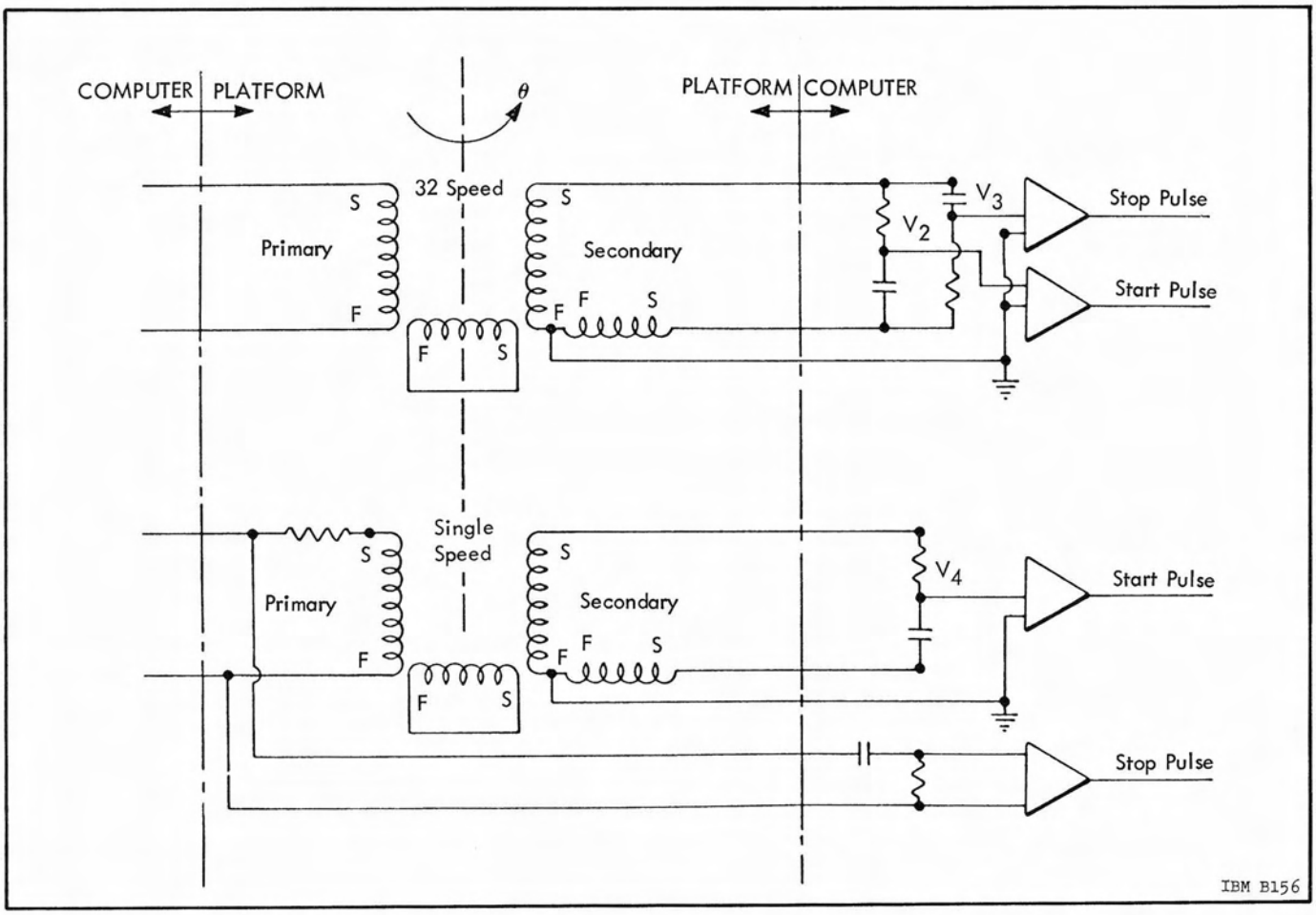


Figure 14.4-2 Two-speed Resolver Schematic

The single-speed winding uses a single RC-passive network which generates a start pulse; the stop pulse is obtained from the reference voltage to the resolver primary as shown in Figure 14.4-2. The method of counting is the same for the high-speed windings. This information is utilized only if the multispeed winding is lost. Thus, degraded accuracy occurs rather than complete failure.

The computer system provides two frequency reference sources, one for the multispeed winding and one for the single-speed winding. These references are controlled by the same frequency standard to insure that the gimbal angle measurement will not be lost if one reference source fails.

The multispeed system accuracy is basically insensitive to temperature variation of the resolver as well as impedance unbalance in the output windings. The open circuit voltage of the resolver is the basic reference voltage as shown in the equations.

The resolver and performance characteristics of the angular readouts are listed in Table 14.4-1.

The Platform system also contains an analogue resolver chain system which can provide vehicle pitch, roll, and yaw attitude steering signals directly to the control system. This is a backup system and is not planned as flight equipment. The capabilities will be utilized in the ground checkout system to program the platform gimbals for vehicle control system calibration.

The resolver chain system includes three servo-driven resolvers whose shafts are time programmed from the ground computer with a maximum rate of 2 degrees per second; operational rate is 1 degree per second. These units are located in the inertial data box.

The resolver chain schematic is shown in Figure 14.4-4. The resolvers X_y, X_x, and X_z are the time programmed units. The characteristics of the resolver chain system are listed in Table 14.4-2.

The resolver chain performs coordinate transformation computations. From Figure 14.4-4, it can be seen that the resolver chain provides six transformation matrices. With proper detection, two chain references (f_1 and f_2) allow vehicle roll, yaw, and pitch signals to be detected from the transformation matrices. The 1.6-kilohertz signal on the $\overline{Z}_B$ winding and the 1.6-kilohertz signal on the $\overline{Y}_B$ at the output of the resolver chain provide the roll and pitch rates, respectively. The 1.92-kilohertz signal on the $\overline{Y}_B$ winding provides the yaw rate. If redundant steer-

Table 14.4-1 Angular Readout Characteristics

Resolver Characteristics	32-Speed	Single-Speed
Excitation voltage	26 V ± 5%	26 V ± 5%
Harmonic content of excitation	0.1%	0.1%
Excitation frequency	1016 Hz ± 0.01%	1016 Hz ± 0.01%
Excitation power	1.8 W	0.08 W
Mechanical accuracy	± 10 arc sec	± 30 arc min
Secondary voltage maximum (open circuit)	5.0 V	5.0 V

System Characteristics	
System high speed	64:1
System low speed	1:1
Static accuracy	± 30 arc seconds
Dynamic accuracy (error is proportional to input rate)	20 arc seconds at 0.2 rad/second
Computer clock frequency	2.048 MHz ± 0.01%
Temperature range for optimum accuracy	± 30° C (54°F)

Table 14.4-2 Resolver Chain System Characteristics

Excitation		Demodulator Output	
f_1	26 V, 1.6 kHz	To control computer	3 Vdc/degree of arc
f_2	26 V, 1.92 kHz	To telemetry (fine)	± 2.5 Vdc/± 3°
		(coarse)	± 2.5 Vdc/± 15°
		Linear range	± 15 degrees

ing signals were required, a third reference (f_3) could be inserted at $\overline{Y}'$ and the detection system would provide an additional roll, yaw, and pitch signal at $\overline{X}_B$ and $\overline{Z}_B$.

The detection scheme for the resolver chain is shown in Figure 14.4-5. When the vehicle coordinate system is aligned to the navigational coordinate system, the $\overline{Z}_B$ winding will have a standing voltage of 15 volts, 1.92 kilohertz which is in phase with vector $\overline{Z}_0$. This bias voltage is removed by a bucking voltage obtained from $\overline{Z}_0$ (f_2). The signals are filtered and, by means of signal bucking, detection filtering, modulation amplification and redetection, are separated as shown in Figure 14.4-5. The output signals are dc with a scale factor of 3 volts per degree. The "3-sigma" accuracy of the resolver chain is 6 arc minutes over a complete cycle.

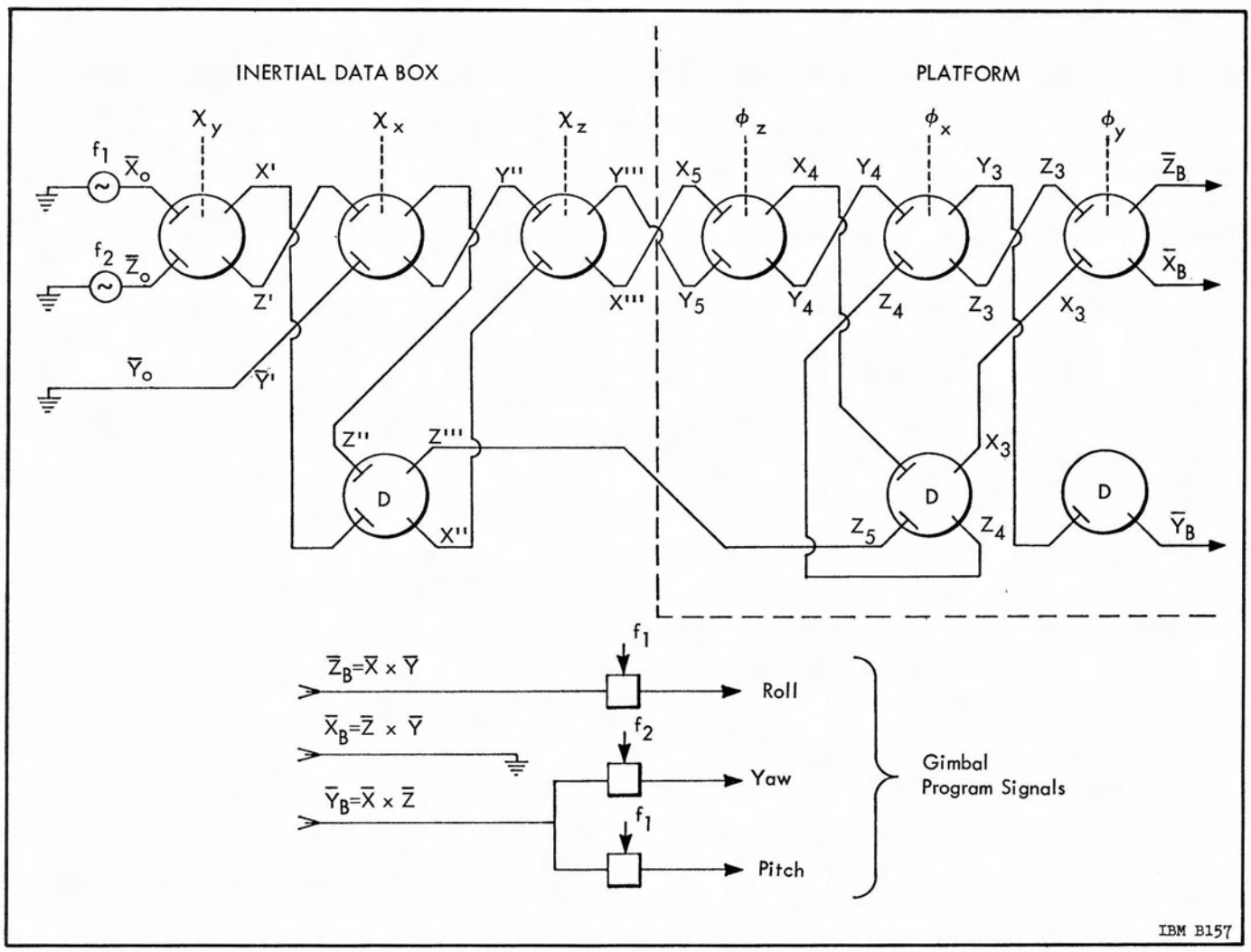


Figure 14.4-4 Resolver Chain Schematic

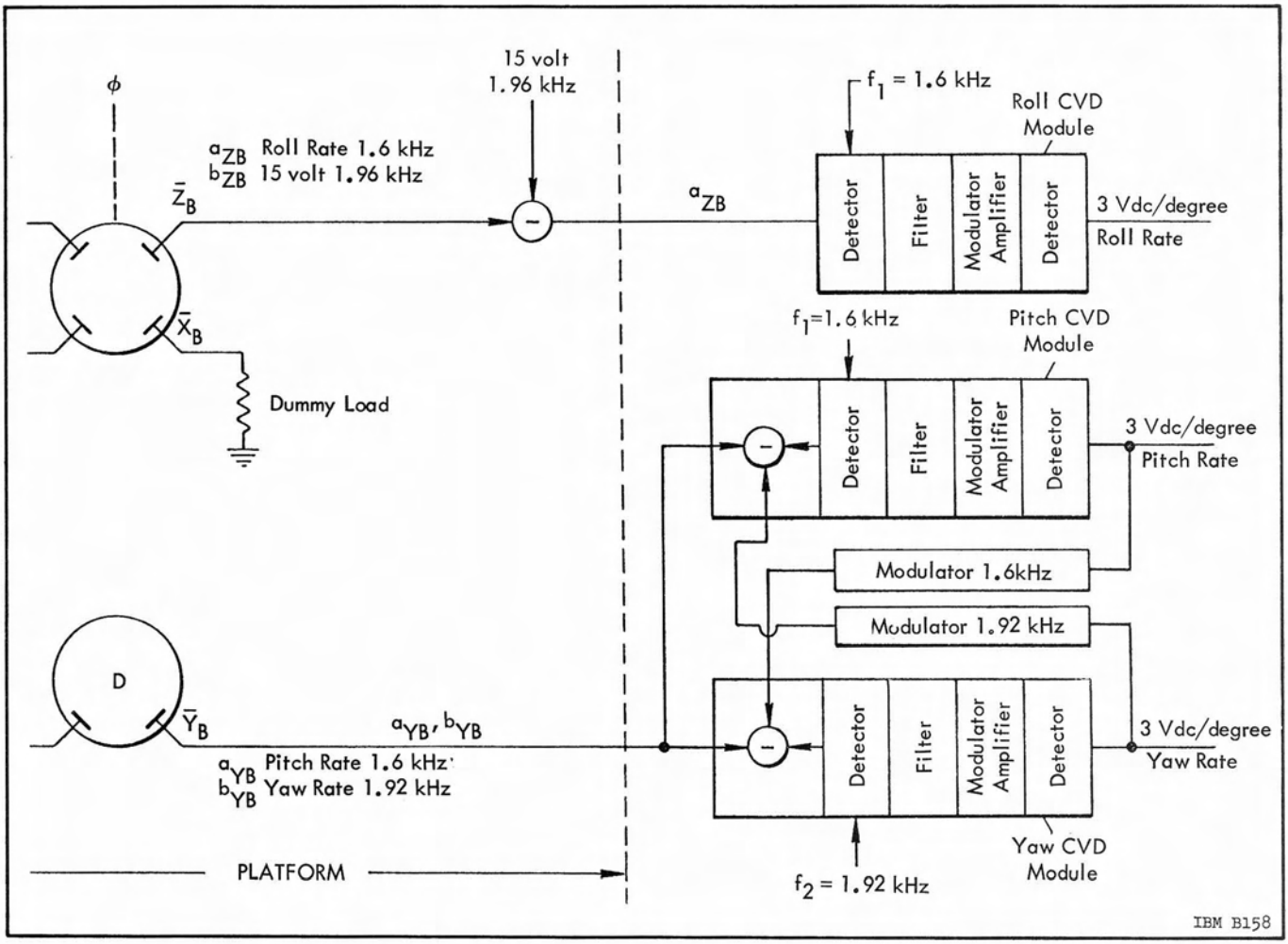


Figure 14.4-5 Resolver Chain Signal Detection Scheme

SECTION 14.5

OTHER PLATFORM SYSTEM UNITS

The ST-124-M Platform Electronic Assembly contains the electronics, other than those located in the Inertial Platform, required for the platform axis and the accelerometer stabilization. Switching electronics for controlling Platform system power and checkout functions are also located in the Platform Electronic Assembly. The electronics are printed circuit, modular constructed, and are fitted into the box with an electrical connector (for ease of assembly and maintenance).

Components or modules requiring pressurization are protected by epoxy encapsulation. Internal heat sources are heat-sinked to the main casting, heat removed by conduction into the temperature' controlled mounting panels of the IU. For system evaluation, critical control signals are conditioned in the Platform Electronic Assembly and supplied to telemetry.

The Platform Electronic Assembly is a cast magnesium structure and is mounted to the vehicle frame with pads which extend out from the box structure. The box has a light-gage sheetmetal cover, gasket-sealed, and pressurized to 1.7 N/cm^2d (2 psid). Internally, the box contains a cast magnesium deck for mounting electronic components and a grooved rack for mounting printed circuit modules. The assembly weighs 19 kilograms (42 pounds).

PLATFORM AC POWER SUPPLY

The ST-124-M Platform AC Power Supply (Figure 14.5-1) furnishes the power required to run the gyro wheels, excitation for the platform gimbal synchros, frequency sources for the resolver chain references, and for gyro and accelerometer servosystems carrier. It is a solid-state-regulated, three-phase, ac power supply, capable of supplying up to 250 VA continuously. With an input voltage from 25 to 30 Vdc, it produces a three-phase sine wave output, which is fixed at 26 volts (rms) line-to-line, at a fixed frequency of 400 ± 0.01 hertz. Three single-phase, 20-volt reference-square-wave outputs of 4.8 kilohertz, 1.92 kilohertz, and 1.6 kilohertz are also provided.

The oscillator generates a temperature-stable square wave of 19.2 kilohertz derived by frequency division from a quartz crystal oscillator. This 19.2-kilohertz square wave is the frequency source from which all the frequency outputs are derived.

The frequency divider network, referenced with the 19.2-kilohertz square wave, produces two buffered 4.8-kilohertz square waves. One 4.8-kilohertz wave becomes the "clock pulse" for the cycle register; the other feeds the regulator-driven amplifier. In addition, the network provides dividers and buffers for the auxiliary outputs. All frequency-divider circuits use Johnson-type counter logic to provide symmetrical square wave outputs to eliminate complicated decoding gates. The network section utilizes integrated circuits construction.

The cyclic register produces six push-pull, square-wave, 400-hertz outputs spaced in 30-degree increments. The 4.8-kilohertz signal from the divider network is used as the clock pulse to trigger the six register flip flops. The flip flops are bistable circuits of the same type (integrated-circuit) used in the frequency divider network.

Each cycle register flip flop drives one channel of the power amplifier. One channel consists of two cascaded push-pull stages which are transformer coupled; all transistors operate in the switching mode, which contributes to the high efficiency of the inverter. Each channel excites a push-pull primary winding of a toroidal output transformer. The secondary windings consist of three per transformer with a 4:3:1 winding ratio (A of Figure 14.5-2). Each of the outputs has 1 winding from each of the 6 transformers (B of Figure 14.5-2) in a combination of 3 pairs with a 4:3:1 wattage ratio. The manner in which these ratios are used in the generation of the sine wave output is illustrated in C of Figure 14.5-2.

The output voltages contain a 15-percent harmonic distortion. A low-pass output filter reduces this distortion by approximately 10:1. The voltage regulator compares a sample of the three-phase output voltage with a stable Zener reference voltage, then amplifies the error and biases the power amplifier to close the loop.

The 19. 2-kilohertz oscillator, the frequency dividers, the network dc supply, and the cycle register operate in dual redundancy. If the 400-hertz voltage is not detected in channel A, a bistable switching circuit will instantly switch power demand to channel B.

The Platform AC Power Supply box is cast magnesium and has a light-gage sheetmetal cover which is gasket-sealed and maintains a pressure of 1. 7 N/cm^2d (2 psid). Modular-potted construction is used throughout. Motherboard printed circuit boards with integrated circuitry minimize internal wiring. The weight of the assembly is 14. 5 kilograms (32 pounds).

ACCELEROMETER SIGNAL CONDITIONER

The Accelerometer Signal Conditioner accepts the velocity signals from the accelerometer optical encoders and shapes them before they are passed on to the guidance computer. Each accelerometer requires 4 shapers — a sine shaper and a cosine shaper for the active channel and a sine shaper and cosine shaper for the redundant channel. Also included are four buffer amplifiers for each accelerometer — one

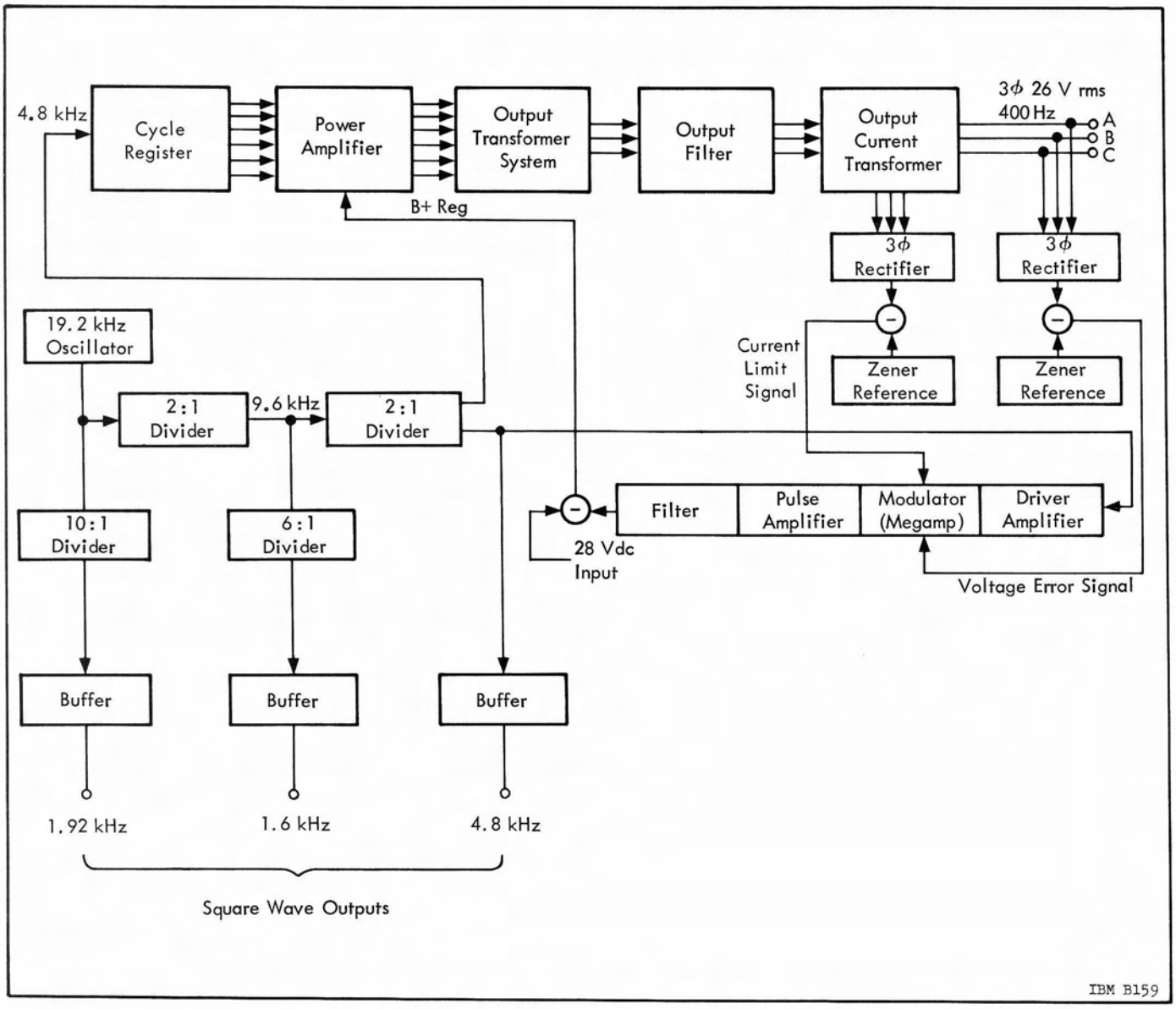


Figure 14. 5-1 Platform AC Power Supply Assembly

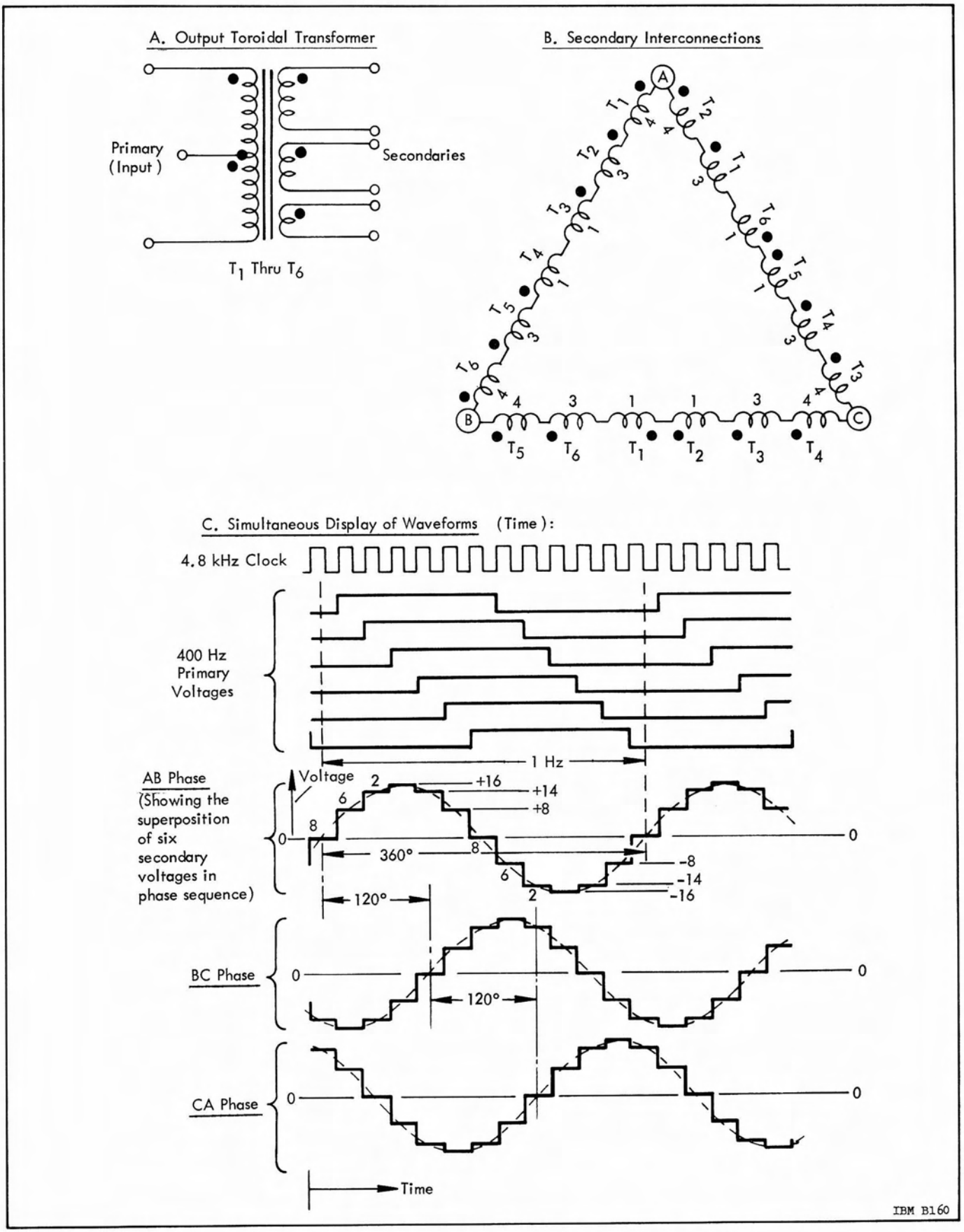


Figure 14.5-2 Generation of 3-Phase, 400-Hertz Voltage

for each sine and cosine output. The output of these buffers is furnished to the blockhouse for a prelaunch accelerometer calibration check. The accelerometer telemetry velocity signals are also conditioned in this assembly. Characteristics of the velocity signals are listed in Table 14. 5-1.

The total assembly weighs approximately 4. 5 kilograms (10 pounds) and is fabricated from a magnesium casting. Light-gage sheetmetal covers with gasket seals maintain as intermal pressure of 1. 7 N/cm^2d (2 psid).

Table 14. 5-1 Characteristics of the Accelerometer TM Velocity Signals

Output voltage levels	0-6 volts minimum (3 volt bias) 0-8 volts maximum (4 volt bias)
Signal rise time	50 us on square wave
Output frequency of acceleration signal	+ 60 g (50 Hz/g) - 30 g (50 Hz/g)

SECTION 14.6

PLATFORM ERECTION SYSTEM

The erection of the platform to the local vertical is accomplished by two gas bearing pendulums which are fitted to the inner gimbal. The input axes of the pendulums are parallel to the X and Z accelerometer measuring axes.

The gas bearing pendulum is a single-axis gravity-sensing device. Its sensing element is a gas-floated slug which supports a soft iron core as shown in the cutaway view of Figure 14.6-1. The iron slug moves inside the coils of a linear differential transformer which provides the electrical output signal. Damping of the slug motion is provided by a chamber and an exhaust orifice while the spring restraint is obtained magnetically.

The characteristics of the pendulums are listed in Table 14.6-1.

The block diagram of the erection system is shown in Figure 14.6-2. The input axes of the X and Z pendulums are along the inertial gimbal Z and X axes, respectively. The pendulum output is amplified by a preamplifier on the Inertial Platform and then transmitted to the ground equipment alignment amplifier.

The alignment amplifier provides a proportional plus integral path to the torque driver amplifier, which returns the signal from the ground to the variable coil of the gyro torque generator. The erection system is a second order system with a natural frequency of 0.05 radian per second and a damping ratio of 0.5. The leveling accuracy of the erection system is $\pm$ 3 arc seconds.

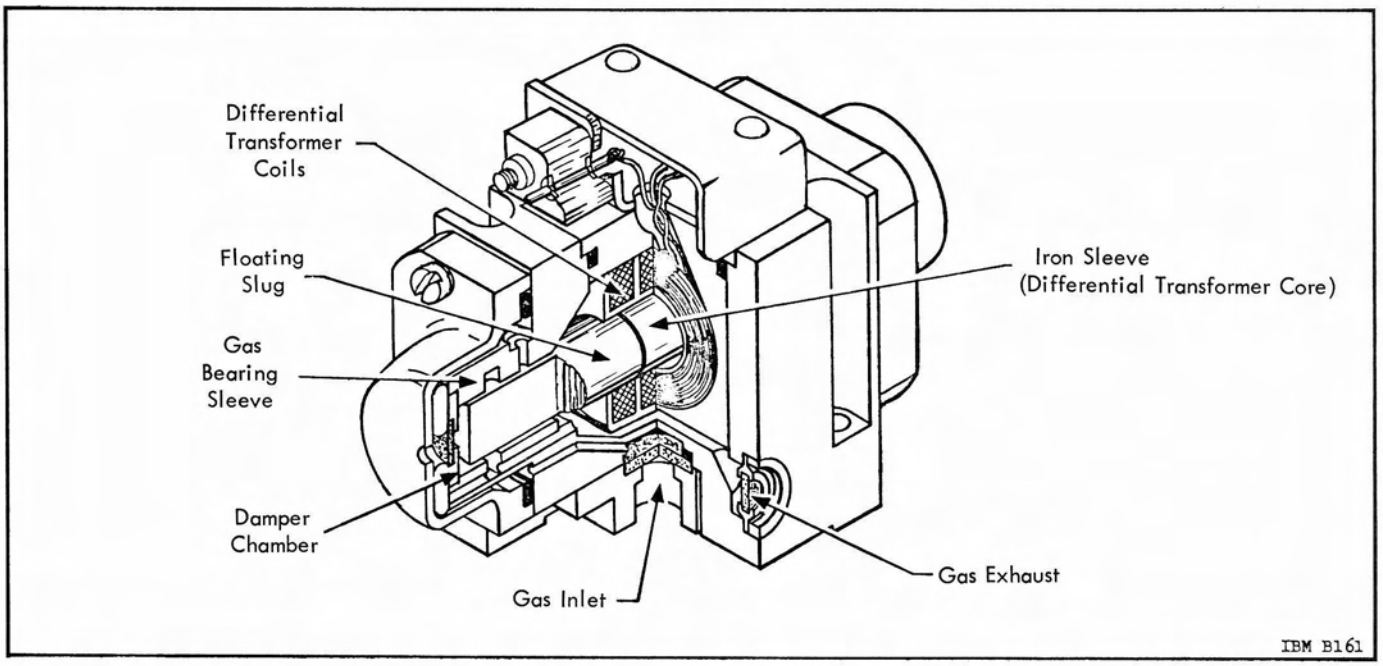


Figure 14.6-1 Gas Bearing Pendulum

Table 14.6-1 Gas Bearing Pendulum Characteristics

Physical Characteristics	
Size	5.7 cm x 3.8 cm x 3.2 cm (2.25 in. x 1.5 in. x 1.25 in.)
Weight	92 grams (0.2 pound)
Gas Bearing	
Gas pressure	10.3 N/cm^2d (15 psid)
Gas flow	100 cc/min STP (6.1 $in.^3$/min)
Gas gap	0.015 to 0.02 cm (0.006 to 0.008 in.)
Signal Generator	
Type	Inductive
Excitation	4 V, 400 hertz
Sensitivity	300 mV/degree
Performance	
Leveling accuracy	± 5 arc seconds
Input range	± 0.5° (signal saturation)
Time constant	10 seconds

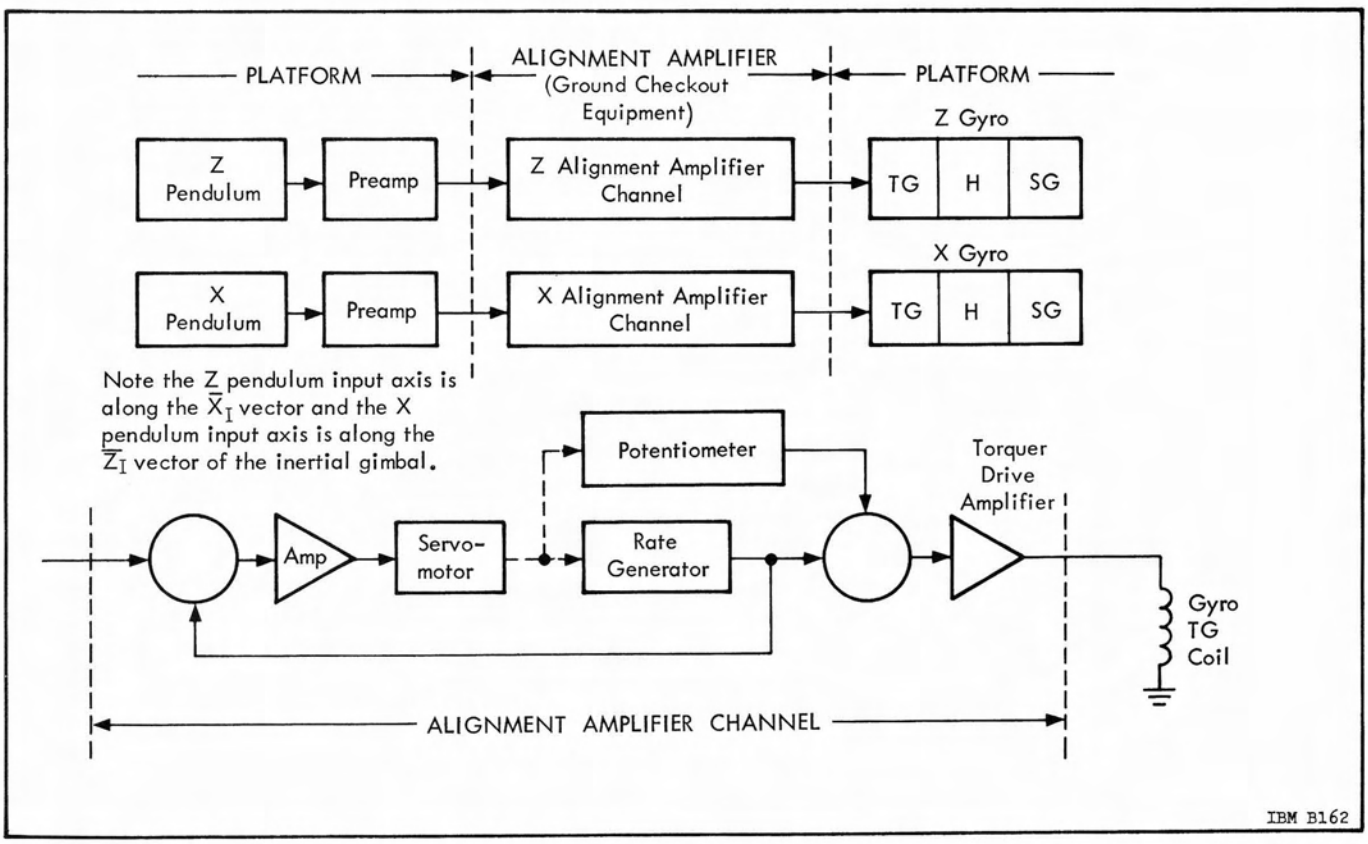


Figure 14.6-2 Platform Erection System Block Diagram

SECTION 14.7

AZIMUTH ALIGNMENT SYSTEM

The azimuth alignment system orients the Inertial Platform +X coordinate axis to the desired flight azimuth. To obtain the high accuracy requirement, the azimuth alignment system utilizes electro-optical techniques. The basic elements of the azimuth alignment system are an autocollimating theodolite with detection system, synchro encoder servosubsystem, launch control computer for azimuth programming and reference, and an alignment torquing servosubsystem. Fitted to the inertial gimbal is a porro prism (intermediate infrared) with its dihedral edge parallel to the X axis of the inertial gimbal. A second prism (near infrared) is fitted to the stator of the two-speed synchro which has its dihedral edge free to rotate in the X-Z plane (Figure 14.7-1).

The basic element of the optical system is the SV-M2 Theodolite (Figure 14.7-2). The system consists of an autocollimating theodolite with necessary optics and detectors, a penta mirror set, an automatic sway control system, reference prism with stand, closed circuit TV monitoring system, and support electronics and control.

The theodolite has three control channels — the synchro prism, the inertial prism, and a trihedral prism (Figure 14.7-3). An infrared energy spectrum is generated by a tungsten filament lamp. This spectrum has a bandwidth of two microns which lie between 0.7 and 2.7 microns. Atmospheric absorption of infrared in this bandwidth occurs at 1.35 and 1.8 microns. Therefore, the control channels are divided at 1.35 and 1.8 microns with the 0.7 to 1.35 microns near infrared-band assigned to the synchro prism, the 1.25 to 1.8 microns intermediate infrared-band assigned to the inertial prism, and 1.8 to 2.6 micron far infrared-band assigned to the trihedral prism (Figure 14.7-4). The prisms have a dichroic multilayer coating that allows only the desired bandwidth of energy to pass.

The angular position of the synchro prism is controlled directly from the theodolite. A theodolite error signal drives a servoamplifier which is located in the launch umbilical tower. The amplifier output is transmitted to the Inertial Platform where it excites a servomotor located on the inertial gimbal. The servomotor positions the synchro prism throuh a gear train of 10^5:1, reducing any angular error to zero. This loop is active throughout countdown until vehicle lift-off. The angle between the inertial gimbal (navigation coordinates) and movable prism is measured by a precision 25:1 dual-speed control transmitter synchro (Figure 14.7-5). The inertial prism is controlled by the theodolite output signal through the roll alignment servoelectronics by torquing the roll gimbal until the prism is in the desired azimuth plane.

The trihedral prism, which is fixed to the vehicle, is used as reference for a servosystem to position the penta mirror which provides the theodolite with the capability of translatory tracking. At the vehicle elevation of the Platform system, the SV-M2 Theodolite (Saturn V, Mod 2) will compensate for a ± 35.5 centimeters (± 14 inches) translation movement of the vehicle. The trihedral prism servoloop increases the aperture of the autocollimator from 20 centimeters (8 inches) to 85 centimeters (32 inches) at a rate of 76 centimeters/second (32 inches/second).

Prism acquisition signals from the three channels are generated with the same infrared-coded bandwidths that produce the error signals. These are used to automatically block and/or initiate other events in the vehicle launch procedure and azimuth alignment system. Indicator lights on the theodolite control panel in the launch control center confirm that the 3 prisms are in the acquisition range of the theodolite. Two closed-circuit TV monitor systems provide the launch control center with a view of the 3 prisms and a monitor of the theodolite control and display panel in the theodolite hut.

The elevation angle (nominally 25 degrees from horizontal) of the theodolite is set by a dc motor-driven actuator which is manually controlled

from the launch control center. At the Saturn V launch complex, the theodolite can operate with a ± 35.5 centimeter (± 14 inches) variation in elevation without requiring any adjustment.

The encoder-synchro package consists of a 25:1 dual-synchro, an 18-bit optical shaft angle encoder, and a motor-tachometer-gear assembly. The encoder is provided with an enclosure containing strip heaters to maintain the temperature within ± 5°C (9°F), maintaining the designed accuracy of ± 10 arc seconds. The encoder system has a self-generated encoder sampling time of 20 milliseconds. The output is a cyclic gray code with logic levels of 0 or 28 volts. The 25:1 dual synchro with the platform dual synchro has a back-to-back control transmitter: control transformer error of ± 10 arc seconds.

The reflected infrared energy from the prisms is acquired by the theodolite's optics. From this coded energy, the theodolite detects deviations from the desired position of the prisms. These coded signals are separated into their respective channels by slit prism angle filters and dichroic beam splitters.

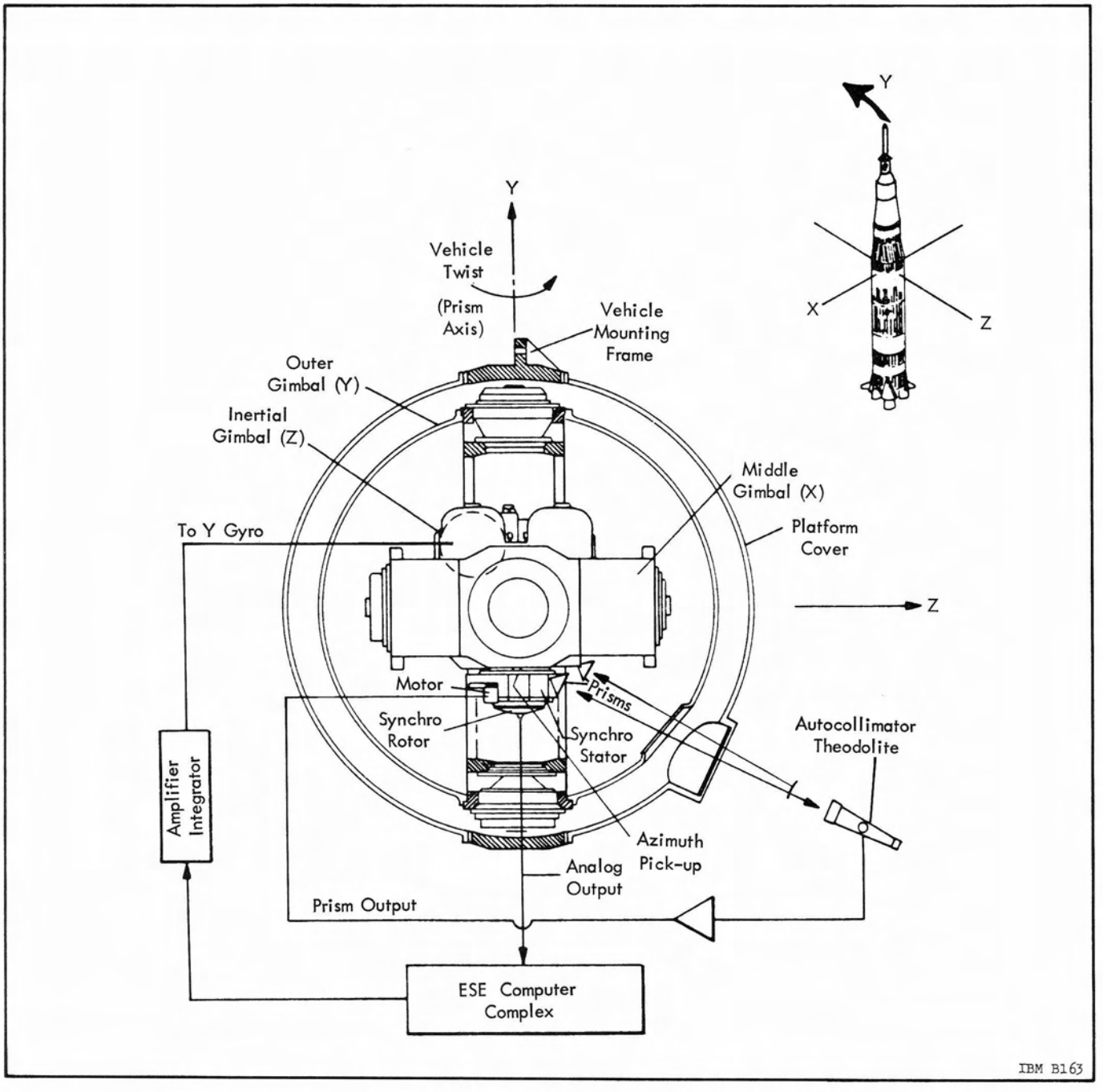


Figure 14.7-1 Automatic Azimuth Alignment

The dichroic beam splitters have a dichroic multilayer coating similar to the prisms. Each of the three channels has acquisition detectors which generate dc signals when the prisms are within the acquisition range of the theodolite. These signals are used to indicate acquisition and to control relay switching in various other vehicle-associated control functions. When an error exists in any channel, a representative portion of the infrared energy passes through the slit prism filter to the dichroic beam splitter and on to a lead sulfide detector. A phase-oriented ac voltage is generated which is directionally proportional to the angular error. This voltage is amplified and demodulated to achieve the desired signal gradient of 100 millivolts per arc second.

The simplified azimuth block diagram in Figure 14.7-6 shows the operation of the azimuth alignment system. After all systems have been energized, the erection system positions the inertial gimbal to the local vertical. The azimuth alignment equipment is switched into the acquisition mode. This closes contacts A, B, C, and D and opens contacts E, F, G, and H. A bias signal is injected into the synchro prism servoloop to drive this prism into acquisition; the acquisition signal removes the bias and closes the synchro prism servoloop on the theodolite and drives the synchro prism to null.

The output of the dual-speed control transformer drives the encoder-synchro servoloop until the synchro output is zero through contact E. The RCA-110A Launch Computer reads and stores the position of the 18-bit encoder. Thus, the baseline azimuth is stored in the computer. This is the azimuth of the navigation coordinate system and is the reference from which launch azimuth is established. Any deviation from this position will generate an error signal in the CX:CT measurement causing the Y gyros to torque the gimbal and reduce the error to zero.

The mission azimuth is established with contacts A, B, C, and D open and contacts E, F, G, and H closed. The launch control computer computes the

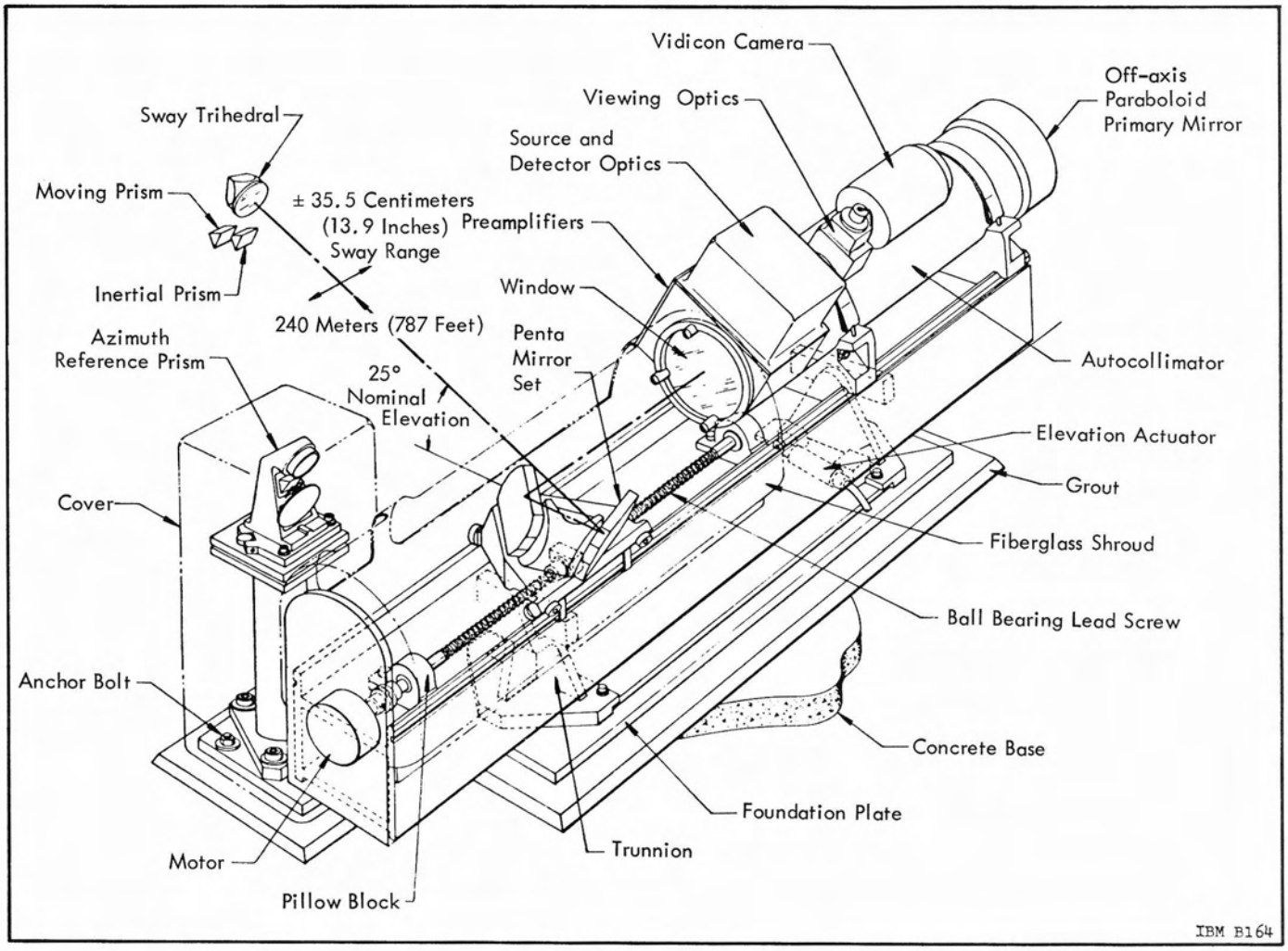


Figure 14.7-2 Theodolite

azimuth program angle by comparing the baseline azimuth to the stored mission azimuth and torquing the synchro-encoder repeater until the encoder output agrees with the computer. The error signal from the dual-speed synchro system if fed to the Y gyro alignment loop and drives the inertial gimbal to the mission azimuth which also nulls the CX:CT unbalance. The synchro prism is held fixed with respect to the optical beam from the theodolite on the baseline azimuth. The inertial gimbal (navigation coordinates) is held on the mission azimuth with the CT acting as an azimuth pickoff. The azimuth angle computation is a function of the predicted launch time. The computer program translates any deviations from the predicted launch time into a respective azimuth angle change and repositions the inertial gimbal to the changing azimuth through the encoder synchro. The mission azimuth is displayed in the launch control center by a digital monitor.

The analysis of the azimuth alignment error shows the root sum squared system error to be less than ± 20 arc seconds.

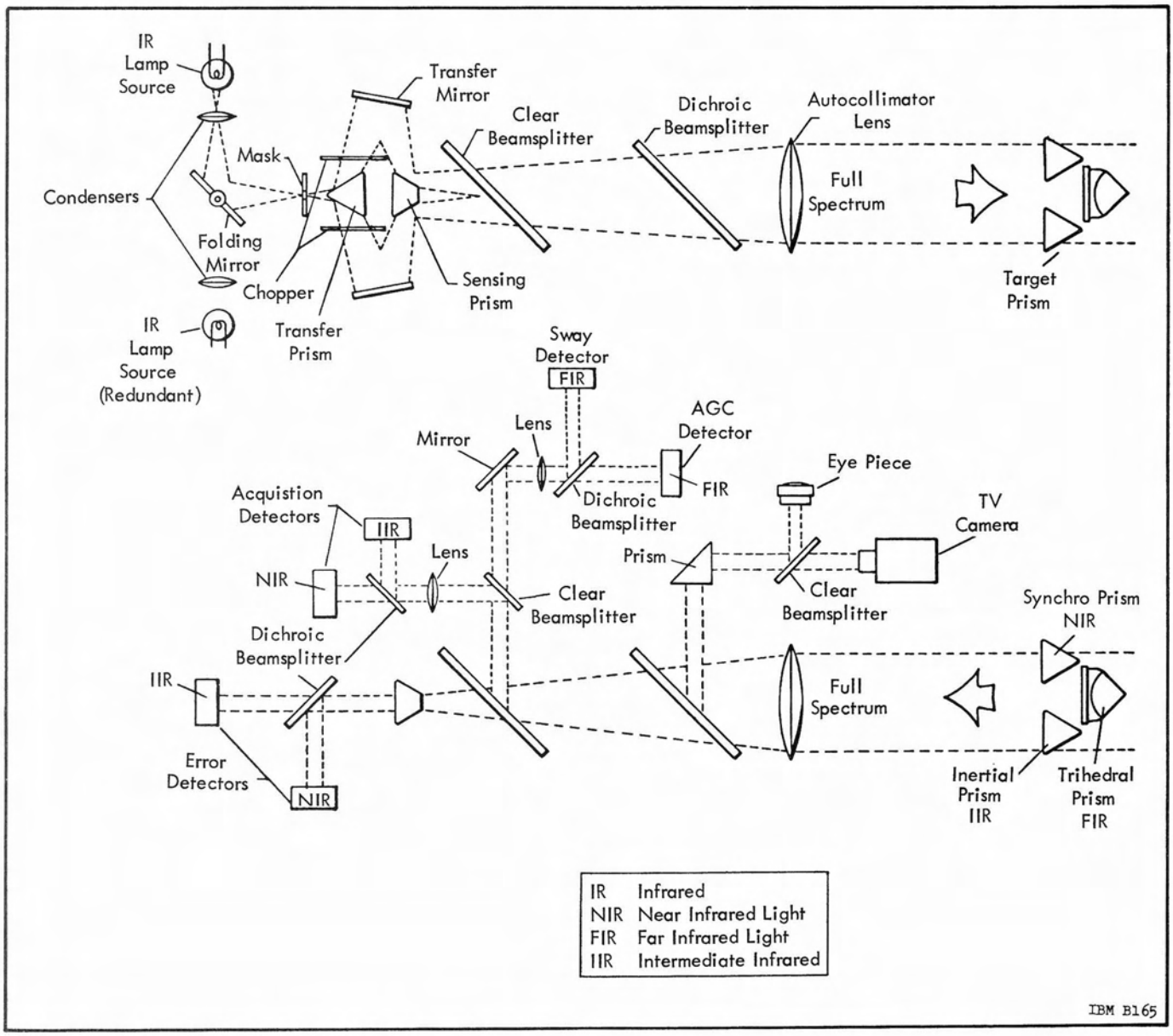


Figure 14.7-3 Optical Schematic Diagram of SV-M2 Theodolite

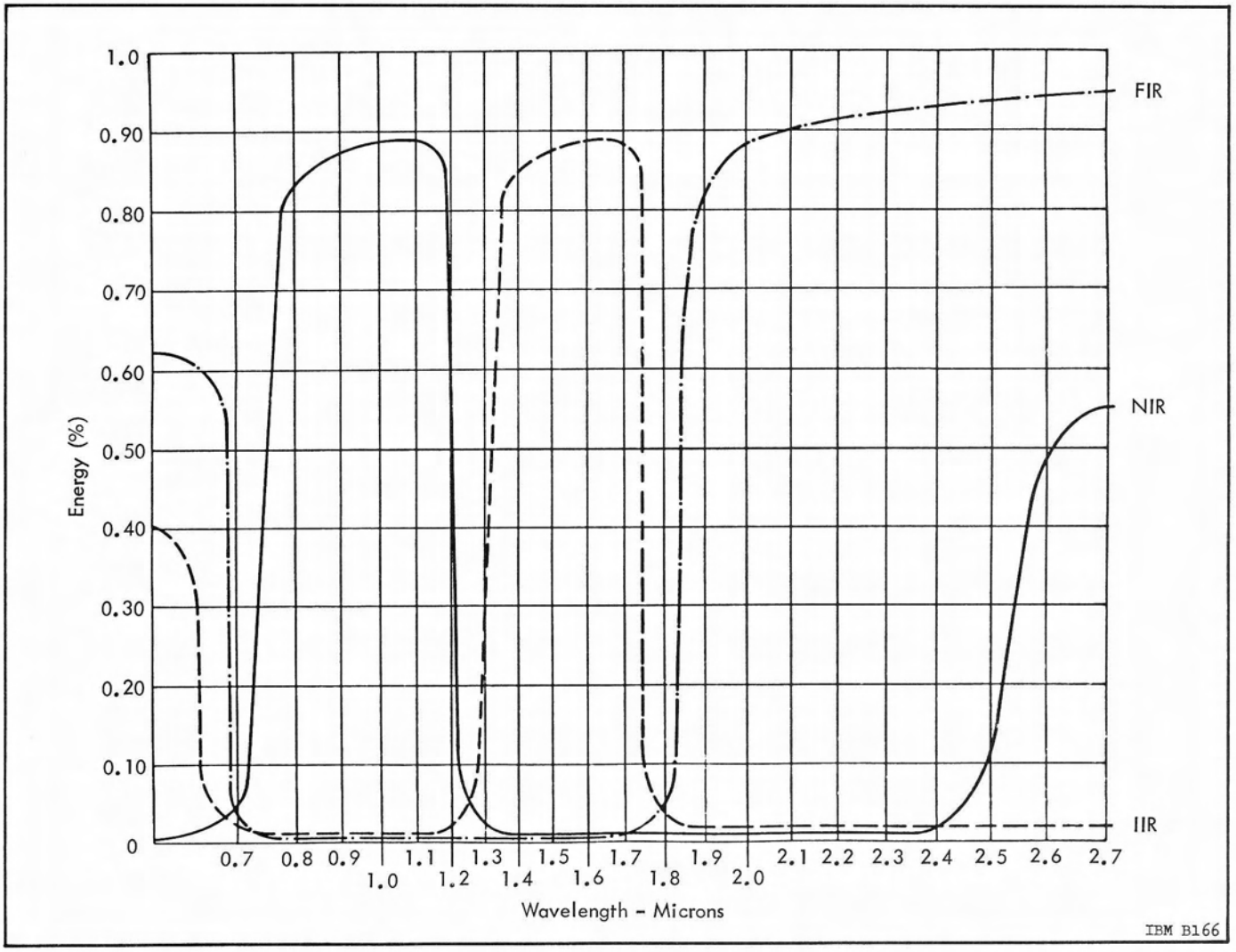


Figure 14.7-4 Optical Spectrum

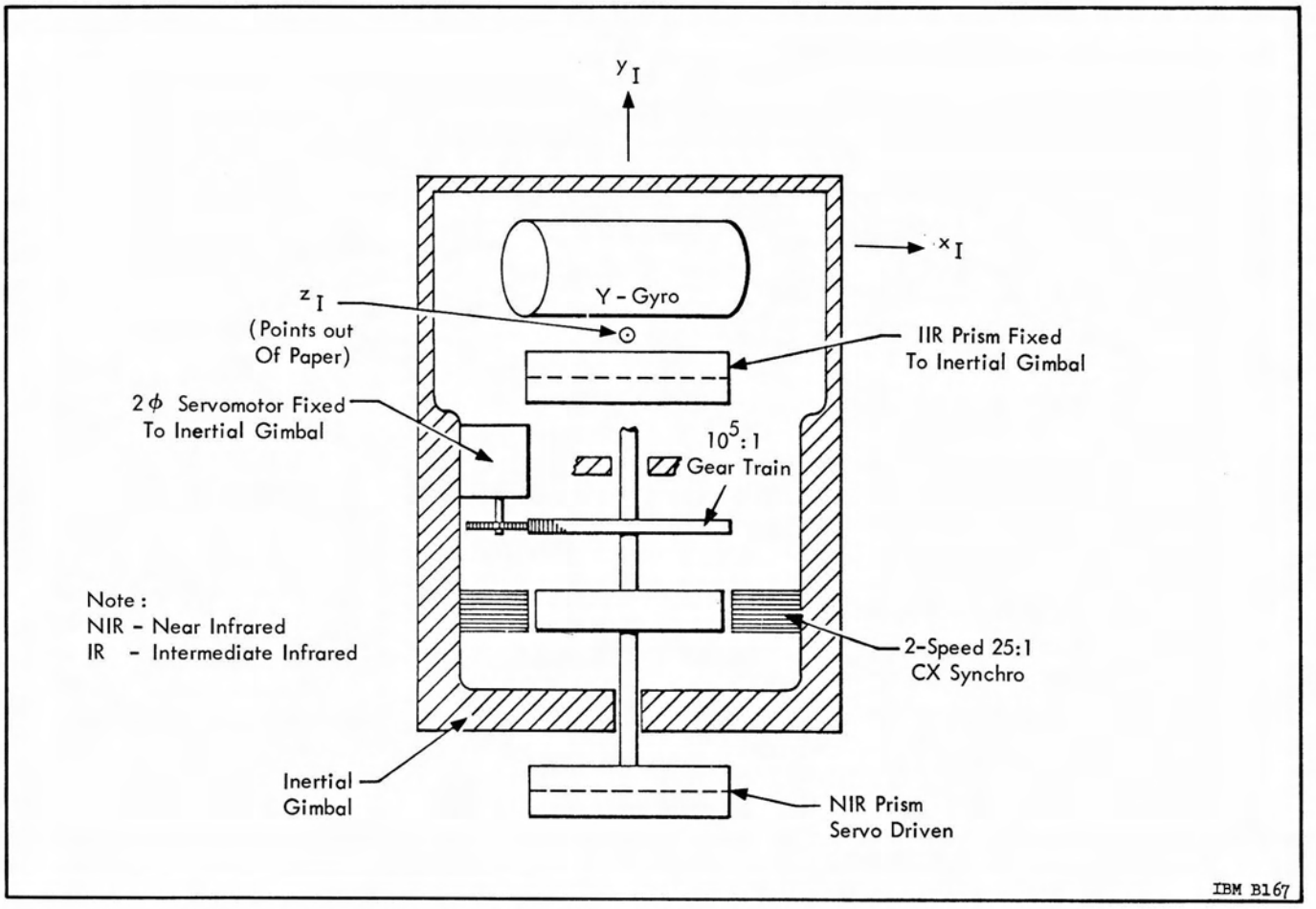


Figure 14.7-5 Optical Gimbal Laying System

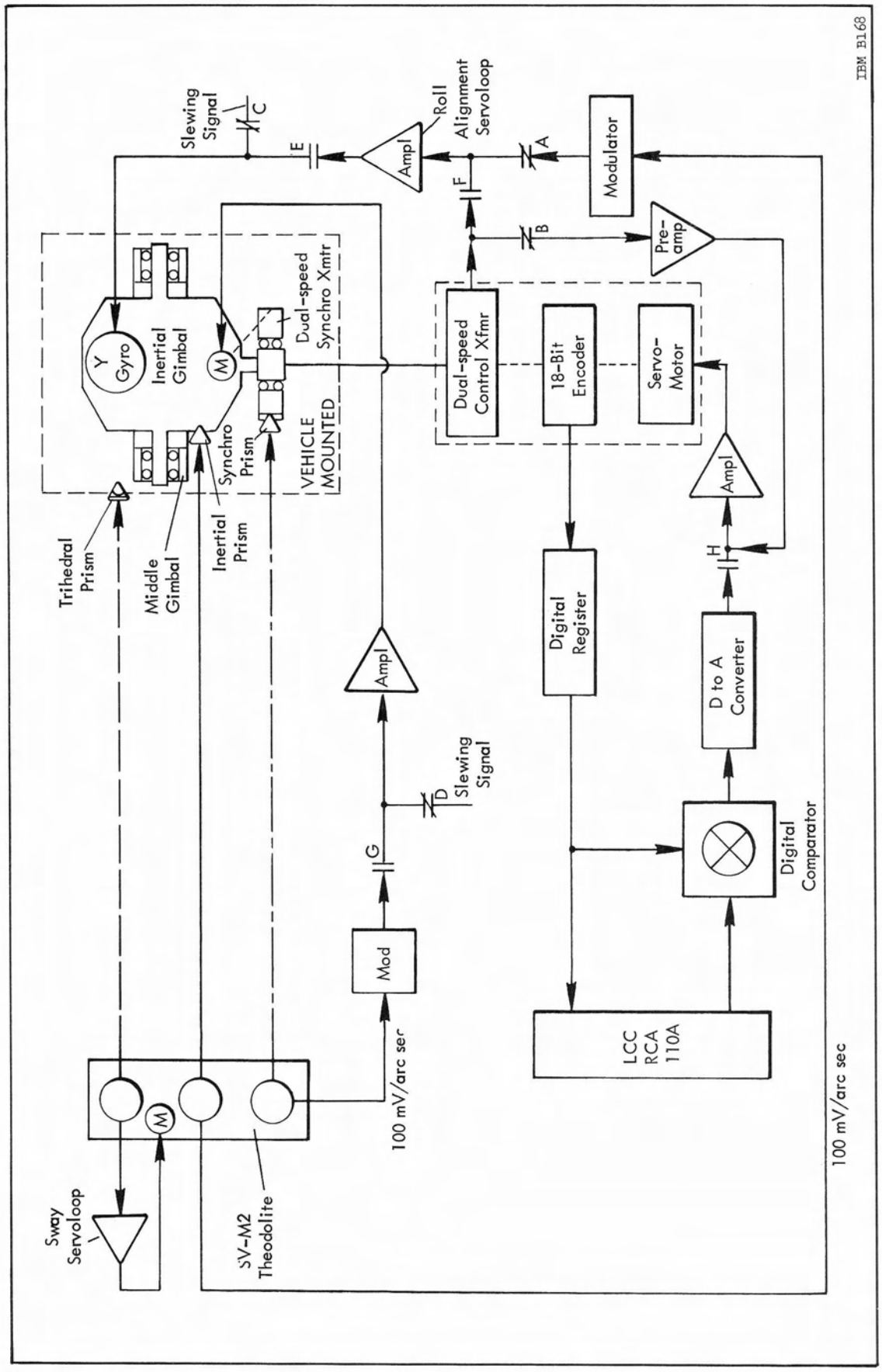


Figure 14.7-6 Azimuth Alignment Scheme

SECTION 14.8

GAS BEARING GYRO

The ST-124-M Inertial Platform Assembly contains three AB5-K8 gas bearing single-degree-of-freedom gyros. These components measure the vehicle motion; their performance capabilities define the hardware accuracies of the guidance system. No active compensation is used in the LVDC for instrument error terms and absolute tolerances are established for the life of the instruments.

The gas bearing gyro is shown in a cutaway view of Figure 14.8-1. The cylindrical, externally-pressurized gas bearing suspends the cylinder between the sleeve and endplates, as shown in Figure 14.8-2, and provides both axial and radial centering. The endplates are bolted to the sleeve and their assembly forms the case of the gyro.

Dry gaseous nitrogen is passed through two rows of 24 holes with millipore discs in the sleeve to act as flow diffusers and provide the bearing stiffness. The gas in the cylinder chamber generates the hydrostatic bearing and flows symmetrically to both endplates, escaping around the hub at each end of the cylinder. The sleeve, endplates, and cylinder are constructed of beryllium with machined tolerances of 20 microinches in roundness and 20 microinches per inch in squareness.

The gyro wheel shown in Figure 14.8-2 mounts in a yoke of the cylinder endcap. The neck section of the yoke is controlled to minimize the anisoelastic drift of the wheel assembly. The endcap is mounted in the cylinder forming the gyro cylinder assembly. The cylinder is helium filled to reduce windage losses. The wheel is a two-pole, synchronous hysteresis motor. Precision bearings are fabricated to the beryllium shaft with the motor laminations and windings to form the stator of the wheel. The rotor is made up of an elkonite ring with P-6 hysteresis laminations shrunk-fitted into the elkonite ring and beryllium endbells which are bolted to each side.

The signal generator and torque generator, shown in Figure 14.8-2, are coupled to the cylinder by means of a copper-shorted loop which is mounted on the cylinder. The signal generator is an ac-type, shorted-loop, single-winding sensor for the angular displacement of the gyro about its output axis. The torque generator operates like an eddy current motor. It provides only alignment torques for initial erection. The 3-phase, 400-hertz wheel power is transmitted by ribbon flex leads to standoffs on the gyro cylinder. A magnetic shield is placed between the gyro case and the signal generator. Dust covers, which are also magnetic shields, complete the assembly.

The electrical schematic for the AB5-K8 stabilizing gyro is shown in Figure 14.8-3. The coordinate definition for a single gyro is also shown. The wheel phase rotation A-B-C, American Standard, with the gyro connected to the 26-volt, 400-hertz supply, causes the gyro wheel to rotate in a negative direction about the gyro spin reference (Y_{GU}) vector.

Table 14.8-1 lists the gyro characteristics.

Table 14.8-1 Gyro Characteristics

Gyro Wheel	
Type	Synchronous hysteresis
Angular momentum	2.6×10^6 g cm^2/s
Wheel speed	24,000 rpm
Wheel excitation	26 V, 3-phase, 400 Hz
Wheel bearing preload	3.4 kg, operating (7.5 pounds)
Wheel power at sync	8 W
Wheel life	3000 hours, minimum
Wheel mount	Symmetrical
Wheel sync time	90 seconds
Gas Bearing	
Gas pressure	10.3 N/cm^2d (15 psid)
Gas flow rate	2000 cc/min STP (122 $in.^3$/min)
Gas gap (one side)	0.015 to 0.02 cm (0.006 to 0.008 in.)
Orifice restrictors	Millipore discs
Sleeve material	Anodized beryllium
Endplate material	Anodized beryllium
Cylinder material	Anodized beryllium
Signal Generator	
Type	Short turn reluctance
Excitation	10 V, 4.8 kHz
Sensitivity	550 mV/° with 10 k load
Float freedom	$\pm 3^{\circ}{}^{+0^{\circ}}_{-0.5^{\circ}}$
Torquer (for platform erection and earth rate bias only)	
Type	Shorted turn reluctance
Normal erection rate	6°/min
Fixed coil excitation	26 V, 400 Hz, 45 mA
Maximum variable coil excitation	30 V, 400 Hz, 50 mA
Impedance	
Fixed coil resistance	184 Ω
Fixed coil impedance	555 Ω ∠+31° (400 Hz)
Variable coil resistance	190 Ω
Variable coil impedance	330 Ω ∠+53° (400 Hz)

Table 14.8-1 Gyro Characteristics (Cont'd)

Physical Characteristics	
Size	
Diameter	7.7 cm (3 inches)
Length	10.3 cm (4 inches)
Weight	900 grams (2 pounds)
Mounting	3-point flange mounting
Temperature Characteristics	
Calibration temperature	40°C (104°F) (gyro housing)
Drift versus temperature gradient	0.009°/h/°C

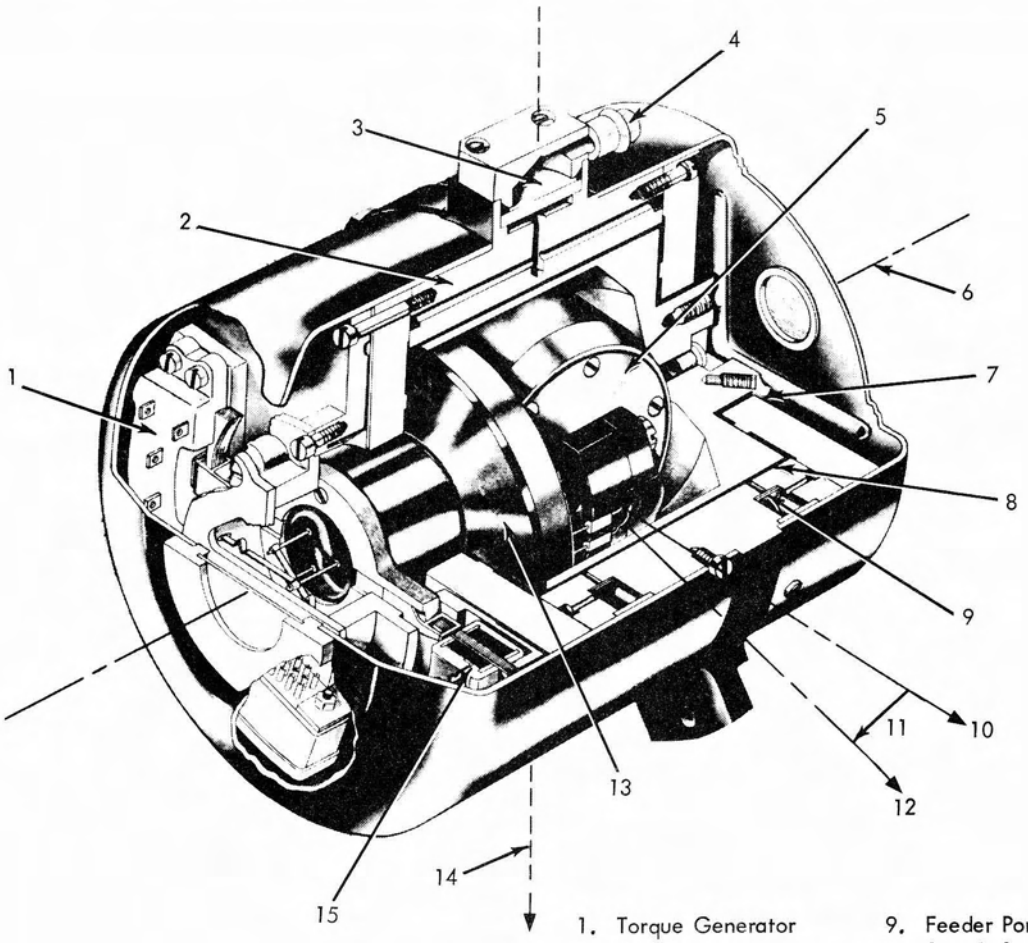


Figure 14.8-1 Cutaway View of a Single-axis Integrating Gyro

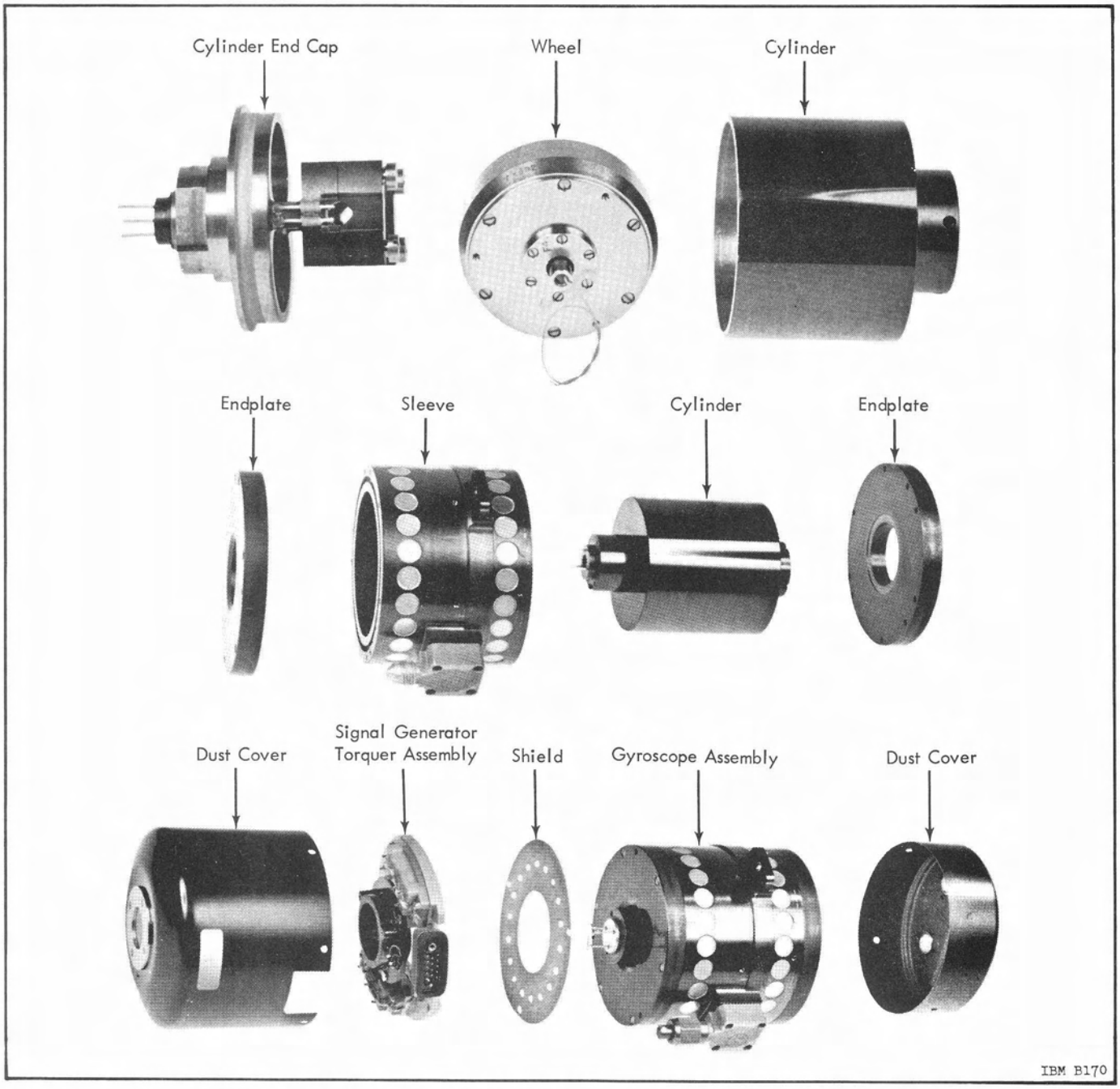


Figure 14.8-2 Exploded View of a Signal Generator and Torque Generator

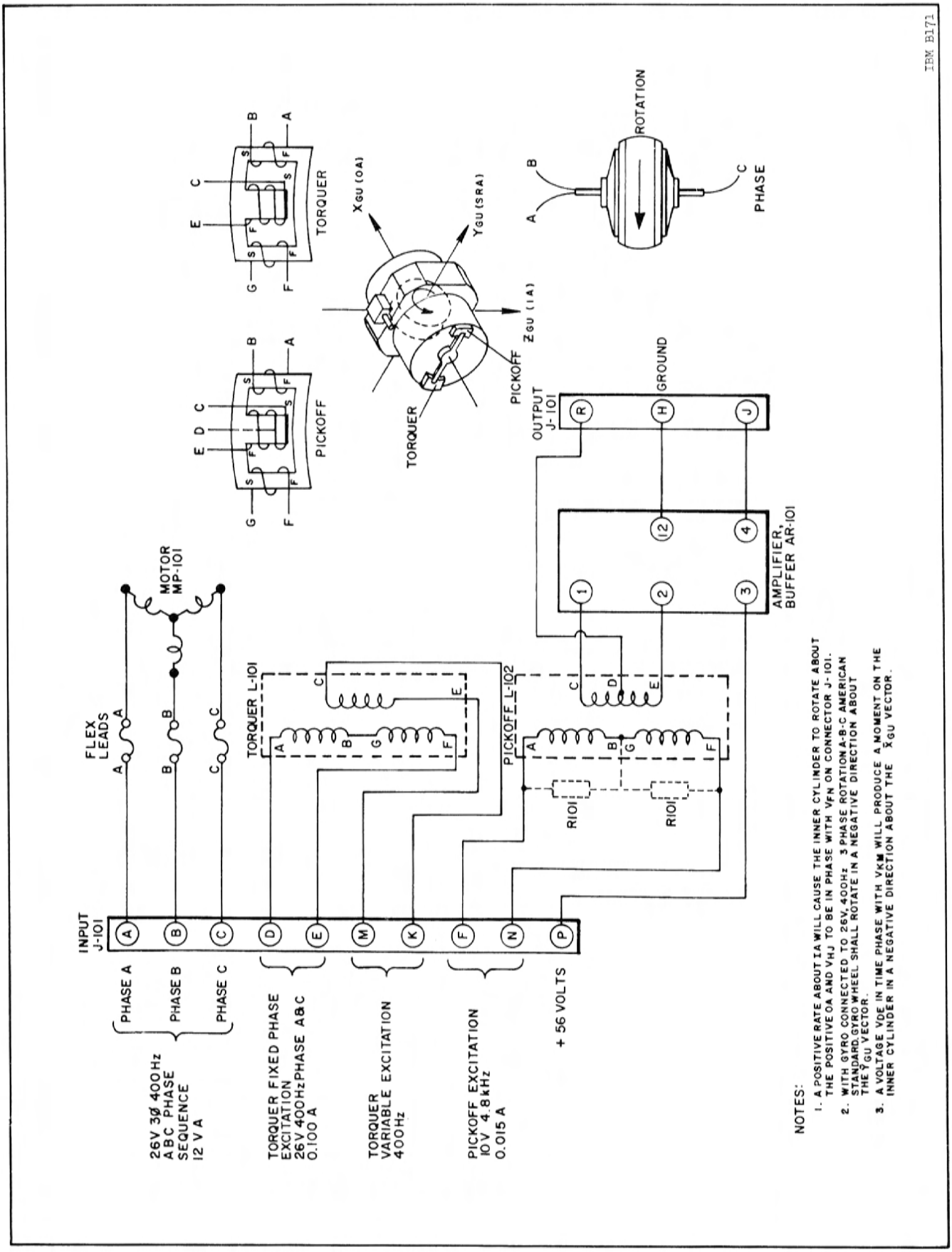


Figure 14.8-3 Electrical Schematic of an AB5-K8 Stabilizing Gyroscope

SECTION 14.9

PENDULOUS GYRO ACCELEROMETER

The AB3-K8 instrument is a pendulous gyro accelerometer; a cutaway view and schematic is shown in Figure 14.9-1 and Figure 14.9-2, respectively.

The accelerometer is a single degree-of-freedom gyro unbalanced about its output axis. The gyro motor and flywheel of the gyro accelerometer are shifted along the spin reference axis to obtain desired pendulosity about the gyro output axis. The pendulous cylinder is machined with a pair of pivots mounted into a frame with a set of Class-7 bearings. Thus, the cylinder is free to rotate about the gyro input axis, which is aligned in the acceleration-measuring direction. A torque is produced by the unbalance or pendulosity which is proportional to the acceleration to which the pendulous mass is subjected. The precession angle of the gyro is proportional to the integral of the acceleration. A signal generator measures the precession angle and a servo closes the loop to a direct-axis torquer which is mounted on the gyro input axis. Thus, the gyro measuring head is stabilized and the pendulous weight is held perpendicular to the input axis. The speed of the measuring head or gyro, with respect to inertial space, is proportional to thrust acceleration along the input axis, and the position of the measuring head is a measure of thrust velocity. An optical incremental encoder is mounted on the input axis and provides a measure of the thrust velocity. The power source for the synchronous spin motor is referenced from a crystal-controlled frequency, guaranteeing a constant accelerometer scale factor, or velocity increment/revolution, about the input axis.

The symmetrical gyro wheel is mounted in a cylinder that is suspended on a hydrostatic gas bearing. The gyro is constructed the same as the AB5-K8 gyro except there are two rows of 18 holes for feeding gas into the bearing. All nonmagnetic parts are machined from beryllium material except the endplates. which are fabricated of Monel to reduce the servoloop nutation frequency.

The electrical schematic for the AB3-K8 accelerometer is shown in Figure 14.9-3. The wheel phase rotation A-B-C, American Standard, with the gyro connected to a 26-volt, 400-hertz, 3-phase power supply, causes the wheel to rotate in a positive direction about the spin reference axis vector.

Table 14.9-1 lists the accelerometer characteristics.

Table 14.9-1 Accelerometer Characteristics

Gyro Wheel	
Type	Synchronous hysteresis
Angular momentum	94,000 g cm^2/second (207 pounds)
Wheel speed	12,000 rpm
Wheel excitation	26 V, 3-phase, 400 Hz
Wheel sync time	90 seconds
Wheel power at sync	4.5 W
Wheel life	3000 hours, minimum
Wheel mount	Symmetrical
Wheel bearing preload	907.2 grams (1.99 pounds) operating

Table 14. 9-1 Accelerometer Characteristics (Cont'd)

Gas Bearing	
Gas pressure	10. 3 $N/cm^2 d$ (15 psid)
Gas flow rate	2400 cc/min STP ($146\ in.^3/min$)
Gas gap	0. 015 to 0. 02 cm (0. 006 to 0. 008 in.)
Orifice restrictors	Millipore discs
Sleeve material	Anodized beryllium
Endplate material	Monel
Cylinder material	Anodized beryllium
Signal Generator	
Type	4-pole shorted turn reluctance
Excitation	10 V, 4. 8 kHz
Sensitivity	285 mV/° with 700 Ω load
Float freedom	$\pm 3^{\circ}\ ^{+0^{\circ}}_{-0.5^{\circ}}$
Torque Motor	
Type	Direct-axis dc torquer
Maximum torque	1. 44 kg cm at 1. 1A and 44V
DC resistance	32. 6 ohms
Inductance	12. 5 millihenries
Velocity Pickoff	
Type	Digital encoder (optical grid)
Count	6000 count/revolution
Resolution	5 cm/s/bit (1. 96 in. /s/bit)
Output	Incremental with redundant channels
Physical Characteristics	
Size	
Diameter	8. 3 cm (3. 25 inches)
Length	12. 8 cm (5 inches)
Weight	1200 g (2. 64 pounds)
Mounting	3-point flange mounting

Table 14.9-1 Accelerometer Characteristics (Cont'd)

Performance	
Accelerometer scale factor	300 m/s/revolution of output axis (985 feet/s/revolution)
Pendulosity	20 g cm
Temperature Characteristics	
Calibration temperature	40°C ambient (104°F) (on housing gyro)
Ambient temperature range for required accuracies	40°C ± 3°C (104°F ± 5.4°F)

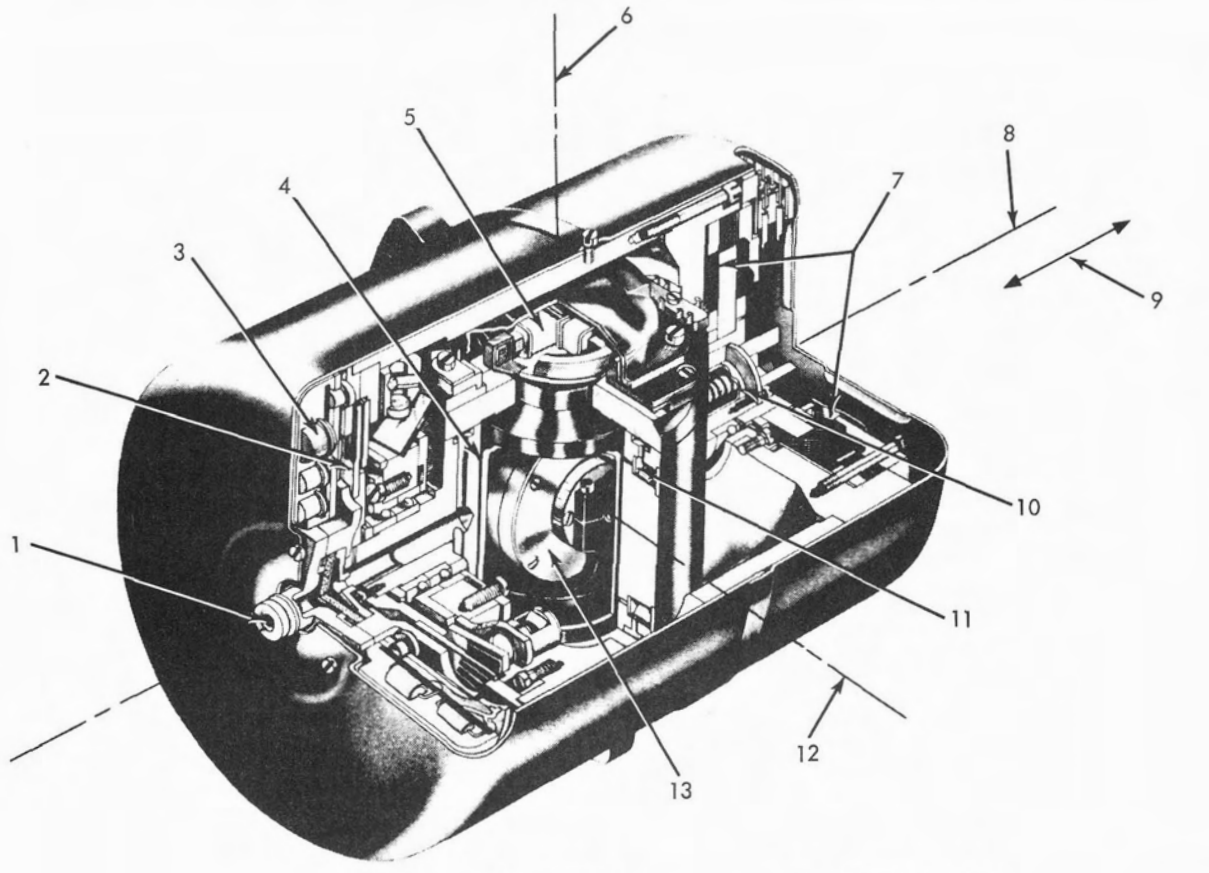


Figure 14.9-1 Cutaway View of a Pendulous Integrating Gyro Accelerometer

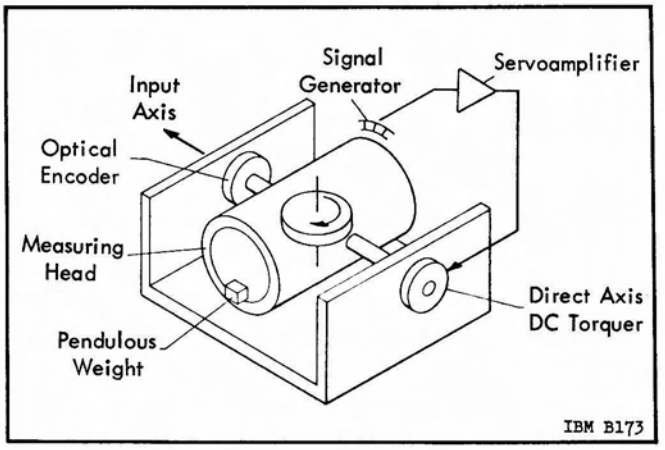


Figure 14.9-2 Pendulous Integrating Gyro Accelerometer Schematic

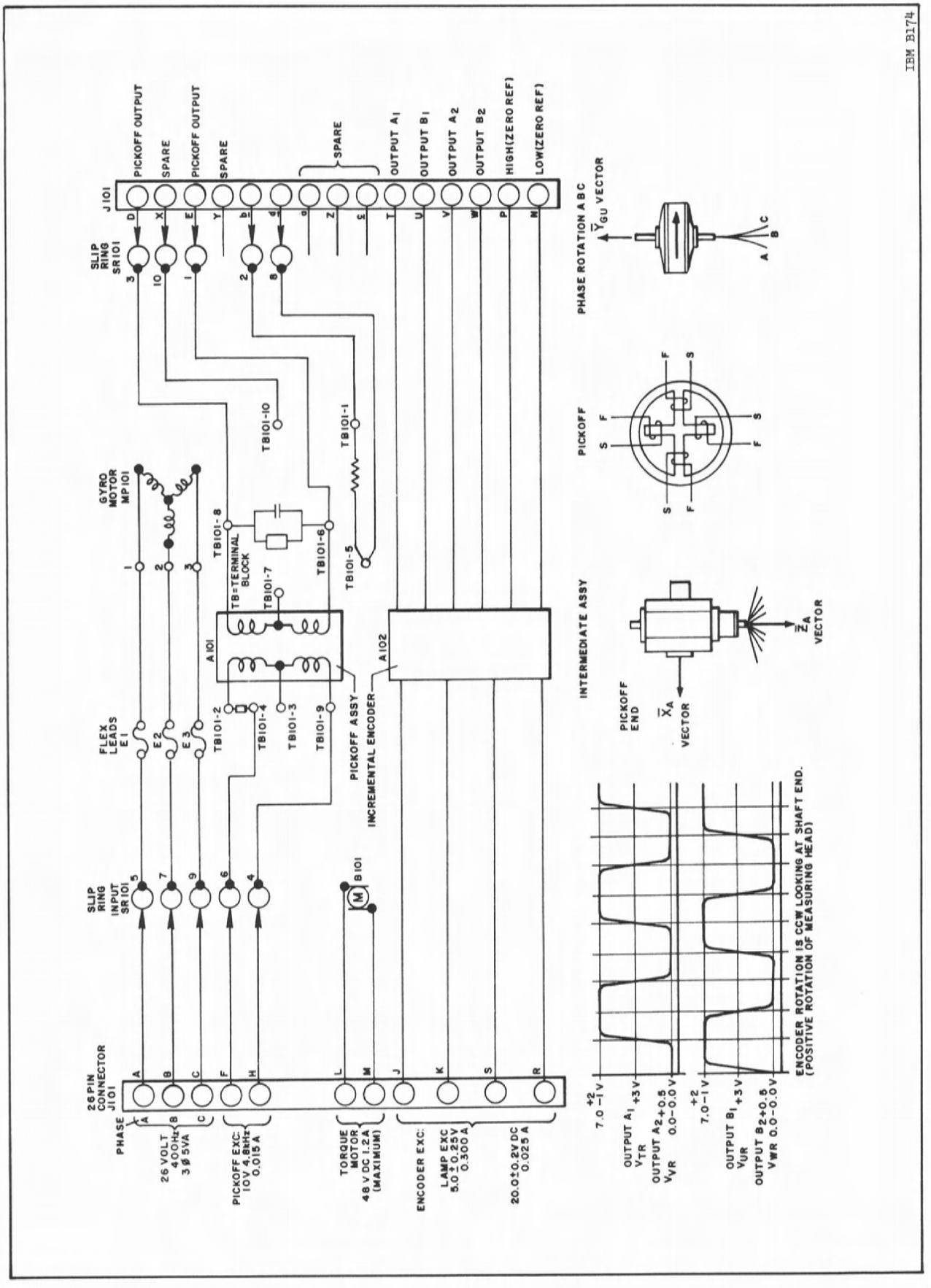


Figure 14.9-3 Electrical Schematic of an AB3-K8 Acceleometer

SECTION 14.10

POWER AND GAS REQUIREMENTS

The input power requirements and the expected heat dissipation of the system assemblies are shown in Figure 14.10-1. The input power figures show the normal (quiescent) requirements and the peak (maximum disturbing forces and g loading) requirements.

PLATFORM HEATERS

The Inertial Platform has 150 watts of resistive heating with the application of 115 volts, 60 hertz, or 400 hertz. The heaters are used to assist the Inertial Platform to reach its optimum operating temperature. Thermostats, located inside the platform, control the heaters and turn them off when the operating temperature is reached. The platform component heat dissipation maintains this temperature. The heaters will also be available if inflight environment dictates the necessity for heating.

Inflight platform temperature is controlled by circulating a constant-temperature fluid through ducts in the platform covers. The exterior of the Inertial Platform is painted with aluminum to provide an emissivity of approximately 0.4, thus providing a near-constant temperature radiating surface. Blowers will be utilized to circulate the internal gaseous nitrogen and maintain normal temperature gradients across the gimbals.

Gaseous nitrogen is supplied from a 0.056 cubic meter (two cubic feet) storage reservoir, pressurized to 20.7×10^6 N/m^2 (3000 psi), and regulated to 10.3×10^4 N/m^{2}d (15 psid) supply to the Inertial Platform. Temperature conditioning of the gas will be from the water-methanol IU coolant system. The Inertial Platform requires 1.4×10^{-3} cubic meters per minute (0.5 cubic feet per minute) of gaseous nitrogen.

Table 14.10-1 lists the power supply specifications.

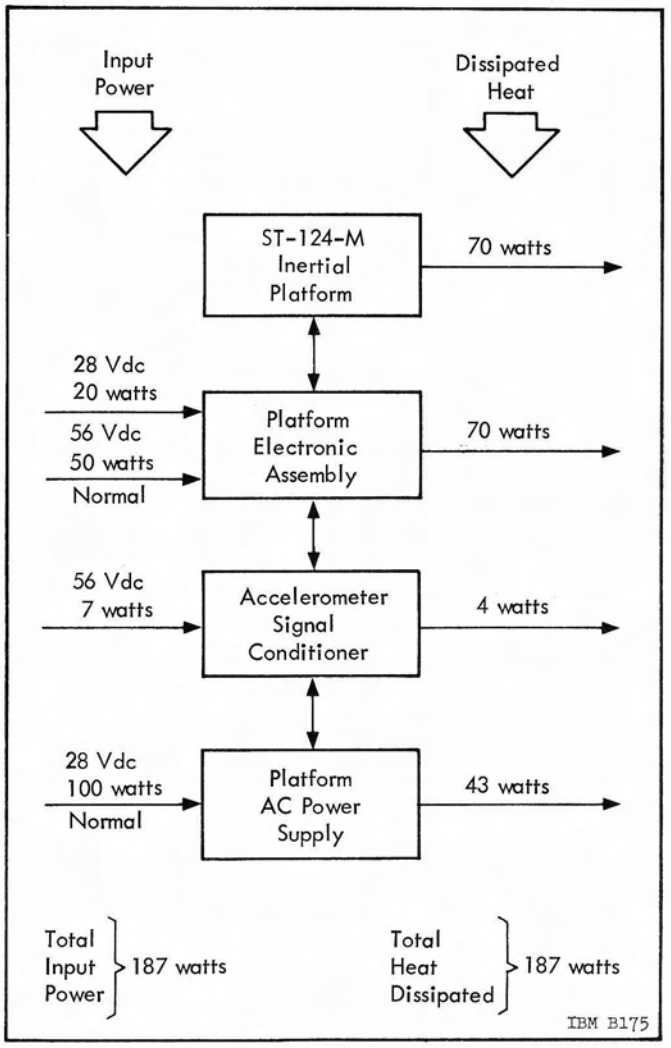


Figure 14.10-1 System Power Requirements and Heat Dissipation

Table 14.10-1 Power Supply Specifications

28 Vdc Supply	
Voltage regulation	± 2.0 Vdc
Ripple content	0.5 V
Normal current	9 A
Peak current	11 A
56 Vdc Supply	
Voltage regulation	± 3 V
Ripple content	0.25 V
Normal current	1.0 A
Peak current	6.0 A

CHAPTER 15

LAUNCH VEHICLE DATA ADAPTER

AND

LAUNCH VEHICLE DIGITAL COMPUTER

TABLE OF CONTENTS

SECTION 15.1

INTRODUCTION

The LVDA and the LVDC together contain the equipment and perform the functions which usually represent an electronic computer system. The LVDA is the input/output device of the LVDC. Any signal to or from the computer is routed through the LVDA. In addition, the LVDA serves as central equipment for interconnection and signal flow between the various systems in the Instrument Unit. The LVDA converts signals from digital to analog form and visa versa. The separation into LVDA and LVDC offers several advantages, the 2 boxes, each having approximately half the size and weight of a combined unit, can be mounted much easier in the vehicle. Also, flexibility is gained since functional or operational changes in the Saturn Astrionics System will essentially affect the LVDA only and can be implemented without changing the LVDC.

The LVDA and the LVDC are involved in the following main operations:

Prelaunch checkout
Navigation and guidance computations
Vehicle sequencing
Orbital checkout

The interconnections between LVDA, LVDC, and other Astrionics equipment is indicated in Figure 15.1-1.

The LVDC contains the logic circuits, the memory and the timing system required to perform arithmetic operations. The LVDA houses circuitry for temporary storage and conversion of data for communication with the LVDC and the power supplies for the LVDA and the LVDC.

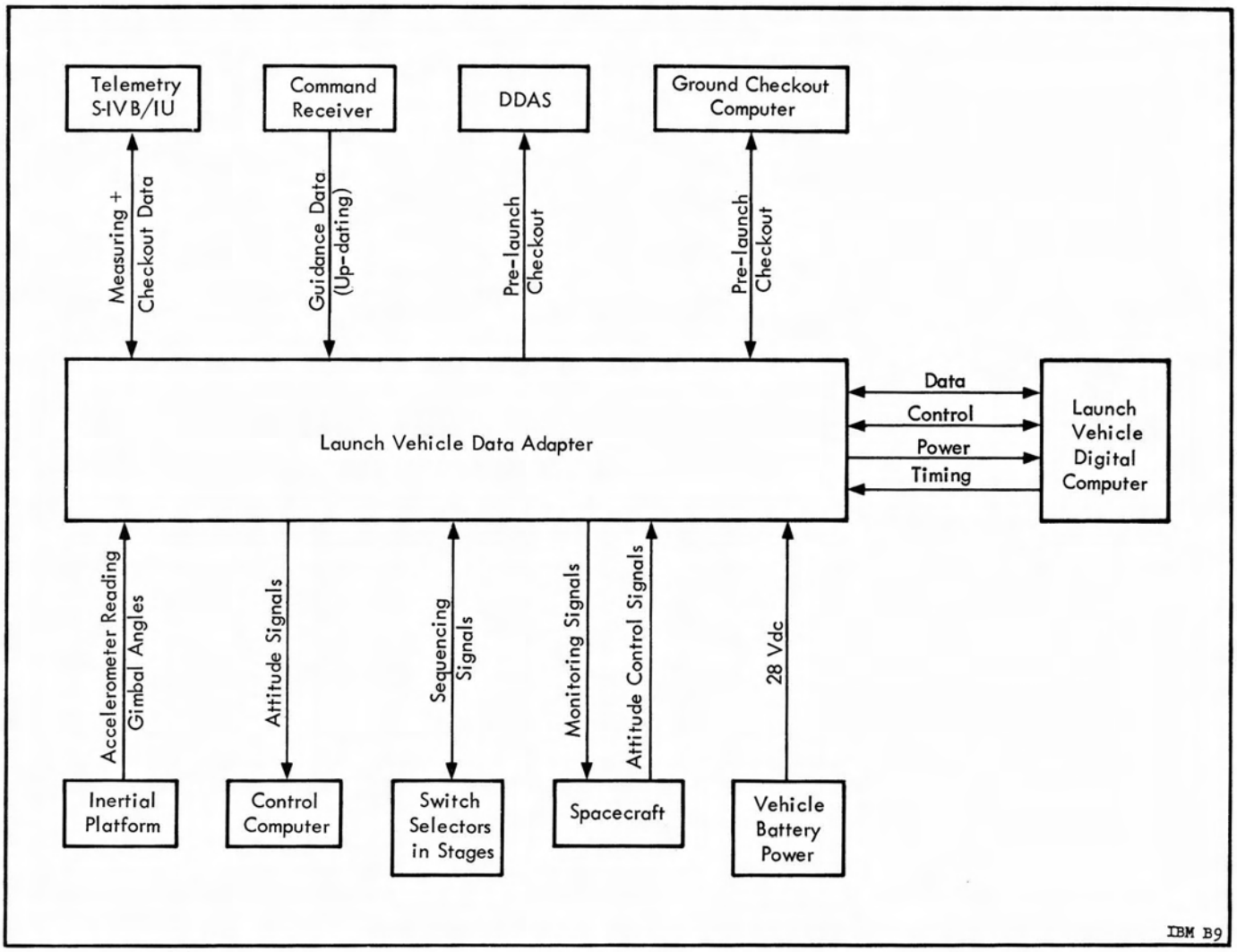


Figure 15.1-1 Connections Between Digital Computer, Data Adapter, and the Astrionics System

SECTION 15.2

PHYSICAL DESIGN

Microminiature packaging techniques are used as far as feasible in the LVDA and LVDC. Semiconductor chips are mounted on square ceramic wafers (side length 7.5 mm) on which interconnecting wiring and film resistors have been deposited by silk-screen printing and firing (Figure 15.2-1). The devices, called unit logic devices, are attached to multilayer interconnection boards using solder reflow techniques by infrared heating. Each multilayer interconnection board has a capacity of 35 unit logic devices. Two multilayer interconnection boards are bonded back-to-back to a supporting metal frame to form a logic page assembly (Figure 15.2-2). Multilayer interconnection boards and pages are joined by connectors to a central multilayer printed circuit board.

For applications requiring extreme accuracy or large drive current capability, circuit modules composed of conventional discrete components are utilized. These find greatest application in the LVDA, but are also used in the LVDC as memory drivers. The circuit modules are mounted on the interconnection boards previously mentioned. In volume, one circuit module page is equivalent to three unit logic device pages.

The magnesium-lithium frames of the LVDC and the LVDA are cooled by circulating a liquid through channels in the frame to remove heat generated by the electronic components. This cooling results in a low operating temperature for the electronic components and thus in a high reliability for the devices. The coolant is composed of 60 percent methanol and 40 percent water and is provided by the IU environmental control system.

An exploded view of the LVDA is shown in Figure 15.2-3 and the LVDC in Figure 15.2-4.

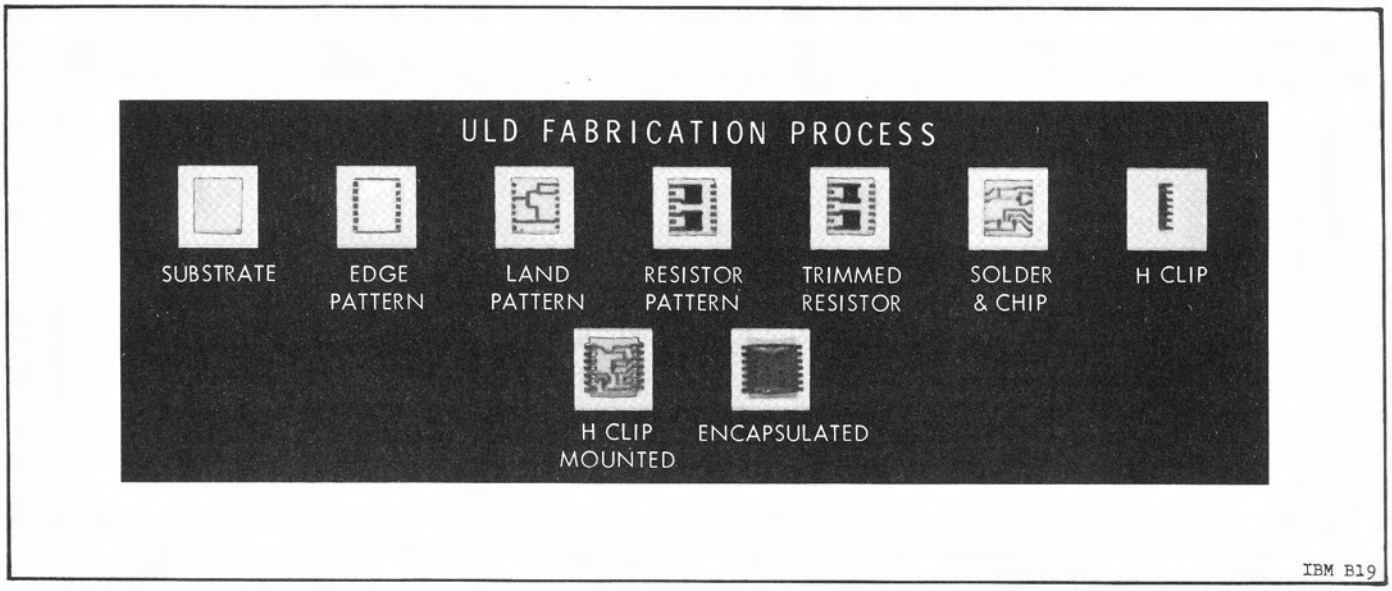


Figure 15.2-1 Unit Logic Device Buildup

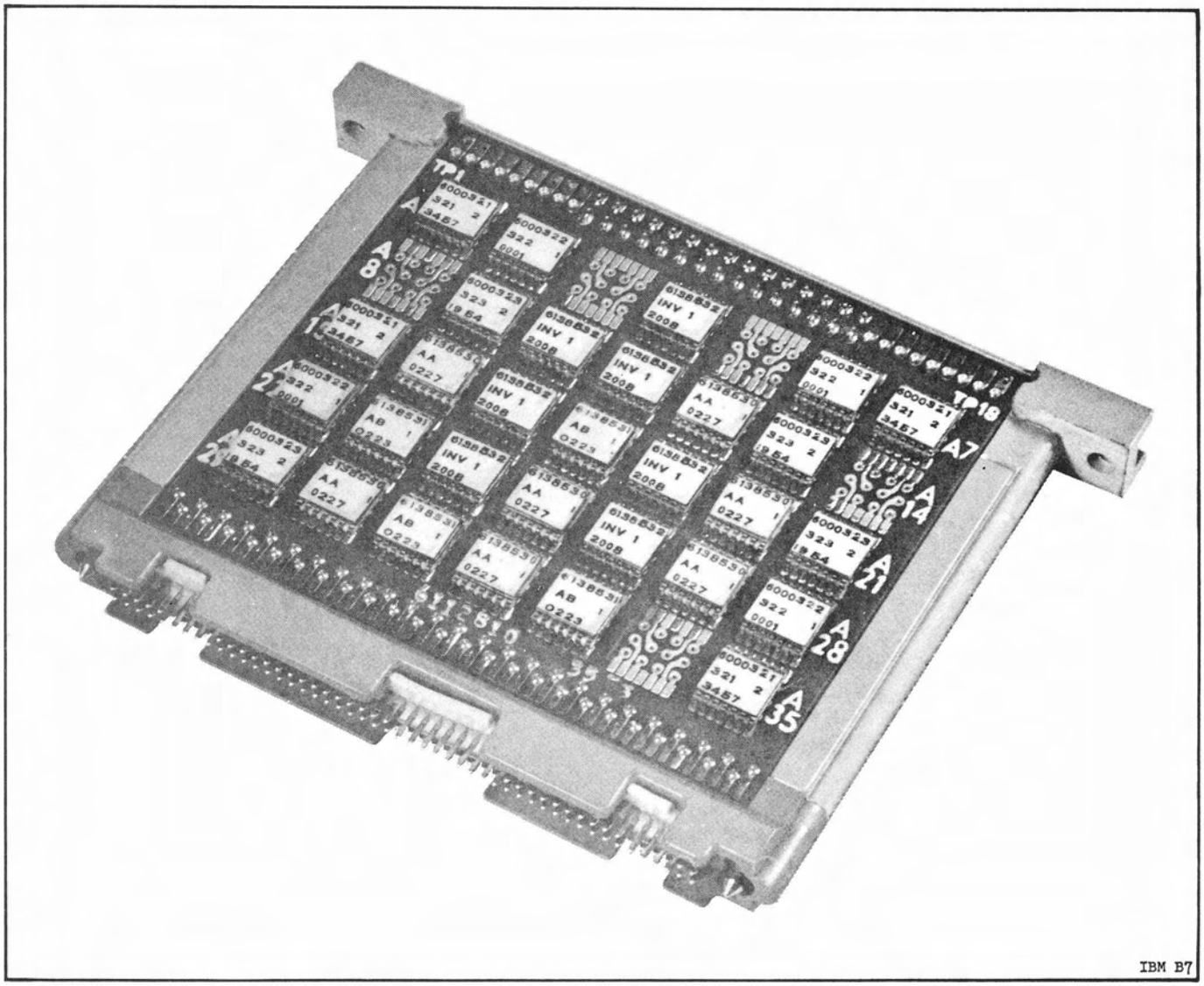


Figure 15. 2-2 Unit Logic Device Page Assembly

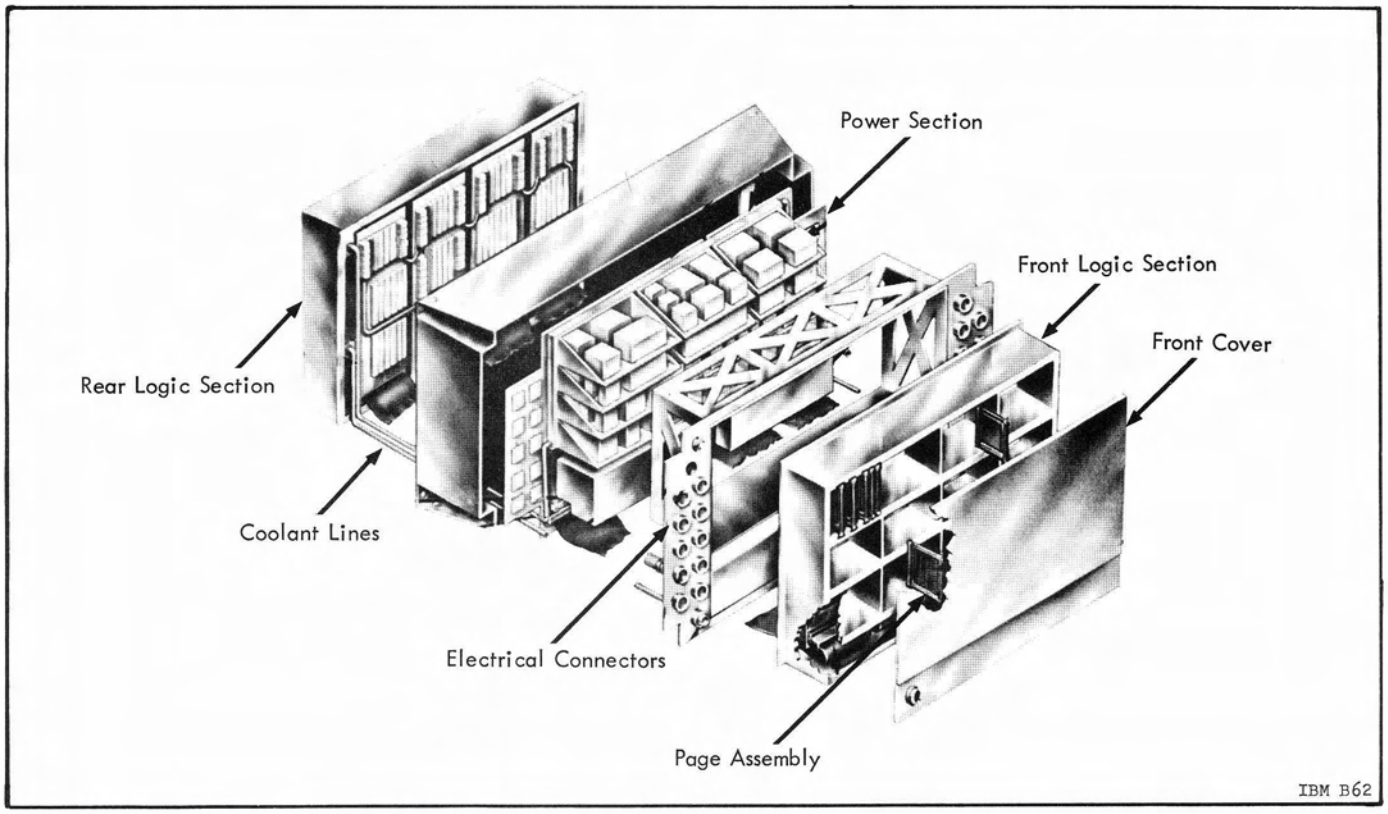


Figure 15.2-3 Exploded View of the Launch Vehicle Data Adapter

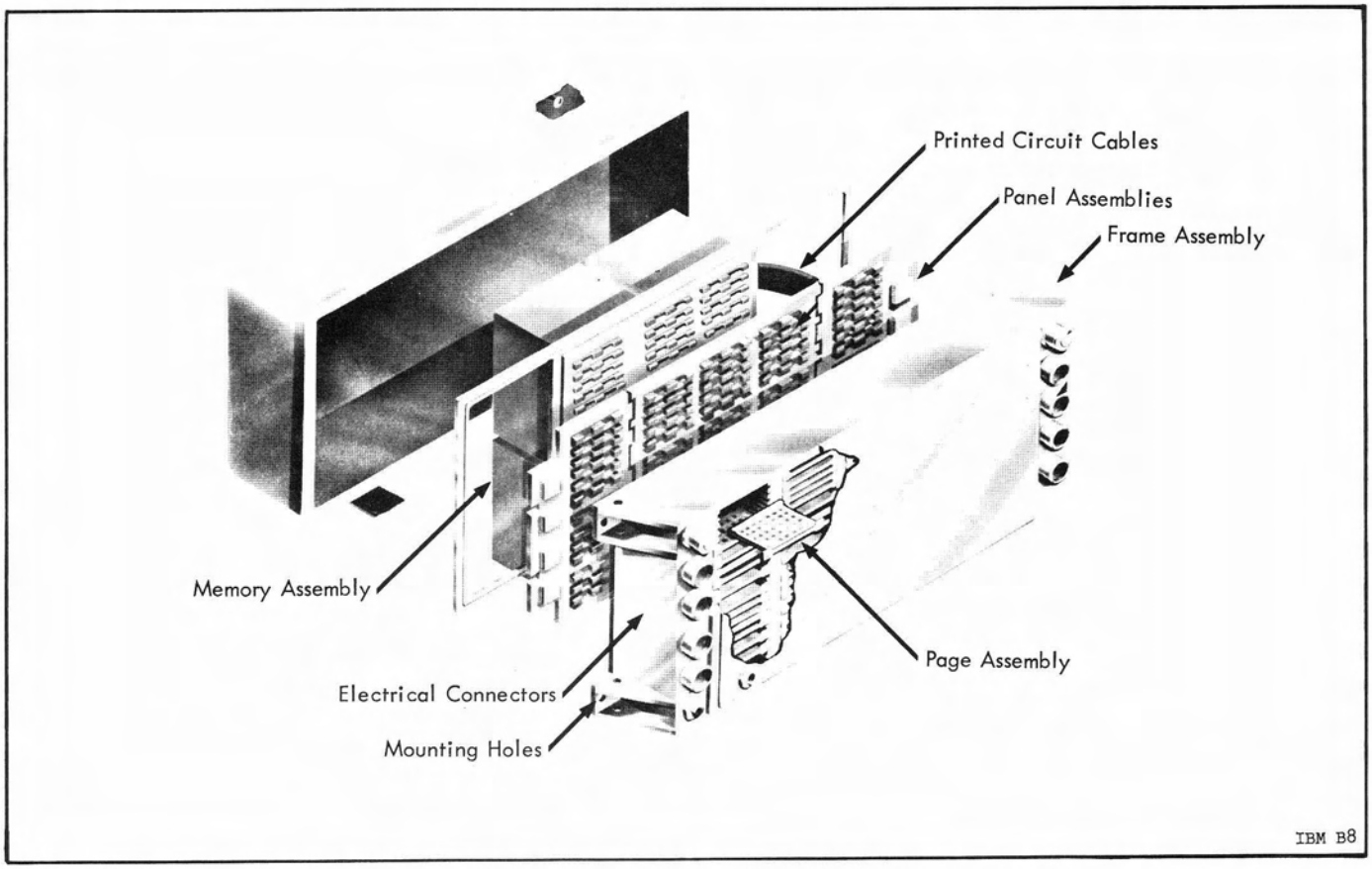


Figure 15.2-4 Exploded View of the Launch Vehicle Digital Computer

SECTION 15.3

RELIABILITY

Reliability of the LVDC is predicated on the use of triple modular redundancy in the central computer. The LVDC is divided into 7 modules (Refer to Table 15. 3-1) which are triplicated. Calculations and simulation based on Monte Carlo techniques indicate a reliability of 0. 996 for 250 hours (0. 999966 for a 6-hour mission) for the computer logic and memory using triple modular redundant and duplex techniques, respectively. This is compatible with the minimum design objective of a reliability of 0. 98 for a 250-hour mission for the combination of the LVDC and LVDA. For comparison, the equivalent simplex logic has a reliability figure of 0. 955 for 250 hours. Theoretically, the reliability of a duplex module exceeds that of triple redundant modules by a factor $\frac{2R - R^2}{3R^2 - 2R^3}$, but the difference is of a second order effect for values of R close to "one" and therefore negligible. Duplex redundancy, however, has limited application because of the problem of determining which one of the two units failed.

The triple modular redundant logic system of the LVDC uses three identical simplex logic channels (Figure 15. 3-1) and subdivides each channel into seven functional modules. The outputs from corresponding modules are voted upon in voter circuits before the signal is sent to the next modules. Figure 15. 3-2 shows typical modules and voters. The output of the voter circuit is equal to the majority of the inputs to the circuit. Thus, even if one of the three inputs is incorrect, the output to the next module will be correct.

An average of 13 output signals from each module are voted on. The voter circuit outputs may go to any of the other subdivided modules of the LVDC. This allows correct computations to be obtained, even with several malfunctions in the LVDC, provided two identical modules of a triple redundant set are not in error.

This method provides greater reliability than using three independent computers. If the outputs from three independent computers were compared, any malfunction in two of the computers would cause the computation to be in error.

Table 15. 3-1 TMR Computer Module Breakdown

Module Number	Module Name or Description
1	Computer Timing
2	Transfer Register
3	Arithmetic Unit
4	Multiply and Divide
5	Operation Code
6	Memory Address Register and Decoder
7	Memory Timing and Parity Check

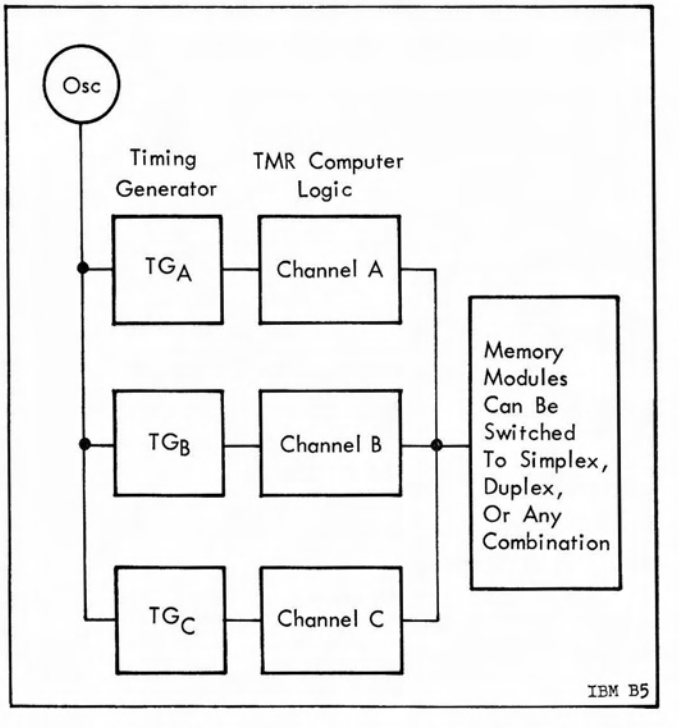


Figure 15. 3-1 Computer Redundancy Configuration

Disagreement detectors are used on module outputs as shown in Figure 15. 3-2 to indicate a failure in the system. Approximately 13 disagreement detectors are logically combined and fed to a register in the LVDA. These signals are then fed to the telemetry buffer register for monitoring either before launch or in flight.

The memory system has two individual memories which can be used in parallel (duplex) for increased reliability or completely independent (simplex) for increased capacity. In the duplex mode, information is read out of both memories from corresponding cores and by means of a selection network, just one memory output will be used. If the selected memory should contain an error (parity or timing), the information from the other memory would be used with the correct information being readback into both memories. Thus, the computer can correct memory errors.

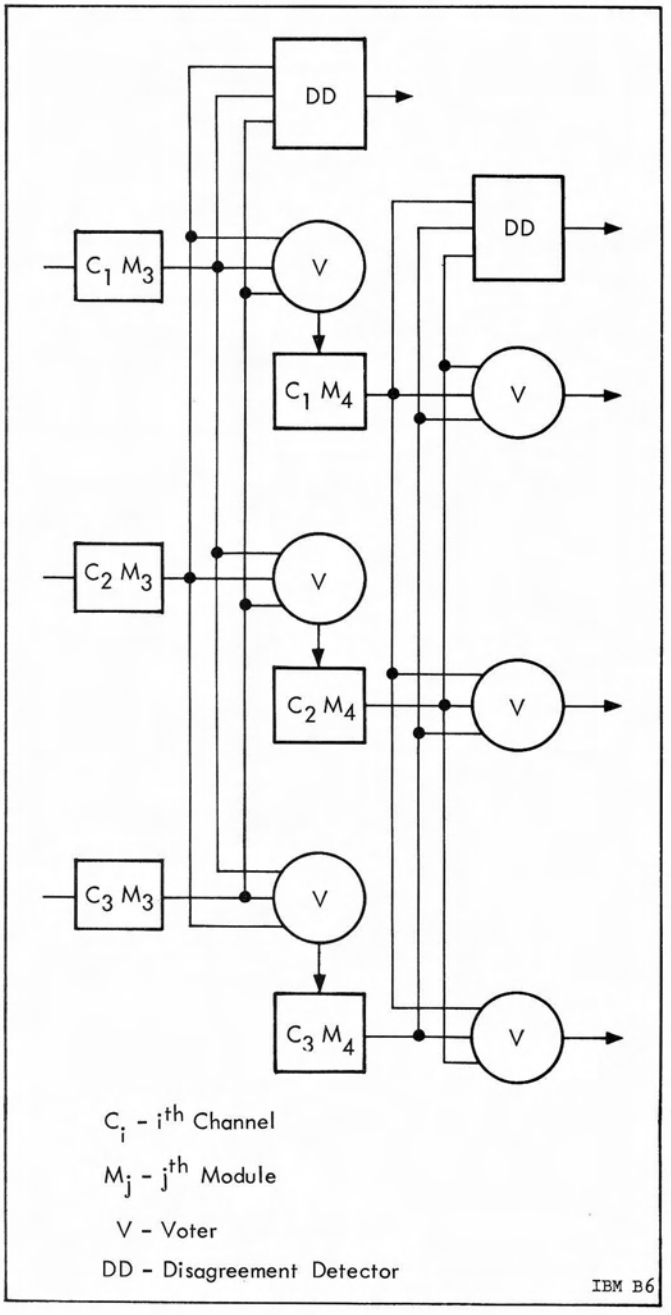


Figure 15. 3-2 Triple Modular Redundancy (TMR)

SECTION 15.4

DESCRIPTION OF THE LAUNCH VEHICLE DIGITAL COMPUTER

15.4.1 GENERAL CHARACTERISTICS

The Launch Vehicle Digital Computer is a general purpose computer which, under control of a stored program, processes data using fixed-point, two's complement arithmetic. Data is processed serially in two arithmetic sections which can, if desired, operate concurrently. Addition, subtraction, and logical extractions are performed in one arithmetic section while multiplication and division are performed in the other.

The principal storage device is a random access, ferrite-core memory with separate controls for data and instruction addressing. The memory can be operated in either a simplex or duplex mode. In duplex operation, memory modules are operated in pairs with the same data being stored in each module. Readout errors in one module are corrected by using data from its mate to restore the defective location. In simplex operation, each module contains different data which doubles the capacity of the memory. However, simplex operation decreases the reliability of the LVDC since the ability to correct readout errors is sacrificed. The memory operating mode is program controlled. Temporary storage is provided by static registers composed of latches and by shift registers composed of delay lines and latches.

LVDC ELEMENTS

The LVDC is composed of the following eight functional elements:

Timing	Program Control
Memory	Arithmetic
Memory Control	Multiply-Divide
Data Control	Voting

Figure 15.4-1 is a block diagram of the LVDC showing the major parts of each functional element (except the voting element) and how they are interconnected. The heavy lines on the diagram show major paths of information flow.

Timing Element. The timing element develops 3 levels of standard timing signals which synchronize and control logic operations in the remaining 7 elements. Direct outputs of the timing element are used in every functional element, except the memory element which generates its own timing signals.

Memory Element. The memory element and the memory control element operate together to store the programmed instructions and the constants and data required by the program. The memory element is composed of up to eight memory module assemblies, each of which contains a ferrite-core array and all the circuits necessary to transfer data to and from the module. The memory control element determines when a transfer will occur and selects both the direction of transfer and the memory location to be exercised. Buffer storage for data enroute between the memory and the central computer is also located in the memory control element.

In addition to controlling data transfers, the memory control element determines the mode (simplex or duplex) in which the memory will operate. In duplex operation, the memory modules are divided into 2 groups, effectively forming two separate memories with identical contents. The even numbered modules make up the "A" memory and the odd numbered modules make up the "B" memory. Each module in the "A" memory is paired with a module in the "B" memory which contains the same information. The memory control element selects both modules of a pair and provides separate buffer storage for each

memory. The 2 memories are operated simultaneously, but the LVDC uses information from only 1 memory. The memory select and error monitor circuit determines which memory will be used and changes the selection when an error is detected in the active memory. The memory select and error monitor circuit continuously samples the drive currents in each memory and checks the parity of each word transferred out of both memories. In simplex operation, each module contains different information, and only one module is selected at a time. The memory select and error monitor circuit then makes the memory selection follow the selected module so that the "B" memory is active when an odd numbered module is selected and the "A" memory is active when an even numbered module is selected. The ability to correct errors is sacrificed in simplex operations.

Data and constants are stored in the memory in 2 segments called syllables. Thus, the memory is described as being divided into syllables. One syllable of data is transferred to or from the memory at a time; consequently, two memory cycles are necessary to transfer a complete data word. Instructions are only half the length of data words and are stored one per syllable. The syllable selection for instructions is stored in the syllable select circuit of the memory control element. Timing signals determine whether the stored selection will be used or the selection will be sequenced to read both syllables of a data word.

When a memory operation is required, the memory control element provides a sync impulse to the memory element. Memory mode and module select circuits direct the impulse to two memory modules for duplex operation or one module for simplex. Once impulsed, each memory module generates all the timing signals and drive currents required to complete its cycle.

The memory clock drivers produce either read or store timing pulses, depending on a control signal from the memory timing and sync select circuits. The memory address decoders reduce the address of the desired memory location to selection signals for the X and Y memory address drivers of that location in each syllable of the memory.

The syllable select circuit determines which syllable will be used. Syllable and address selection signals are applied to all the modules in the memory. However, only the module (or modules for duplex) which receives a sync impulse will generate the memory clocks which cause the module to cycle. When the memory clocks occur, data is transferred in parallel between the memory buffer registers A and B and the selected memory location. All data entering or leaving the memory passes through the memory buffer registers enroute to or from the data control element.

Data Control Element. Data words and constants enter the transfer register from the memory in 2 syllables. Each syllable enters the transfer register in parallel and is then serialized and distributed to the arithmetic element, the multiply-divide element, or the LVDA. Some special constants are also distributed to the program control and memory control elements in serial form.

Data words which are bound for the memory enter the transfer register in serial form. The transfer register then divides them into syllables and forwards each syllable to the memory buffer registers in parallel. At the memory buffer registers, a parity bit is added to each syllable before it is stored in the memory. The parity counter monitors the number of "1's" entering the transfer register and assigns odd parity to the memory buffer registers by controlling the parity bit. Odd parity means that the total number of "1's" in a syllable is odd.

Another item which enters the transfer register serially is the contents of the instruction counter. The instruction counter controls the normal sequencing of the program through the memory. Just before a new instruction is required, the contents of the instruction counter are shifted into the transfer register and transferred in parallel to the address register in the program control element. The address register then selects the memory location of the new instruction.

When the new instruction is read, it is transferred from the memory buffer registers into the transfer register. The instruction is then separated into an operation code and an operand address; the 2 parts are transferred in parallel to the program control element. The operation code is loaded into the operation code register and the operand address into the address register. The operand address of some instructions constitutes a special constant which, in addition to the parallel transfer, is shifted out of the transfer register in serial form.

Program Control Element. The program control element stores and decodes the programmed instructions and in addition, controls sequencing the

program through the memory. The operation code register and the address register store their respective parts of the instructions. Outputs of the operation code register, and those of the operation decoders, control the arithmetic and multiply-divide elements, the data and memory control elements, and parts of the program control element to perform the commanded operations.

The address register selects the memory location of the data to be used in the commanded operation. When the operation is complete, the address register is reloaded with the contents of the instruction counter to address the next instruction. The address register is augmented by the data module register and the instruction module register (located in the memory control element) and by the data sector register and the instruction sector register in the program control element.

The module and sector registers preselect an area of the memory within which the program must operate. As implied by the names of the registers, 2 selections are made, one for data and one for instructions (the same area may be selected for both).

The address register then selects individual locations within the preselected areas from which data and instructions will be read. Timing signals discriminate between instruction and data addressing. The contents of the module and sector registers are changed upon command of the program.

It was noted previously that the program control element controls sequencing the program through the memory. Actually, the program controls its own sequencing through the use of instructions which command the program control element to change the contents of the module and sector registers (discussed in the preceding paragraph) and the instruction counter.

The instruction counter stores the address of the next instruction to be operated. Each time the LVDC performs an instruction, the instruction address is incremented by one to develop the address of the following instruction. In this manner, the program steps sequentially through the area of memory selected by the instruction module register and the instruction sector register.

The sequential stepping continues until the program issues an instruction to alter the sequence or select a different area of the memory to read instructions from. Area selection is changed by shifting a "HOP constant" out of the transfer register which reloads the instruction counter to select the starting location of the next instruction sequence. The instruction counter then begins stepping sequentially through the newly selected memory area beginning at the specified starting point.

The instruction counter can also be reloaded without affecting the module and sector registers. This feature permits repeating short program loops and enables the LVDC to make logical choices. When commanded, the LVDC can examine the contents of the accumulator register for certain conditions and alter the program sequence if the condition exists. If the condition is not met, sequential stepping continues.

The program control element also contains two other circuits which can alter the normal program sequencing, the start-stop control and the interrupt control circuits. The start-stop control circuit provides the means to externally control starting and stopping the LVDC and to single-step through its program one instruction at a time. Application of a HALTV signal results in clearing certain registers to an initial condition and directs the LVDC to the first instruction of its program. During power application, the HALTV signal remains ON until power is fully applied to prevent spurious instructions from being operated. A CSTN signal is manipulated by the test equipment to step through the program one instruction at a time, on command.

The interrupt control circuit enables external equipment to break off normal sequencing of the program and direct it to process data of a higher priority. The interrupt control circuit allows the instruction in progress at the moment of the interruption to finish, then forces execution of a command to reload the instruction counter and the module and sector registers.

The first few instructions of the new program sequence store the contents of the important registers in order to preserve the conditions existing in the LVDC at the moment of interruption. Once the priority data has been processed, the LVDC can restore these conditions and resume operation where it left off. The very first item to be stored must be a HOP constant defining the location at which the interrupt occurred. This constant is produced by the HOP constant serializer and is used to redirect the program to the point of interruption.

Arithmetic and Multiply-Divide Elements. The arithmetic and multiply-divide elements encompass the machine's total computing ability. The arithmetic element performs addition, subtraction, shifts, and logical extractions. The multiply-divide element

performs the iterative processes of multiplication and division. The 2 elements are independent and can, if desired, be operated concurrently.

Once a multiply or divide operation has been started, it runs automatically to completion and the next few instructions of the program are operated during its progress. During this time the arithmetic element is available for concurrent use. There is, however, a program option for multiplication which stops the program until the product of the multiplication is available. When using this option the product is placed in both the product-quotient register and in the accumulator register.

The accumulator register in the arithmetic element provides one of the operands for all the arithmetic instructions and the memory provides the other. For multiplication and division, the accumulator contents and the operand from memory are simply transferred into shift registers in the multiply-divide element for temporary storage during the iterative process. The remaining arithmetic operations combine the 2 operands in the add-subtract logic and place the result in the accumulator register. The result can then be sensed to control logical decisions or it can be transferred to the memory, the multiply-divide element, or the LVDA. The result remains unchanged in the accumulator register after sensing or transfer.

The multiply-divide logic senses the operands each iteration and forms a partial product or quotient. The final result is circulated in the product-quotient register until another multiply or divide operation is initiated, or until the LVDC is commanded to store data in the product-quotient register. Unlike the accumulator register which provides data to several destinations, the product-quotient register has only one outlet for its contents. All data leaving the product-quotient register must pass through the accumulator register. The product-quotient register contents are accessible to all arithmetic instructions except multiply and divide.

Voting Element. The voting element comprises the voters and disagreement detectors located between modules of the LVDC and between the central computer and the memory. The voters resolve differences between the outputs of triple redundant circuits before the outputs are passed on to succeeding circuits. Thus the LVDC can sustain multiple failures (but not identical failures occurring simultaneously) and still function reliably. The disagreement detectors monitor inputs to the voters and provide outputs which indicate when a failure has occurred. Since failures are self-correcting, there are no failure indications for non-catastrophic malfunctions in the computer logic except those from the disagreement detectors. The voting element is not shown in Figure 15.4-1 because it is widely disseminated through and between the functional elements.

TYPICAL OPERATION

Assume that the LVDC program has been initiated and is running smoothly. The area of the memory in which the program will operate has been selected and instructions are coming from syllable zero. The memory is operating in the duplex mode with memory "A" selected. For descriptive purposes, typical operation begins with reading an instruction from the memory. The address of the instruction is shifted out of the instruction counter and applied to the transfer register and the add-subtract logic in the arithmetic element. The add-subtract logic increments the count by one and reinserts it into the accumulator register where it is circulated. The instruction address is shifted into the transfer register and then transferred in parallel to the address register. The next events occur in the memory control element.

Timing inputs indicate to the syllable select circuit and the memory timing and sync select circuit that an instruction is due to be read. The syllable select circuit selects syllable zero (the stored syllable selection for instructions) in all memory modules. The memory timing and sync select circuit performs 3 functions at this time. It conditions the memory address decoders to decode the contents of the instruction sector register rather than the data sector register; it conditions the memory clock drivers of all memory modules to produce read pulses; and it delivers a sync impulse to the memory mode and module select circuit. The memory mode and module select circuit routes the sync impulse to the memory clock drivers of the two (duplex operation) memory modules selected by the instruction module register.

Upon being impulsed, the memory clock drivers produce read timing pulses which enable the selected X and Y drivers to transfer the instruction out of the addressed memory location. The memory sense amplifiers transmit the instruction to the memory buffer registers. The memory buffer registers store the instruction for parity checking and to enable the inhibit drivers during the restore memory cycle (explained later). If the parity of either memory buffer register is incorrect or if a drive current

failure occurred during the read operation, the memory select and error monitor circuit provides an error indication to the LVDA. Upon sensing an error, the memory select and error monitor circuit also places both sets of inhibit drivers under control of the memory buffer register containing correct information, and if the error is in the selected memory, changes the memory selection. The instruction is then transferred from the selected memory buffer register to the transfer register.

Reading a ferrite-core memory destroys the information in the memory. Consequently, a read operation must always be followed by a store (or restore) operation to preserve the contents of the memory. The restore operation is accomplished after the instruction has been transferred to the transfer register. The memory timing and sync select circuit changes the conditioning level to the memory clock drivers so that they produce store timing pulses, then delivers a second sync impulse to the memory mode and module select circuit. There have been no changes in address or memory module selection, therefore the same memory location is exercised again. However, on this memory cycle, data is transferred from the memory buffer registers to the memory through the inhibit drivers.

Almost immediately upon entering the transfer register, the instruction is separated into an operation code and an operand address. The operation code defines what operation will be performed, and the operand address gives the location in memory of the data to be used in the operation. The operation code is transferred in parallel to the operation code register and the operand address to the address register. The remainder of the operation is dependent upon the code transferred to the operation code register. The code can specify any of three general types of operations: (1) those which require data from memory, (2) those which place data into the memory, and (3) those which do not use the memory.

Assume first that the operation code requires data to be read from the memory. The syllable select circuit selects syllable zero, the first syllable of the data word. The memory timing and sync select circuit conditions the memory address decoders to combine and decode the contents of the address register and the data sector register; it then initiates a read cycle in the memory which transfers the first half of the data word to the memory buffer registers. While in the memory buffer registers, the half-data word is parity checked, then transferred to the transfer register and restored in the memory. The transfer register serializes the data by shifting it to the TRS output latch. The TRS output makes the data available to the arithmetic and multiply-divide elements, the program and memory control elements, and the LVDA. Outputs from the operation code register and the operation decoders determine which element will accept it and how it will be used.

As the first half of the data word nears the end of the transfer register, the syllable select circuit selects syllable 1 and the memory timing and sync select circuit initiates another read cycle in the memory. This read cycle transfers the second half of the data word into the memory buffer registers where it is parity checked. Then, just in time to fall in behind the last bit of the first half of the data word, the second half of the data word is transferred into the transfer register. The transfer register continues shifting and the two halves of the data word appear as a continuous serial output on the TRS line.

To obtain the result of a multiply or divide operation, the operand address specifies the product-quotient register. When the product-quotient register is addressed, the memory is inhibited and the product or quotient is shifted directly into the accumulator register without passing through the transfer register.

When providing a data output, the transfer register is synchronized with the accumulator register. Thus, the output of the transfer register and the contents of the accumulator register can be combined bit-for-bit in the add-subtract logic. The results of these operations are placed in the accumulator register for recirculation. As the last bit of the accumulator contents emerges from the accumulator register, timing signals end the arithmetic processes in the add-subtract logic and the contents of the instruction counter begin to emerge from the accumulator register. The add-subtract logic increments the instruction count by one and reinserts it in the accumulator register immediately behind the result of the arithmetic operation. Simultaneously, the instruction count is shifted into the transfer register to address the next instruction.

When the operation code specifies that data is to be transferred into the memory, the basic operations are reversed. Instead of transferring 2 syllables of data to the transfer register which serializes them into a continuous unit, a continuous unit of serial data is shifted into the transfer register which divides it into syllables. The syllables are then transferred to the memory in parallel. Shortly after the instruction is loaded into the operation code and ad-

dress registers the data word to be stored begins to emerge from the accumulator register. Outputs from the operation code register and the operation decoders condition the transfer register to shift in step with the accumulator register and accept its output. As the data word enters the first position of the transfer register, the parity counter monitors the number of "1's" it contains. At this point, the focus moves to the memory control element.

Timing signals indicate to the memory control element that a data word is due to be transferred to or from the memory. The operation code specifies that data is going to the memory by causing the memory timing and sync select circuit to switch the read/store signal to store. The syllable select circuit selects syllable zero as the first syllable to be transferred. The memory timing and sync select circuit conditions the memory address decoders to enable the X and Y drivers of the memory location addressed by the address register and the data sector register. Just before the last bits of the syllable enter the transfer register, the memory timing and sync select circuit delivers a sync impulse to the memory mode and module select circuit. The memory mode and module select circuit routes the impulse to the memory clock drivers of the selected data modules. The memory clock drivers produce read timing pulses, but the data transferred out of the memory is not sensed because a store, not read, operation has been specified. Since reading the memory is a destructive process, the addressed memory location is left cleared.

Simultaneous with clearing the memory location, the last bit of the syllable enters the transfer register and the syllable is transferred to the memory buffer registers. The transfer register continues shifting and the second syllable of data starts to file into the transfer register. At the memory buffer registers, a "parity bit" is added to the syllable entering the memory. The parity bit is controlled by the parity count circuit so that each memory buffer register contains an odd number of "1's". (Bear in mind that the parity count circuit monitors the number of "1's" in the syllable as it enters the transfer register.) The memory timing and sync select circuit then impulses the memory again, and the first syllable of data enters the memory through the inhibit drivers. The second syllable of data enters the memory in the same manner as the first and like the first includes its own parity bit.

It was noted previously that data could be stored in the product-quotient register. When this operation is specified, the memory is inhibited and the accumulator contents are shifted directly into the product-quotient register as one intact unit.

Operations which do not use the memory either shift the contents of the accumulator register or use the operand address as a constant for controlling the program. Shifting the contents of the accumulator register is accomplished by shortening or lengthening its circulation loop. Before the first bits of the accumulator contents begin to emerge, outputs from the operation code register and the operation decoders, along with control bits from the address register, alter the recirculation path of the accumulator register to effect the shift. When the last bit has been shifted, timing signals restore the loop to normal to prevent shifting the contents of the instruction counter. The instruction counter is then incremented and shifted into the transfer register to address the next instruction.

Among the operations which do not use the memory are those which make logical decisions based on the contents of the accumulator register. As noted previously, logical decisions are made by altering the contents of the instruction counter if a specified condition exists in the accumulator register. If the condition exists, the operand address of the instruction replaces the existing contents of the instruction counter and the next instruction begins the new sequence. Logical decisions are implemented by continuously sampling the accumulator contents part way through the register for the conditions upon which decisions are based. Thus, when a logical decision is initiated, most of the accumulator contents have already been sampled and the computer need not wait until the complete contents emerge from the register to make the decision. The contents of the instruction counter immediately follow the accumulator contents in the accumulator register. Consequently, when the last data bit has been sensed and the decision made, the contents of the instruction counter are still only part way through the accumulator register. If the condition is met, the accumulator register is broken just behind the last bit of the accumulator contents and the operand address is shifted into the accumulator register from the transfer register, replacing the existing instruction count.

Since the memory is not being used, the transfer register is not needed to distribute data from it, and therefore is not cleared after the instruction is distributed to the program control element.

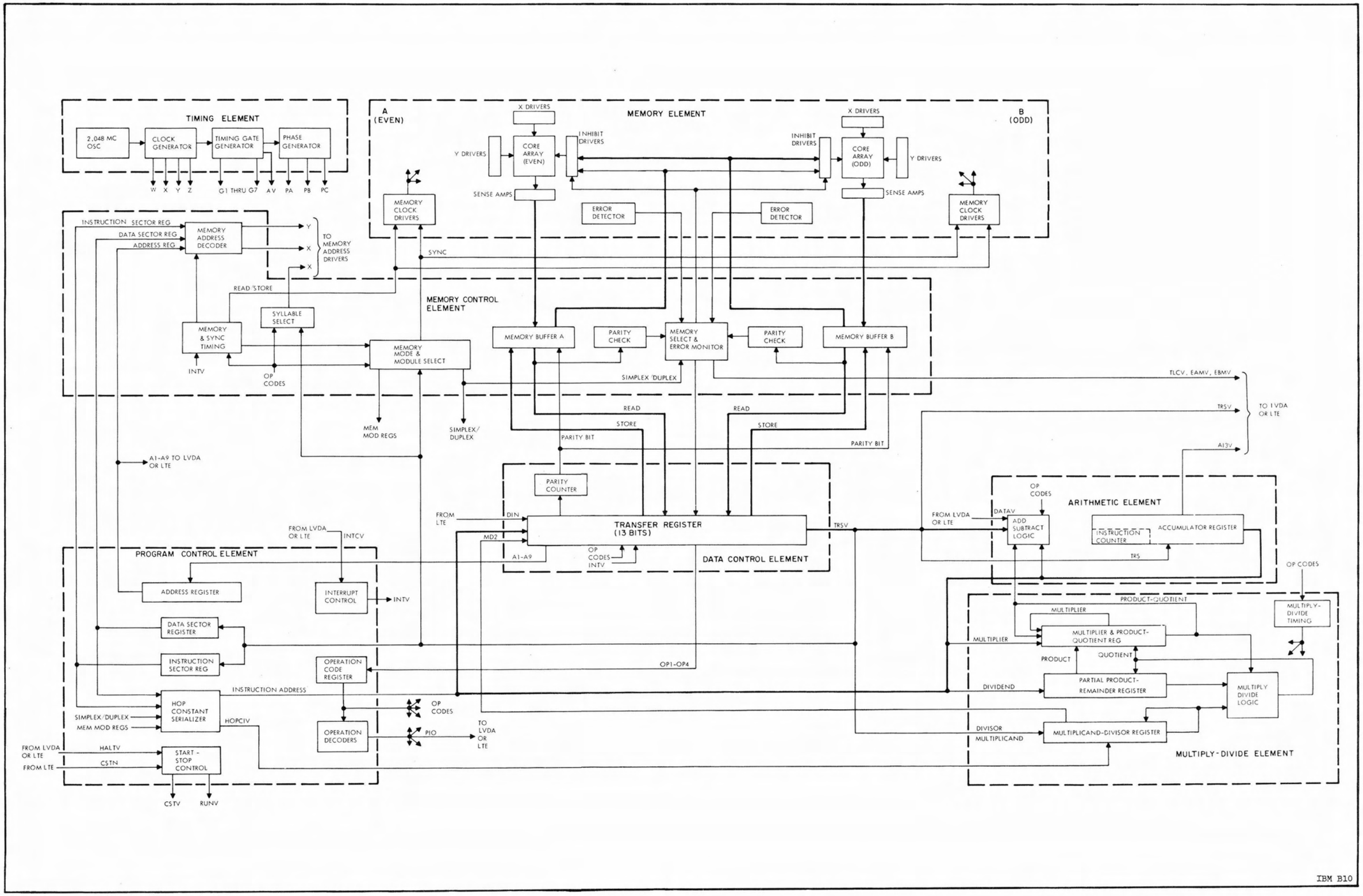


Figure 15.4-1 Computer Functional Block Diagram

If the condition is not met, the accumulator register is not broken and the existing contents of the instruction counter are retained to address the next instruction.

Data are processed by using two's complement arithmetic. Two's complement arithmetic eliminates the necessity for a recomplementation cycle when using sign plus magnitude arithmetic. Special algorithms have been developed and implemented for multiplication and division of two's complement numbers. Multiplication is done 4 bits at a time and division 2 bits at a time.

The LVDC is interconnected with the LVDA which contains input/output conversion electronics and power supplies for the LVDC. Salient characteristics of the triple modular redundant LVDC are summarized in Table 15.4-1.

Table 15.4-1 Launch Vehicle TMR Computer Characteristics

Characteristic	Description
Type	Stored program, general purpose, serial, fixed-point, binary
Clock	2.048 MHz clock, 4 clocks per bit, 512 kilobits per second
Speed	Add-subtract and multiply-divide simultaneously
Add time, accuracy	82 us, 26 bits
Multiply time, accuracy	328 us, 24 bits
Mult-hold time, accuracy	410 us, 24 bits
Divide time, accuracy	656 us, 24 bits
Memory	Random access toroidal core
Storage Capacity	Up to a maximum of 32,768 twenty eight-bit words in 4096-word modules
Word Length	Memory word 28 bits: 2 instructions may be stored in one memory word
Data	26 bits plus 2 parity bits
Instruction	13 bits plus 1 parity bit
Input/Output	External: computer-programmed I/O control: external interrupt provided
Component Count*	40,800 silicon semiconductors and film resistors (cermet). Up to 917,504 toroid cores
Reliability*	0.996 probability of success for 250 hours using TMR logic and duplex memory modules
Packaging	Structure constructed of magnesium-lithium material, designed to house 73 electronic pages and 8 memory modules
Weight*	30 kg (75.0 lbs) (4 memory modules)
Volume*	0.07 meters^3 (2.4 feet^3)
Power*	150.0 watts (4 memory modules)

*Figures given here are estimated values

In the following paragraphs some details about the computer circuits and their operation will be described.

15.4.2 WORD ORGANIZATION

The LVDC uses a 28-bit word consisting of two 14-bit syllables. Each syllable includes 13 data bits and 1 parity bit. Each syllable is stored separately in the memory. The parity bits are used only to check the accuracy of transfers to and from the memory which leaves a data word 26 bits in length (Figure 15.4-2).

The use of the data word is at the discretion of the programmer. Each of the 26 bits may be used as an indicator to show the presence or absence of some condition, or the word may be used as a binary number for arithmetic computations. Binary numbers are represented by a sign bit and 25 magnitude bits; negative numbers are shown in two's complement form.

This text uses 2 methods for designating bit positions in the data word. Where the word represents a binary number, the bits are designated sign and 1 through 25, proceeding toward the least significant digit. When used in this context, bits 1 through 25 are called "magnitude bits". The bits are designated 1 through 26 when not referencing the data word as a binary number; bit 1 corresponds to sign and bit 26 corresponds to bit 25 of the numeric designations.

The computer word is also used to store the instructions of the computer program. Instructions are 13 bits in length with one instruction stored in each syllable of the computer word. An instruction consists of a 4-bit operation code (OP1-OP4) and a 9-bit address (A9, A1-A8). Figure 15.4-2 shows how the instructions are placed in the computer words.

15.4.3 TIMING

The basic unit of computer timing is called the "computer cycle". The duration of an LVDC cycle is approximately 82 microseconds; this is the time required for the LVDC to read, decode and operate its basic instructions. The signals which define a computer cycle originate in the phase generator. A computer cycle corresponds to a full cycle of the phase generator which produces three equal-length timing signals called phase A, phase B, and phase C. Thus, a computer cycle is defined by three "phase times".

The phase generator separates the computer cycle into "instruction time" and "operation time". As the names imply, instruction time is the period in which an instruction is read and decoded, and operation time is the period in which the operation commanded by the instruction is performed. Generally, instruction time occurs during phase A and operation time during phase times B and C.

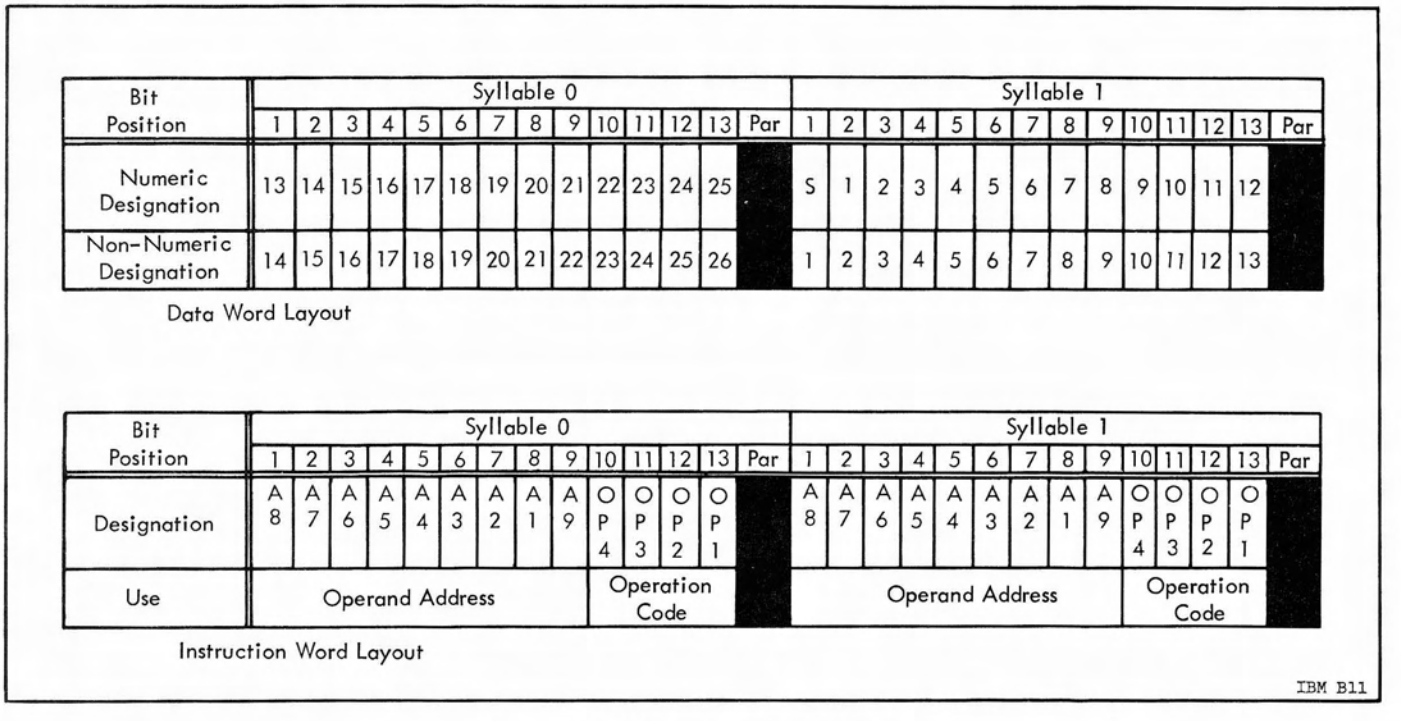


Figure 15.4-2 Word Organization

Notice the correlation between the organization of timing and word layout. The LVDC cycle is defined by 3 phase times and involves 3 syllables of information: 1 syllable for an instruction and 2 syllables of data for an operand. The correlation also extends downward one stop. A syllable consists of 14 bits (13 data and 1 parity) and each phase time is divided into 14 equal segments called "bit times". A bit time is the time each bit of data is stored in one position of a serial storage device before moving on to the next.

To facilitate several logic operations during each bit time, the bit times are subdivided into four equal parts called clocks. The clocks are identified by the letters W, X, Y, and Z and occur in alphabetical sequence. Figure 15.4-3 shows the relationships of the various levels of timing and gives the time duration of each level. Timing is given by a letter-number-letter abbreviation of the phase time, bit time and clock time in descending order of time duration. For example, an event resulting from the W clock of bit-time 11 during phase A is described as happening at A-11-W time. If one level of timing does not apply or has been previously established, that level may be dropped from the abbreviation; i. e., a circuit which operates independent of phase timing may produce an output at every 6-Z time.

The timing element contains all the circuits which generate timing signals for the operation of computer logic. Basically, the timing element consists of an oscillator and 3 cascaded frequency dividers: the clock generator (which includes the oscillator), the timing-gate generator, and the phase generator. The oscillator produces the basic timing signal, from which all other timing signals are derived. The clock generator divides its oscillator output frequency by four to produce a sequence of 4 clock signals which recur each bit time. The clock signals divide each bit time into 4 parts, enabling several logic operations to be performed on each serial data bit. The signals used to identify bit times are developed by the timing-gate generator.

The timing-gate generator divides the clock frequency by seven, producing seven timing gates which, with their complements, can be combined to identify 14 bit times. The phase generator then divides the output frequency of the timing-gate generator by three to define the 3 phases of the LVDC operation cycle. Several additional signals, embodying various combinations of phase, timing gate, and clock signals are generated by special timing circuits.

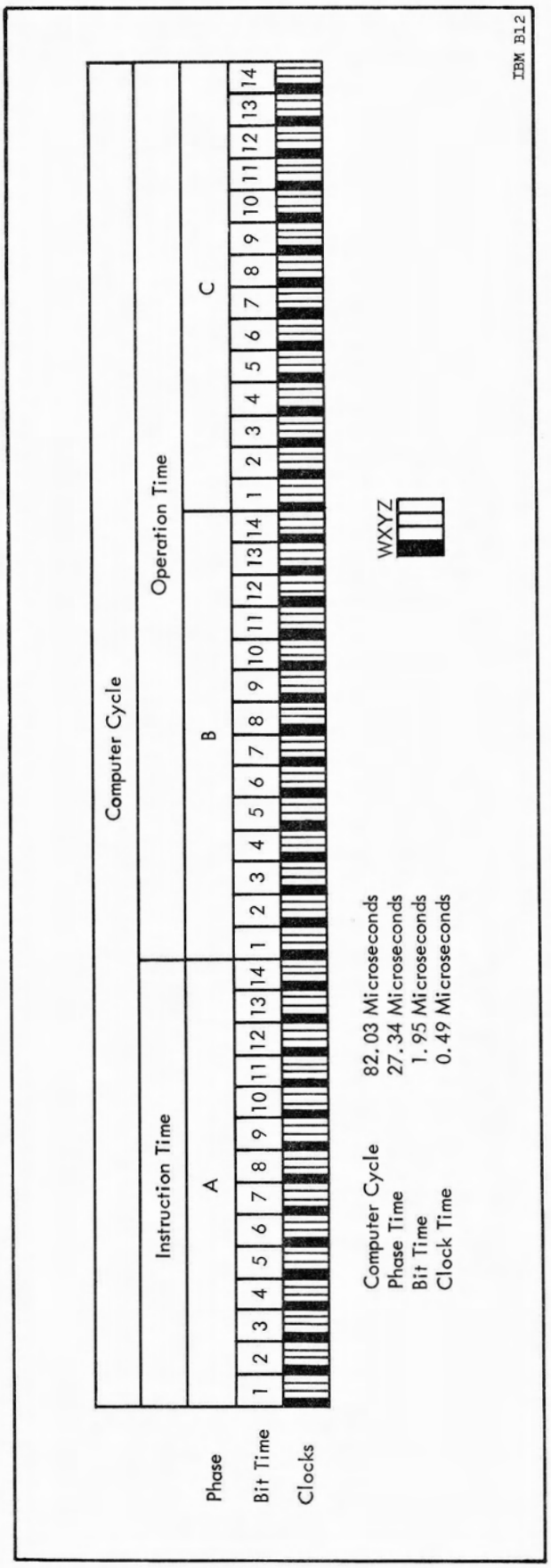


Figure 15.4-3 Computer Timing Organization

The clock generator consists of 4 parts: an oscillator, a buffer amplifier, timing logic, and clock drivers (Figure 15.4-4). (All parts except the oscillator are triple redundant; therefore, the following description applies to all channels.) The clock generator produces a repetitive sequence of four clock pulses (W, X, Y, and Z) which are used to time logic operations in the LVDC. A special clock called BON is generated for driving the delay lines. The logic clocks occur at a repetition rate of 512 kHz, while the delay-line clock occurs at a 2.048 MHz rate.

The oscillator produces a 2.048 MHz sine wave which is used, ultimately, to generate all other computer timing signals. The sine wave is amplified and shaped in the buffer amplifier which produces a complementary pair of square wave outputs, BO and BON. The BON signal is fed to the delay lines and the BO signal to the timing logic where it is frequency divided to generate signals which separate the 4 clocks.

A modified Pierce oscillator is used to generate the 2.048 MHz sine wave which is the basic timing signal for the clock generator. The oscillator contains only 6 components and draws all its operating current from the buffer amplifier. The low component count and absence of a supply-voltage input greatly enhances the oscillator's reliability.

15.4.4 MEMORY

A core memory provides the necessary storage medium in the LVDC. The memory is divided into memory modules. The number of memory modules may vary from one to eight. Each module consists of 14 planes with 128 by 64 cores in each plane (a total of 114,688). The basic module contains 4,096 non-redundant 28-bit words (one bit per core). The memory modules operate independently and may be used in either a simplex or duplex mode. In the simplex mode, each memory module is usable for programming. Duplex operation requires pairs of memory modules to function in parallel. Each pair of modules containing the same information, effectively halves the amount of storage that would be available if the same number of modules were operated simplex. With 8 memory modules operating in simplex, the computer has a memory capacity of 32,768 words (of 28 bits each) which is equivalent to the basic memory capability of the IBM 7090 commercial machine. Storage external to the memory is located predominantly in glass delay lines and latches to provide temporary storage for the accumulator, PQ registers, etc.

The organization of the memory modules is indicated in Figure 15.4-5. For addressing, the 128-core dimension is divided into two equal 64-core

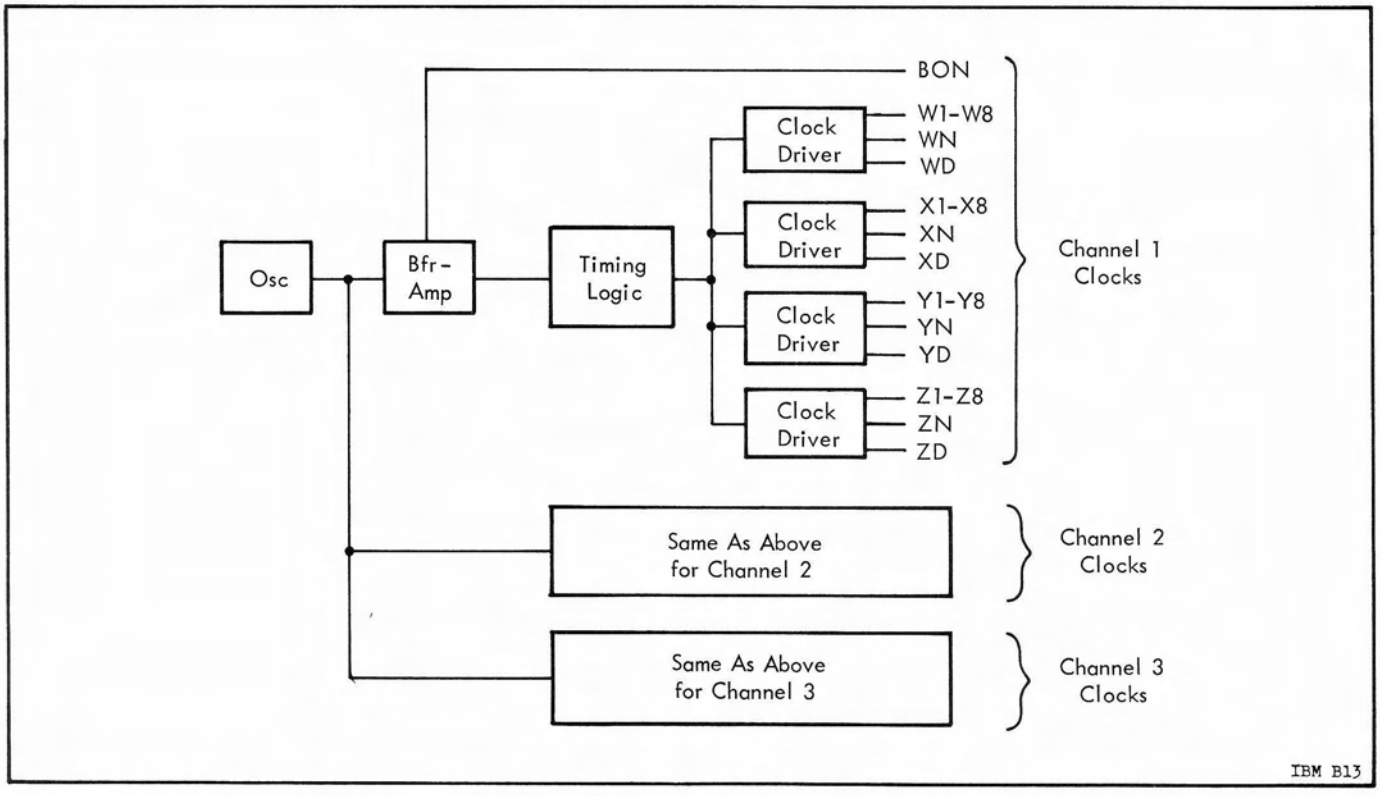


Figure 15.4-4 Clock Generator Block Diagram

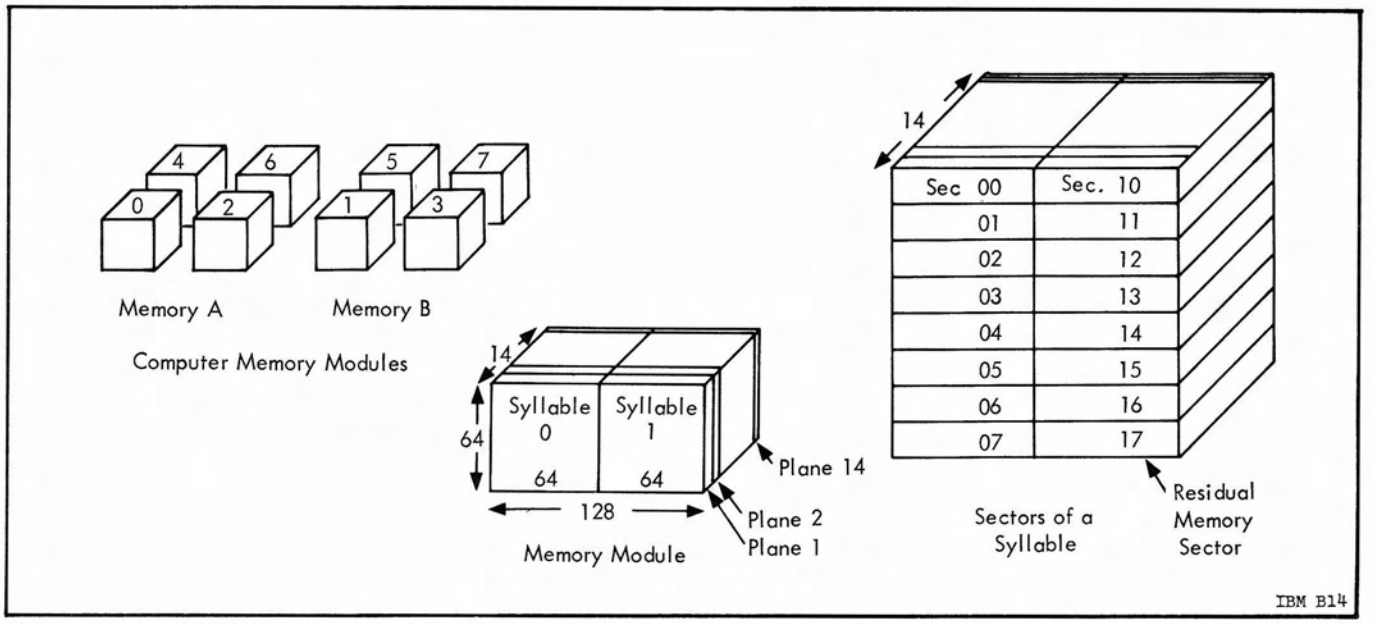


Figure 15.4-5 Memory Module Arrangement

sections to produce the syllable 0 and syllable 1 portions. Each syllable is then divided into 16 sectors (with 8 by 3 cores each). The last sector in each syllable is called residual memory. It provides a common storage area within the module (for constants, frequently used formulas, etc.) and allows efficient programming. Thirteen of the fourteen memory planes in the memory are for data and instructions and one plane for parity bits.

Each sector will have 256 addresses ranging from 0 through 377 (octal). Addresses of sector 17 (residual storage) will be 400 to 777 (octal). The selection of memory modules is program-controlled. The LVDC has the capability of using instructions from one module and data from another, or both from the same module.

To enable the memory to function with a serial arithmetic unit, a serial-by-bit operating mode is used. This is accomplished by taking two 13-bit memory words (syllable 0 and syllable 1) and producing a 26-bit computer word. The central computer logic then utilizes the serialized computer word. Odd parity is assigned to each half, or 13 bits, of a computer word when it is written into memory. A parity check is made on all information read from memory.

CORE MEMORY FUNDAMENTALS

Figure 15.4-6 illustrates the properties of a ferrite core. As shown in the figure, the core can be magnetized in either of 2 directions. By establishing that a core "contains" a "1" when magnetized in one direction and a "0" when magnetized in the opposite direction, the core can be used to store one "bit" of a binary number. The core is magnetized by passing a dc current of $\frac{I}{2}$ through the X and Y drive lines in coincidence.

The direction of magnetic flux about the core can be reversed by passing the same currents through the drive lines in the opposite direction. Reversing a core in this manner is called "switching" the core. A sense winding, represented by S in the figure, also passes through the core and lies within its magnetic field. When a core is switched, the resulting collapse and expansion of its magnetic field causes a pulse of voltage to be induced in the sense winding. Thus, if

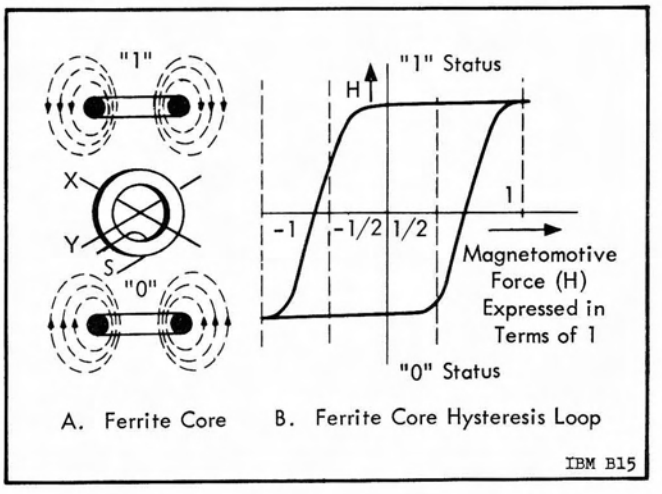


Figure 15.4-6 Ferrite Core Characteristics

a core containing a "1" is switched to a "0", the resulting voltage pulse in the sense winding can be amplified and used to set a latch, indicating the core contained a "1". If the core already contained a "0" it would not switch, and no voltage pulse would appear in the sense winding to set the latch.

This is the method used for reading information from a core memory. It is called "destructive readout" because after the core is read it no longer contains the "1" which was sensed from it. The latch into which the "1" was read is a buffer between the core and the circuits which use the stored information. The "buffer latch" stores the "1" until it can be transferred into the computer and until the core can be switched back to its original state. The process of driving a core to a "0" and sensing whether or not it produced an output is called a "read cycle". Switching the core back to its original state is called a "store cycle".

Cores are arranged in rows and columns as shown in Figure 15.4-7. An X drive line passes through all the cores in a column and a Y drive line through all the cores in a row. The unit is called a plane. The cores are positioned on the drive lines in a pattern which puts the magnetic fields of adjacent cores 90 degrees apart; this eliminates interference between cores. The sense winding runs parallel to the Y drive lines and passes through all the cores in the plane.

If the plane is viewed as the first quadrant of a Cartesian Coordinate System, the X and Y drive lines represent units along the X and Y axes. The location of each core can then be defined by the X and Y drive lines which pass through it. The circuits which operate the plane are controlled so that only one X and one Y drive line carry current at any given time. Only the core at the intersection of the selected drive lines receives the coincident current necessary to switch it. Hence, this method of selecting memory locations is called "coincident-current addressing". When a memory location is selected by coincident-current addressing, one core along each selected drive line receives the full current necessary to select it.

Computers operate using "words" which comprise a number of bits, thus the memory must be expanded to store a complete word in each location. The expansion is accomplished by providing a separate plane for each bit in the word. The planes are stacked one above the other to form an "array". Each X drive line is linked to the corresponding lines of the other planes in the array to form one continuous drive line. This drive line passes through the same locations in every plane of the array. The Y drive lines are similarly interconnected. Thus, when a pair of drive lines are energized, a core is selected in each and every plane at the corresponding intersection of the X and Y drive lines.

Each plane has a separate sense winding and buffer latch to allow the bits to be sensed individually. However, a problem is encountered in attempting to restore the information into the memory.

As presented up to this point, energizing a pair of drive lines switches all the cores in the addressed location to the same state. There is (thus far) no provision for storing numbers which contain both "1's" and "0's". Therefore, a fourth winding called an "inhibit" winding is wound through each plane to allow bits to be stored individually. The inhibit winding runs parallel to the X drive line and carries the same current (but in the opposing direction) as the drive line. These windings are utilized only during store cycles. During a store cycle, the drive lines attempt to switch every core in the addressed location to "1's". However, any buffer storage latches containing "0's" energize the inhibit windings in the corresponding planes. Inhibit current opposes the current in the X drive line and cancels its effect. Thus, the addressed cores in the inhibit planes feel only the half-select current of the Y drive line and do not switch. Since the cores in the addressed location were all switched to "0's" when they were read, any inhibited cores will simply remain in the "0" state.

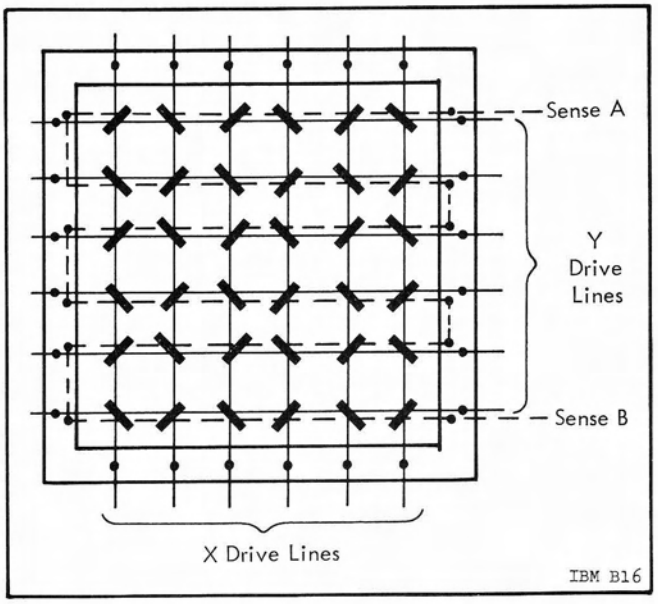


Figure 15.4-7 Core Plane

Associated with the array are a number of special circuits which are required to operate the array. Included in these circuits are the sense amplifiers, some special timing circuits, and the circuits which provide power to the drive lines and inhibit windings.

MEMORY MODULES

The memory element is composed of up to eight integral and asynchronous memory modules, which operate under control of the memory control element. The modules are termed "integral" because each module is a complete memory in itself. Included in each module are a core array and all the circuits required to transfer information to and from it. Asynchronous refers to the fact that the timing signals which carry a module through a memory cycle are developed within the module and are not in synchronism with any others in the computer. When information is to be transferred to or from the memory element, the computer delivers a sync impulse to the selected module (or modules), waits a reasonable time for the module to perform the transfer, and then continues (assuming that the transfer is complete). During the memory cycle, the memory control element provides signals to the memory element which control addressing and determine the direction of transfer.

Figure 15.4-8 is a block diagram of a memory module showing all the circuits it comprises. The memory clock drivers (upper left) receive the sync impulse from the computer and convert it to a series of read or store timing pulses. The timing pulses turn the memory address drivers and inhibit drivers ON and OFF and strobe the sense amplifiers at the

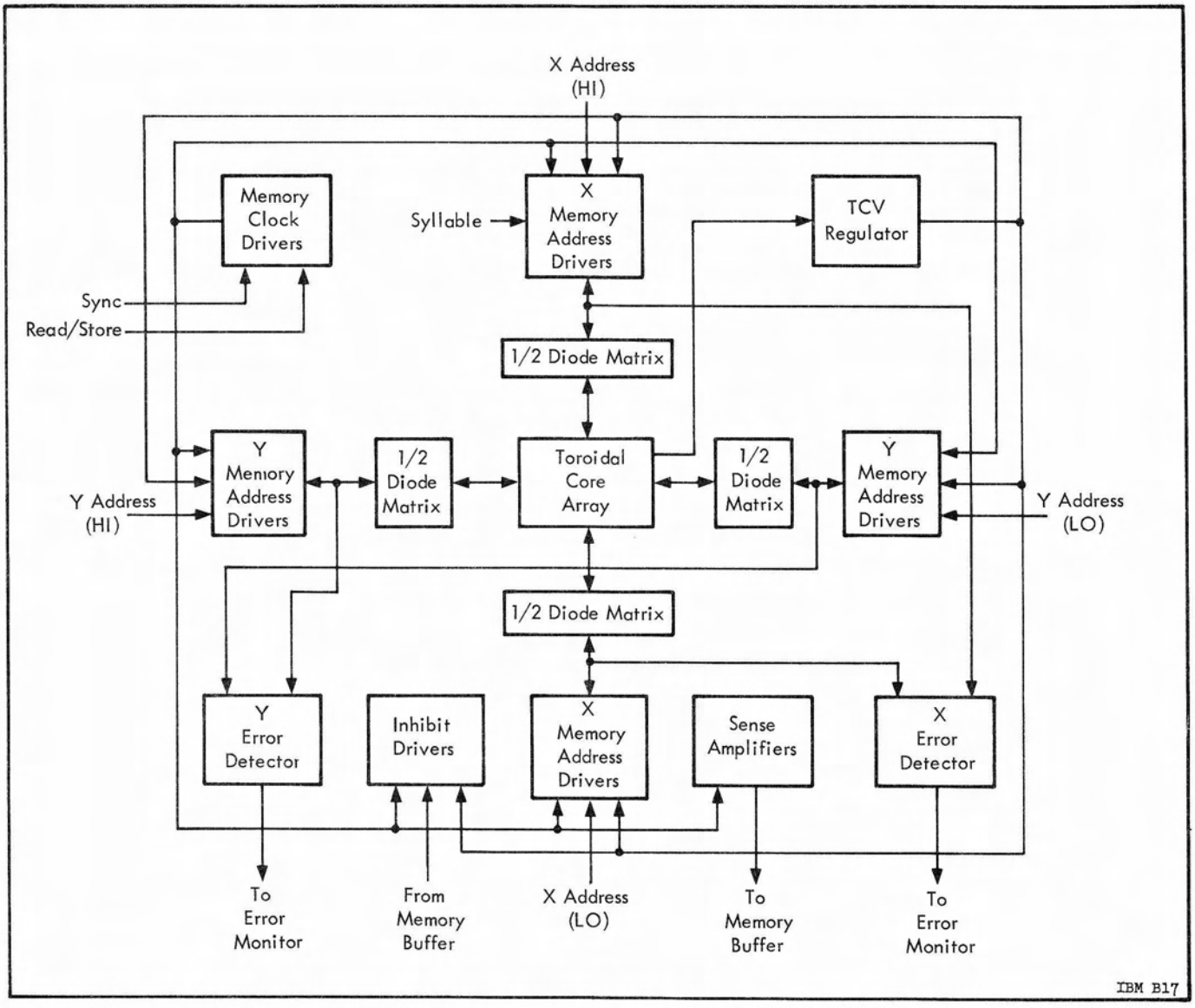


Figure 15.4-8 Memory Module Block Diagram

proper time. There are two memory address drivers for each drive line in the array. Addressing signals from the memory control element select one X and one Y drive line by conditioning two X and two Y memory address drivers. When the timing pulses occur, the conditioned memory address drivers pass coincident current pulses through the selected drive lines to switch the cores in the addressed location. Diode matrices provide isolation between drive lines. A pair of error detectors continuously sense X and Y half-select current to indicate addressing errors to error monitor circuits in the memory control element. A temperature controlled voltage regulator adjusts the memory address drivers and inhibit drivers to produce the optimum current output for the prevailing temperature in the array. A temperature sensing element, attached to the array, develops the inputs for the temperature controlled voltage regulator.

Static control signals from the memory control element determine whether information will be read or stored by conditioning the memory clock drivers to produce the appropriate series of timing pulses. If information is to be read, a series of read pulses is generated causing the memory address drivers to switch all the addressed cores to "0's". Read timing includes a strobe pulse for the sense amplifiers which is delayed from the drive current to allow for the inductive reactance of the windings through the array. If the purpose of the read cycle is to clear the addressed location so that new information may be stored in it, the strobe pulse is inhibited and the sense amplifiers produce no outputs.

If a store cycle is required, the timing pulses produced by the memory clock drivers reverse the polarity of the memory address driver outputs. The memory address drivers then attempt to drive all the addressed cores to "1's"; however, the store pulses are also routed to the inhibit drivers. Any inhibit drivers conditioned by "0's" in the memory buffer register will produce an output opposing the X drive current. Inhibited cores feel only the Y half-select current and therefore remain in the "0" state.

The memory control element provides the timing, decoding, memory selection and temporary storage operations which are required to properly operate the memory element. The memory control element consists of two buffer registers, a timing and sync selection circuit, address decoding circuits, syllable selection circuits, a memory mode and module selection circuit, and an error monitor and memory select circuit.

The computer memory readout is destructive, i.e., as data is read from the memory, the applicable memory bits are all driven to "0". The buffer registers hold the data read from memory long enough so that it can be read back in, thereby making the memory readout effectively non-destructive.

In addition to saving the memory from progressive obliteration, the memory buffer registers feed memory data to the transfer register, and receive data to be stored in memory from the transfer register. The transfer register assumes the role of a shift register when it is receiving data to be loaded into memory. To function as a shift register, the transfer register makes use of multiple clocks. Therefore, special timing is required to lift data from the transfer register as soon as it has been loaded and before it starts another shift cycle. This timing is provided by the buffer register timing circuits which will be discussed later.

The memory select and error monitor circuit continuously checks the performance of the memory. During duplex operation, the memory buffer selection is controlled to correct transient errors and provide an uninterrupted flow of reliable information to the computer. Memory errors are detected by parity checking the buffer registers after every read cycle and by monitoring the outputs of the error detector circuits in the memory modules.

In duplex operation the A and B memories are cycled simultaneously but only one buffer register is selected to provide information to the computer. If an error is detected during a read cycle, the memory buffer containing good information is selected to control restoring both memories; thus the error, if transient, is corrected. If an error occurs in the memory selected to feed the computer, the selection is changed to the correct buffer before the information is used. Thus, the computer receives only reliable information unless both memories fail at the same storage location simultaneously. Operation is not restored to the previously selected memory unless the good memory should develop an error. Monitor signals are provided at the computer interface which indicate the status of each memory and simultaneous failure of both memories.

The memory select and error monitor circuit includes separate parity check and error-detector sensing circuits for each memory; these circuits are called the "error monitors". The error detectors in the memory modules indicate 3 types of addressing failures: (1) multiple address selection; (2) loss of half-select current and (3) spurious selection during

non-cycle times. These failures are combined into 2 types, "on current failures" and "no current failures" by the error-detector sensing circuits. Timing signals which enable the error monitors to sense the different types of errors at the appropriate times are common to both error monitors.

Information flows from the memory buffer registers in 2 directions, through the inhibit drivers into the memory and into the computer to be used. The memory select latches provide separate control over data flowing in each direction. Separate control is maintained so that errors occurring in the non-selected memory can be corrected from the selected memory without changing the selection of the memory buffer which is providing information to the computer.

15.4.5 COMPUTER INSTRUCTIONS

The computer uses a complement of 18 single-address instructions which are composed of a 4-bit operation code and a 9-bit operand address. The 4-bit operation code can select 1 of 16 different instructions to be executed; this range is extended to 18 by grouping 3 instructions under one operation code, then using bits A8 and A9 of the address to discriminate between them. Bits A8 and A9 serve no other function for the instructions which are grouped. A list of the 18 instructions available is given in Table 15.4-2 with the operation code and a brief description of each.

The 9-bit operand address permits selection of 512 memory addresses for use as operands or data storage locations. The memory is divided into a number of sectors, each containing 256 addresses. Address bits A1 through A8 select one of the addresses within the sector. Bit A9 determines whether the address will be in a sector previously selected by the program or in a special sector called "residual memory". Consequently, bit A9 is called the residual bit; residual memory is selected when A9 is a "1".

Instructions which do not require that data be read from the memory frequently use the operand address for special purposes. These special purposes are pointed out in the List of Instructions, Table 15.4-2, where they occur. For example, the shift instructions (SHF) always manipulate the contents of the accumulator and thus requires no operand address; this frees the operand address for use as shift control. One instruction which makes extensive use of its operand address is PIO. A complete breakdown of the PIO addresses is given in Table 15.4-3.

INTERRUPT

A limited program interrupt feature is provided to aid the input-output processing. An external signal can interrupt the computer program and cause a transfer to a subprogram. An interrupt occurs when the instruction in progress is completed. The instruction counter, sector and module registers, and syllable latch are stored automatically in a reserved residual memory location (octal address 777). A HOP constant is retrieved from a second reserved residual memory location (octal address 776). The HOP constant designates the start of the subprogram. Automatic storage of the accumulator and product-quotient registers is not provided. This must be accomplished by the subprogram. Protection against multiple interrupts and interrupts during MPY and DIV operations is provided.

The interrupt signal may be generated by a timed source. The rate at which it is generated is controlled by changing the magnitude of a number which is being continually summed. When the summed number reaches a predetermined value, the interrupt signal is generated. This is accomplished in the LVDA.

The main program can be resumed by addressing the contents of residual memory word 777 with a HOP instruction.

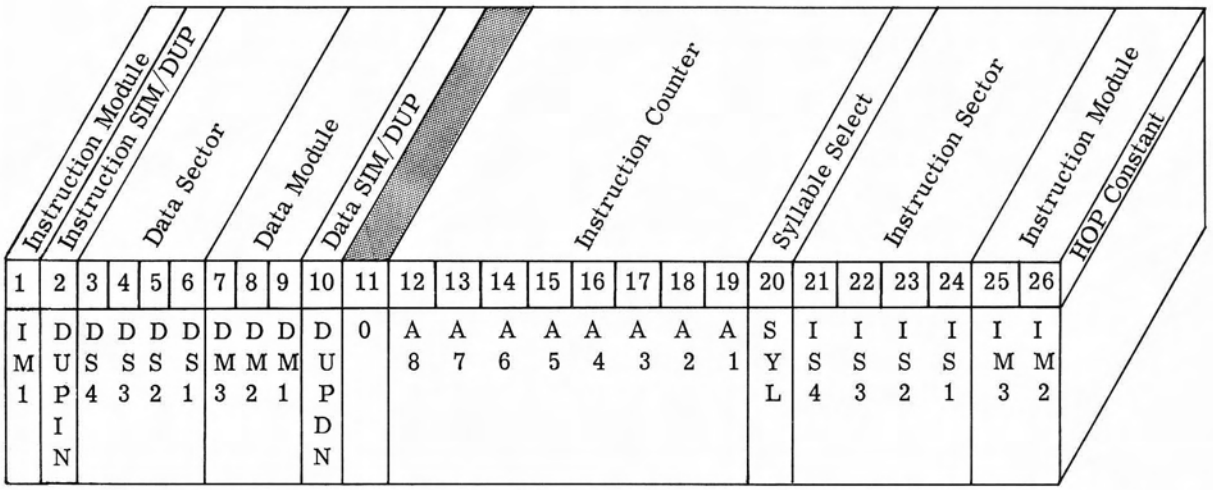
Certain discrete input signals are allowed to cause an interrupt. These are useful in causing the input-output subprogram to give immediate attention to an input or output operation.

The interrupt feature facilitates the timing of input-output operations by causing a transfer to an input-output subprogram. The interrupt signal is generated in the LVDA and may be set to interrupt at the highest rate at which any input-output quantity must be handled. This method avoids the necessity of keeping track of time expired since last entering the input-output subprogram.

The automatic interrupt also makes it possible to permit certain discrete inputs to cause an interrupt. Allowing discrete inputs to interrupt makes it possible to demand that the program give attention to an important discrete input. Communications between the LVDC and the vehicle telemetry monitoring system are thus facilitated.

Table 15.4-2 List of Instructions

Instruction	Operation Code 4 3 2 1	Description
HOP	0 0 0 0	Transfers program to memory location specified by HOP constant and controls simplex/duplex operation of memory. Operand address specifies memory location of HOP constant used to load the registers shown in HOP constant format (below). Full HOP constant MUST be specified each time. First instruction following HOP comes from new location.



MPY	0 0 0 1	Multiplies contents of memory location specified in operand address by contents of accumulator. Uses 24 high-order bits of each operand to form 26-bit product. Product of multiplicand and 12 low-order bits of accumulator is available by addressing 775 with second instruction following MPY; final product is available to fourth instruction following MPY. Program continues while MPY is in progress; concurrent use of accumulator is permitted.
SUB	0 0 1 0	Subtracts contents of memory location specified in operand address from contents of accumulator. Places remainder in accumulator.
DIV	0 0 1 1	Divides contents of memory location specified by operand address into contents of accumulator. The 24-bit quotient is available to the eighth instruction following divide by addressing the P-Q register (775). Program continues while DIV is in progress; concurrent use of accumulator is permitted.
TNZ	0 1 0 0	Conditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select if accumulator contents are not zero. Next instruction comes from new syllable and address. If accumulator is zero, perform next instruction in sequence.
MPH	0 1 0 1	Multiplies contents of memory location specified in operand address by contents of accumulator. Uses 24 high-order bits of each operand to form 26-bit product. Holds up program until multiplication is complete. Product is available from accumulator or P-Q register with instruction following MPH.
AND	0 1 1 0	AND's contents of memory location specified in operand address with contents of accumulator. Result is placed in accumulator.
ADD	0 1 1 1	Adds contents of memory location specified in operand address to contents of accumulator. Sum is placed in accumulator.

Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code 4 3 2 1	Description
TRA	1 0 0 0	Unconditional transfer. Transfers operand address (A1-A8) to instruction counter and A9 to syllable select. Next instruction comes from new syllable and address.
XOR	1 0 0 1	Exclusive - OR contents of memory location specified in operand address with contents of accumulator, bit-for-bit. When accumulator bit and bit from memory are different, a "1" is placed in the corresponding bit of the accumulator; if accumulator bit and memory bit are alike, a "0" is placed in the accumulator.
PIO	1 0 1 0	Process input or output. Operand address specifies input or output and gives address of data source and destination. See Figure 15.4-3 for listing of addresses.
STO	1 0 1 1	Contents of accumulator is stored in memory location specified by operand address. Contents of accumulator is unchanged. Data can be stored in P-Q register by using address 775. A STO instruction with operand address 776 or 777 causes contents of multiplicand register to be stored in memory location 776 or 777 as specified. These addresses are used for HOP-save feature.
TMI	1 1 0 0	Conditional transfer. Transfer operand address (A1-A8) to instruction counter and A9 to syllable select if accumulator sign is minus. Next instruction comes from new syllable and address. If accumulator sign is plus, perform next instruction in sequence.
RSU	1 1 0 1	Reverse subtract. Contents of accumulator are subtracted from contents of memory location specified by operand address. Remainder is placed in accumulator.
SHF	1 1 1 0 A8 = 0 A9 = 1	Contents of accumulator are shifted MSD or LSD a maximum of 2 bit positions as specified by operand address. Shift control codes are: Address Bit — Shift A1 = 1 — LSD 1 A2 = 1 — LSD 2 A5 = 1 — MSD 1 A6 = 1 — MSD 2 Clears accumulator if all shift control bits are "0's".
CDS	1 1 1 0 A9 = 0	Change data sector. Operand address is used as a constant to load registers indicated below.

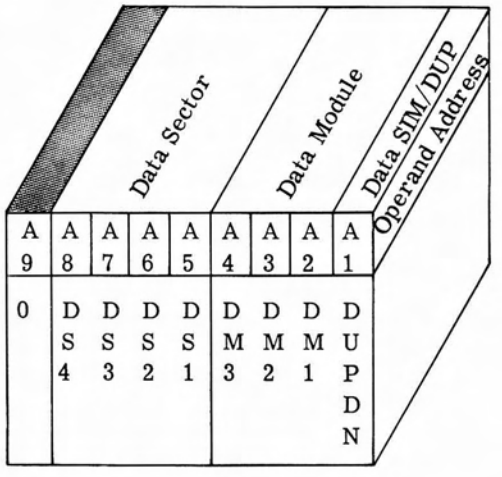
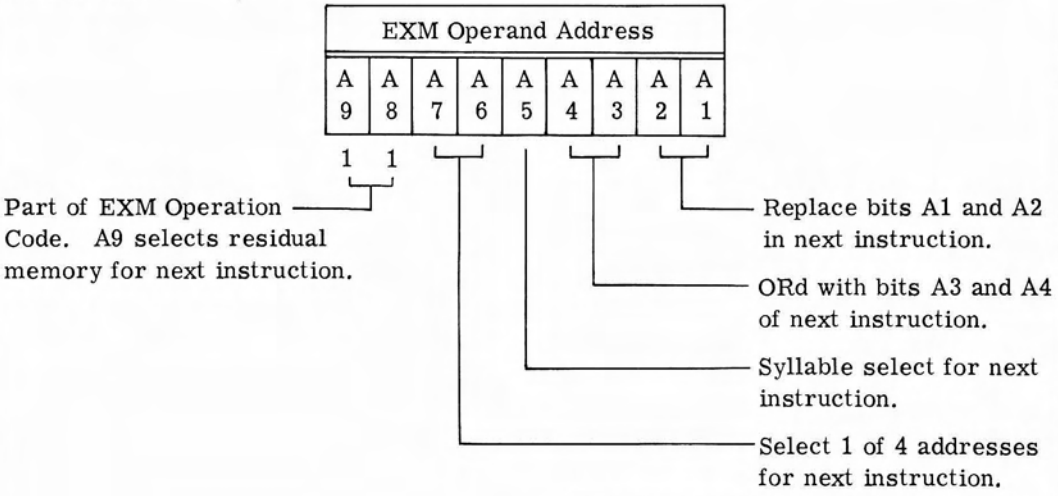


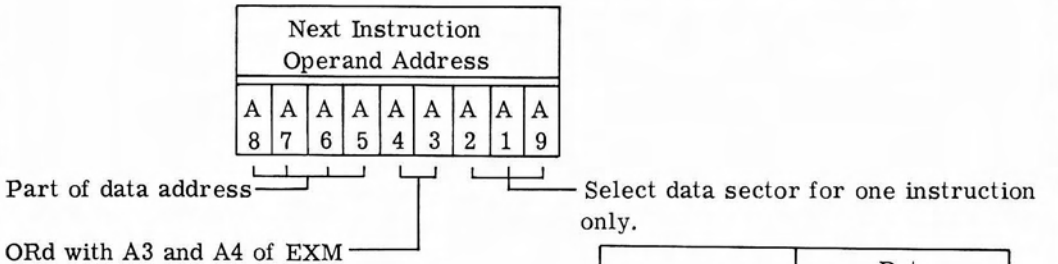
Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code 4 3 2 1	Description
EXM	1 1 1 0 A8 = 1 A9 = 1	Execute modified. Operand address selects 1 of 8 instructions in residual memory to be the next instruction executed and modifies its operand address as shown below prior to execution.



A7	A6	ADD
0	0	600
0	1	640
1	0	700
1	1	740

A5	SYL
0	0
1	1



A2	A1	A9	Data Sector
0	0	0	04
0	0	1	14
0	1	0	05
0	1	1	15
1	0	0	06
1	0	1	16
1	1	0	07
1	1	1	17 (Res. Mem)

Table 15.4-2 List of Instructions (Cont)

Instruction	Operation Code 4 3 2 1	Description
EXM (cont)	1 1 1 0 A8 = 1 A9 = 1	EXM operation is diagrammed below.
CLA	1 1 1 1	Contents of memory location specified by the operand address are transferred to cleared accumulator.

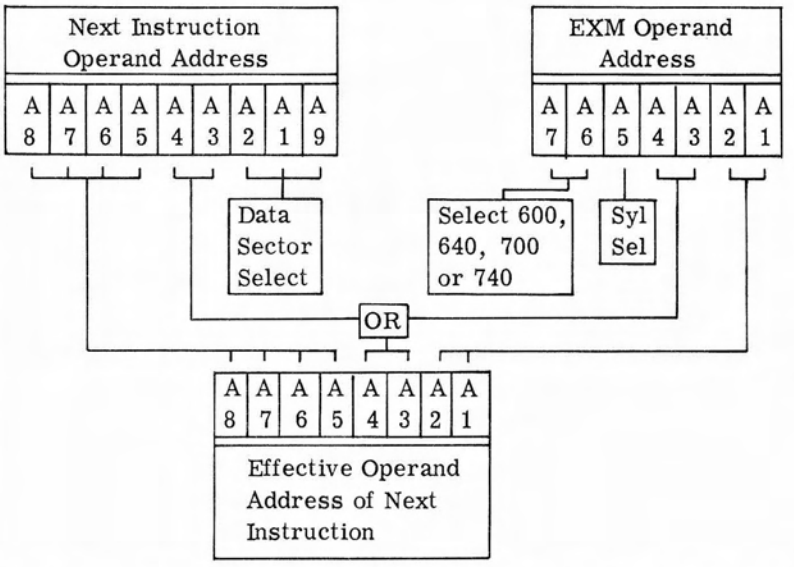


Table 15.4-3 PIO Addresses

Group Selection and Functions											
Group	Data Source	Data Destination	A9	A8	A7	A6	A5	A4	A3	A2	A1
1 & 3	LVDC Accumulator	LVDA Telemetry Registers	X	0	└	Address			┘	0	X
1 & 3A	LVDC Main Memory	LVDA Telemetry Registers	0	1						0	X
1 & 3B	LVDC Residual Memory	LVDA Telemetry Registers	1	1						0	X
2	LVDC Accumulator	LVDA Output Registers	X	0						1	0
2A	LVDC Main Memory	LVDA Output Registers	0	1						1	0
2B	LVDC Residual Memory	LVDA Output Registers	1	1						1	0
4	LVDA Peripheral Inputs and Errors	LVDC Accumulator	X	0						1	1
5	LVDA Resolver Processor Inputs	LVDC Accumulator	X	1						1	1

Group Addresses								
Group 2	Group 4	Group 5	A7	A6	A5	A4	A3
			0	0	0	0	0
Mode Register		Spare No. 6	0	0	0	0	1
Discrete Output Register (Reset)			0	0	0	1	0
Discrete Output Register (Set)		Computer COD Counter Start	0	0	0	1	1
Internal Control Register (Set)	Error Monitor Register	Fine Gimbal No. 1	0	0	1	0	0
Internal Control Register (Reset)			0	0	1	0	1

Table 15.4-3 PIO Addresses (Cont)

Group Address								
Group 2	Group 4	Group 5	A7	A6	A5	A4	A3
Interrupt Register Reset		Coarse Gimbal No. 3	0	0	1	1	0
Switch Selector Register (Load)		Computer COD Counter Start	0	0	1	1	1
Orbital Checkout	Command Receiver	Coarse Gimbal No. 1	0	1	0	0	0
	or RCA-110	Horizon Seeker No. 1	0	1	0	0	1
Switch Selector & Discrete Output	Discrete Input Spares		0	1	0	1	0
Registers(Read)							
		Spare No. 3	0	1	0	1	1
Switch Selector Interrupt Counter			0	1	1	0	0
COD Error (Read)	Telemetry Scanner		0	1	1	0	1
Inhibit Interrupt			0	1	1	1	0
Minor Loop Timed Interrupt							
Counter	Switch Selector	Spare No. 4	0	1	1	1	1
	Real Time		1	0	0	0	0
	Accelerometer						
	Processor X		1	0	0	0	1
		Fine Gimbal No. 4	1	0	0	1	0
	Accelerometer						
	Processor Z	Spare No. 1	1	0	0	1	1
		Horizon Seeker No. 3	1	0	1	0	0
	Accelerometer						
	Processor Y	Horizon Seeker No. 2	1	0	1	0	1
		Coarse Gimbal No. 4	1	0	1	1	0
	Interrupt Storage	Spare No. 5	1	0	1	1	1
		Coarse Gimbal No. 2	1	1	0	0	0
Ladder No. 1			1	1	0	0	1
Ladder No. 2		Fine Gimbal No. 3	1	1	0	1	0
Ladder No. 3		Spare No. 2	1	1	0	1	1
Ladder No. 4		Fine Gimbal No. 2	1	1	1	0	0
Ladder No. 5		Horizon Seeker No. 4	1	1	1	0	1
			1	1	1	1	0
			1	1	1	1	1

A maximum of 12 interrupts are provided for the LVDA. Under normal operating conditions, when a bit is set in interrupt storage, a HOP 400 will be forced to the LVDC upon completion of the instruction currently being executed. When the LVDC program has completed processing the interrupt, a PIO instruction addressing "Interrupt Register Reset" with the bit corresponding to the bit causing the interrupt set, must be sent to the LVDA just prior to executing the return HOP. This is necessary to inform the LVDA that the condition causing the interrupt has been processed. The LVDA will then check to see if the interrupt is still present. If the interrupt is still present, the LVDA will inhibit sending an interrupt for that particular condition until the interrupt has been removed. Once the interrupt has been removed the LVDA inhibit will be removed, and normal processing will be resumed.

15.4.6 COMPUTER CONTROL

The data control element consists of the transfer register and the parity counter. The transfer register is the central storage location in the LVDC which provides a two-way path for transfer of data or instructions between itself and the memory, or itself and other storage locations in the central computer. The parity counter assigns a parity bit to all syllables of data that are stored in the memory. When these syllables of data are subsequently read out of memory, their parity condition is checked against the parity bit.

The transfer register is a 13-bit shift register which receives from and sends inputs to the memory buffer registers, the arithmetic element, the multiply-divide element, and the external equipment.

The parity counter assigns parity bits by making all syllables have "odd" parity. The parity counter "counts" the number of "1's" in a syllable and adds a "1", as necessary, so that the total number of "1's" is an odd number. Thus, if the total number of "1's" is even, the parity counter adds a bit; if odd, no bit is added. The parity counter operates during a store operation when data is loaded into the memory.

The program control element steps the computer program through its instructions to execute the commanded operations. To accomplish this task, the program control element performs the following functions:

- Starts or stops the program under external control.
- Conditions the memory address decoders to select programmed instructions or data words.
- Selects data and instruction memory sectors under program control.
- Selects instruction addresses within a memory sector either automatically or under program control by an instruction counter.
- Store, decode, and initiate operation codes.
- Interrupt the program, under external control, to perform a selected subroutine of the program.
- Generate a word (HOP constant) which reinstates the computer program at the instruction where it was interrupted, after completion of an externally commanded subroutine.

The program control element consists of:

- An address register.
- Data and instruction sector registers.
- Operation code register and decoders.
- Interrupt and start-stop control circuits.
- Any automatic HOP save circuit.
- An instruction counter.

The address register stores instruction or data word addresses while the selected word is read from memory. During an instruction word time, the address register stores the instruction address (from the instruction counter) to select the instruction word address. The operand address portion of the instruction word, stored during data word time, is used to select the data word address.

The address register consists of 9 latches, A1 through A9, with associated AND and inverter output circuits for added driving power. Latches A1 through A8 select 1 of the 256 memory locations in a sector; latch A9 determines whether the addressed data will come from a pre-selected sector, or from the residual memory. The addresses of selected memory locations are loaded into the address register from the transfer register. The address register outputs condition the address decoders in the memory control element and provide control to the LVDA for PIO operations. The transfer address latch provides timing and control for the register.

The instruction address (from the instruction counter) is stored in the address register from A-8-W through A-13-X time. During this period, the addressed instruction is read from memory and placed in the transfer register. The operand address portion of the instructions is then transferred to the address register at A-13-Z time for storage while the data word is read from memory.

The address register stores the data word address from A-14-W through the following A-7-X time. The address register is reset at A-7-Y and A-13-Y times prior to storing the instruction and data addresses.

An EXM instruction executes and modifies the operand address of one of the instructions stored in residual memory locations 600, 640, 700, and 740. The operand address portion of the EXM instruction is transferred into the address register at A-13-Z time. The data stored in latches A1 through A5 remains in the transfer register to select the syllable of the instruction to be executed and modify its address. This data must be cleared from latches A1 through A5 to select the desired residual memory locations.

The data and instruction sector registers store sector codes to select 1 of 16 memory sectors during operation and instruction times, respectively. Sector codes are loaded into both registers during a HOP instruction (HOP sets CDSV to load the data sector register); the data sector register is also loaded during a CDS instruction. The registers store the sector codes until the next HOP (or CDS) instruction commands them to change. The sector register outputs condition the memory address decoders.

The 4-bit operation code register stores the code of the commanded instruction while the instruction is executed. The operation code register outputs control the operation of the circuits which execute the instructions.

The operation code register, loaded by the transfer register, stores the operation code from A-12-Y to A-5-Y time (nearly a full computer cycle).

The operation decoders supplement the operation code register in controlling the operation of circuits which execute the commanded operations. The operation decoders decode programmed operation codes and computer signal combinations to generate control signals. The programmed operation codes which condition the decoders are supplied via the transfer register, address register, or operation code register.

The instruction address is incremented in the arithmetic element and stored in the unused portion of the accumulator register. The instruction address consists of 9 bits but only 8 bits are stored in the accumulator register. When the instruction address is transferred to the address register from the accumulator register to select an instruction, a "0" is forced into address register bit A9 position. The instruction address is increased by one each instruction time during normal operation. The instruction address is not increased during an EXM instruction, during the first four computer cycles of a MPH operation, or after the commanded instruction is completed during a CST operation. The instruction address is changed during a transfer operation; the instruction address currently stored in the accumulator-register is dropped and the transfer instruction operand address is loaded into the unused portion of the accumulator register. The instruction counter is actually part of the arithmetic element.

The LVDC is programmed by means of single-address instructions. Each instruction specifies an operation and an operand address. Instructions are addressed sequentially from memory under control of the instruction counter. Each time the instruction counter is used, it is incremented by one to develop the address of the next instruction. After the instruction is read from memory and parity checked, the operation code is sent from the transfer register to the operation code register, a static register which stores the operation code for the duration of the execution cycle.

The operand address portion of the instruction is transferred in parallel (9 bits) from the transfer register to the memory address register. The transfer register is then cleared.

If the operation code requires reading the memory, the contents of the operand address are read 14 bits at a time (including parity) from the memory into the buffer register where a parity check is made. Data bits are then sent in parallel to the transfer register. This information is then serially transferred to the arithmetic section of the computer. If the operation code is a STO, the contents of the accumulator are transferred serially into the transfer register and stored in two 14-bit bytes. A parity bit is generated for each byte.

Upon completion of the arithmetic operation, the contents of the instruction counter are transferred serially into the transfer register. This information is then transferred in parallel (just as the operand address has previously been transferred) into the memory address register. The transfer register is then cleared and the next instruction is read. This completes one computer cycle.

The data word is read from the memory address specified by the memory address register and from the sector specified by the sector register. Data from the memory goes directly to the arithmetic section of the computer where it is operated on as directed by the operation code.

15.4.7 ARITHMETIC SECTION

The arithmetic section contains an add-subtract element, a multiply-divide element, and storage registers for the operands. Registers are required for the accumulator, product, quotient, multiplicand multiplier, positive remainder and negative remainder. The add-subtract and the multiply-divide elements operate independently of each other. Therefore, they can be programmed to operate concurrently if desired; i.e., the add-subtract element can do several short operations while the multiply-divide element is in operation.

The arithmetic element performs the following general type of operations:

- Arithmetic (addition, subtraction, and shifting)
- Logical extraction
- Stores new operand and a new instruction counter (previously described)
- Modifies the stored instruction counter

The arithmetic element consists of the following (Figure 15.4-9):

- Accumulator Control circuits (Accum Control)
- Add/Subtract circuit (A/S)
- Accumulator Register (Acc Reg)

The A/S circuit and Acc Reg make up an accumulator which performs the arithmetic and logic operations and stores the results. The Acc Reg stores 2 pieces of data: the results of the arithmetic operation (called the stored operand) and the instruction counter.

The Accum Control circuits provide timing and conditioning gates for the A/S and Acc Reg circuits. (The conditioning gates are instruction oriented.)

The A/S circuit performs the following arithmetic and logical extraction operations:

Addition	(ADD)	Arithmetic
Subtraction	(SUB)	
Reverse-Subtraction	(RSU)	
Clear-and-Add	(CLA)	
And	(AND)	Logical Extraction
Exclusive OR	(XOR)	

In each of the preceding operations only the stored operand and the new operand are affected.

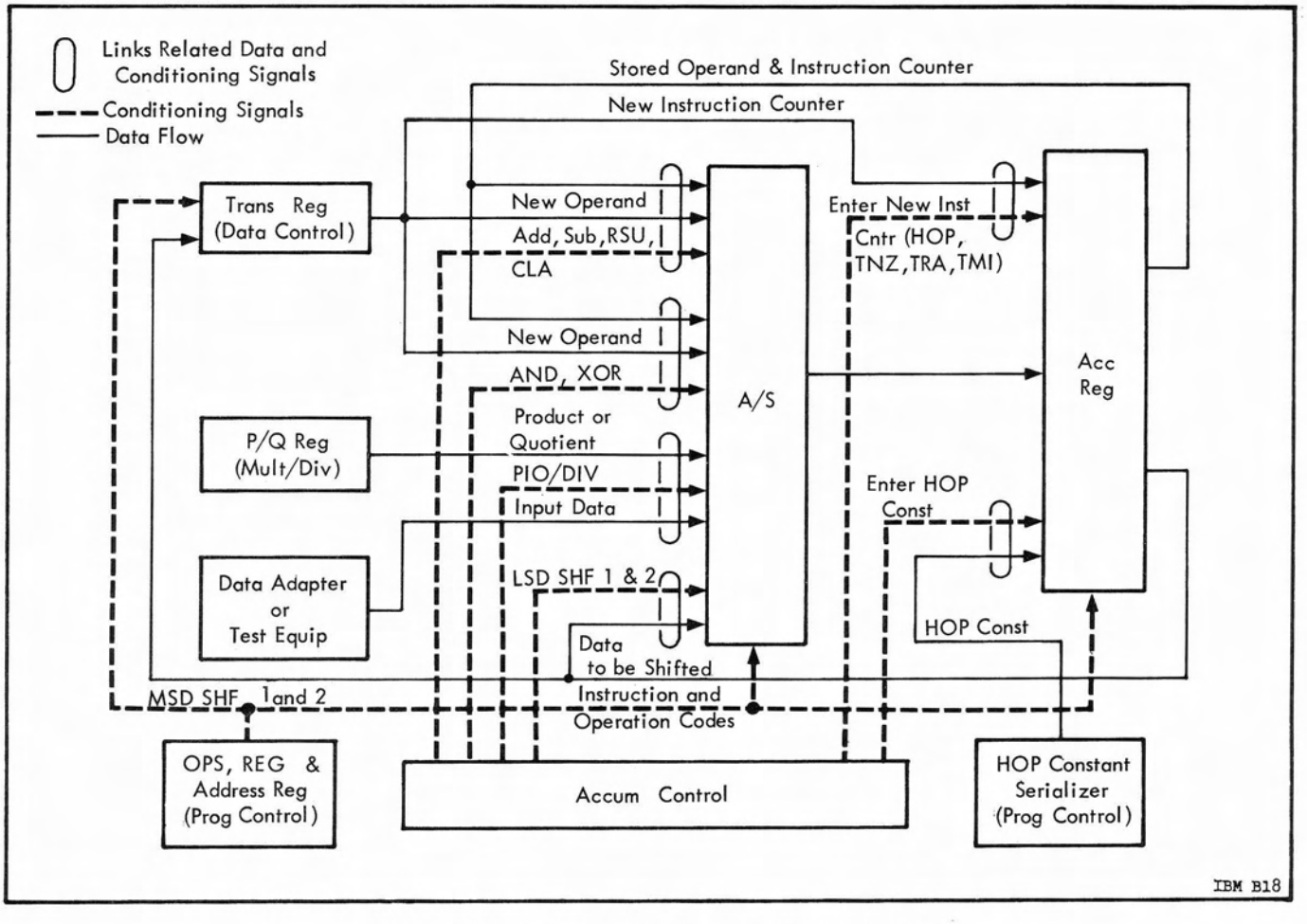


Figure 15.4-9 Arithmetic Element Block Diagram

(The instruction counter is recirculated and updated automatically, except during PIO operations.) During a CLA operation the stored operand is inhibited and the new operand enters the Acc Reg unaltered. Similarly, the product or quotient (from the multiply-divide element) and input data (from the LVDA or test equipment) enters through the A/S circuit and replaces the stored operand in the Acc Reg. During a SHF operation, the stored operand leaves the Acc Reg and returns early to the Acc Reg directly through the A/S circuit for an LSD shift 1 or 2; the stored operand leaves the Acc Reg and returns from the transfer register late for an MSD shift 1 or 2. MSD-shifted data from the transfer register enters the A/S as a new operand.

The Acc Reg is a circulating shift register which utilizes the A/S circuit to complete the loop. When no operations are called forth, the stored operand and instruction counter are continually circulated; the stored operand is unaltered and the instruction counter updated during each pass through the A/S circuit. A new instruction counter (required when performing one of the transfer operations) or a new instruction counter and HOP constant (which becomes the stored operand) may be entered directly into the Acc Reg when performing a HOP.

During each program cycle-time, the result of the simple arithmetic operations are circulated through the accumulator delay line and through the accumulator sync delay line channel to prevent processing of the results.

The multiply element operates in a 2-phase cycle, serial-by-four parallel, and requires 15 phase times, including instruction access time. The program initiates a multiply by placing the 24 high-order bits of the contents of the memory location specified by the operand address into the multiplicand delay line. The multiplier delay line contains the 24 high-order bits of the contents of the accumulator. The phase counter terminates a multiply instruction.

The instrumentation of the multiply algorithm requires 3 delay line channels. Two of the channels contain the partial product and the multiplier. These channels shift both the partial product and the multiplier 4 places to the right every 2-phase cycle. The third channel contains the multiplicand. The accumulator portion (fourth channel) of this delay line is not involved in the multiply operation and can be used concurrently with the multiply operation.

Upon initiation of a multiply and during every other phase time thereafter, the 5 low-order bits of the multiplier (MR_1, MR_2, MR_3, MR_4, and MR_5) are placed in latches or tratches and are used to condition addition or subtraction of multiples of the multiplicant to the partial product. The following algorithm is utilized for multiply:

$$P_i = 1/16 \left[P_{(i-1)} + \Delta 1 + \Delta 2 \right]$$

P_i is the new partial product, and $\Delta 1$ and $\Delta 2$ are formed according to the following rules:

MR_1	MR_2	MR_3	$\Delta 1$	--
MR_3	MR_4	MR_5	--	$\Delta 2$
0	0	0	0	0
1	0	0	+2M	+8M
0	1	0	+2M	+8M
1	1	0	+4M	+16M
0	0	1	-4M	-16M
1	0	1	-2M	-8M
0	1	1	-2M	-8M
1	1	1	0	0

M represents the multiplicand. For the first multiplication cycle $P_{(i-1)}$ and MR_1 are made zeros.

The divide element operates in a 2-phase cycle, serial-by-two parallel, and requires 27 phase times per divide, including instruction access time. The program initiates a divide by transferring the 26 bits of the addressed memory location (divisor) and the 26 bits of the accumulator (dividend) to the divide element. The phase counter terminates a divide operation.

The following algorithm is instrumented to execute divide:

$$Q_1 = R_{is} \cdot DV_s + \overline{R_{is}} \cdot \overline{DV_s} \qquad (1)$$

and

$$R_{i+1} = 2R_i + (1 - 2Q_i)\, DV \qquad (2)$$

where

$1 = 1, 2, 3, \ldots 24$

Q_i = The i^{th} quotient bit

R_{is} = The sign of the i^{th} remainder

DV_s = The sign of the divisor

R_i = The i^{th} remainder

R_1 = The dividend

DV = The divisor

Equation (1) states that the i^{th} quotient bit is equal to a "1" if the sign of the i^{th} remainder is identical to the sign of the divisor. The high-order quotient bit (sign bit) is the only exception to this rule. Q_i as determined by equation (1) is used to solve equation (2) but must be complemented before it is stored as the sign bit of the quotient.

The instrumentation of the divide algorithm requires 3 channels of a delay line. One channel contains the quotient, one the divisor, and one the dividend. These 3 channels are used during multiply to contain the multiplier, the multiplicand, and the partial product respectively. The quotient and the remainder channels of the delay line have been lengthened by latches to shift 2 places to the left each 2-phase cycle. The divisor circulates once each 2-phase cycle.

In the two's complement number system, the high-order bit determines the sign of the number. Since this is the last bit read from memory, it is impossible to solve equations (1) and (2) until the entire divisor has been read from memory. However, equations (1) and (2) can have only two possible solutions.

Either,

$$Q_i = 1$$

and,

$$R_{(i+1)} = 2R_i - DV$$

or,

$$Q_i = 0$$

and,

$$R_{(+1)} = 2R_i + DV$$

Both the borrow of $2R_i - DV$ and the carry of $2R_i + DV$ are generated as the dividend and divisor registers are loaded. When the sign bits of these quantities are finally entered into their respective registers, equation (1) is solved for the first quotient bit. If this quotient bit is a one, the borrow is examined to determine the second quotient bit. If the first quotient bit is a zero, the carry is examined to determine the second quotient bit. The following truth table is solved to determine the second quotient bit if the first quotient bit is a one.

R_i	DV_s	B	$R_{(i+1)s}$	Q
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Where

R_i = The first remainder bit to the right of the sign bit

DV_s = The divisor sign

B = The borrow into the R_i, DV_s position

$R_{(i+1)s}$ = The sign of the new remainder

Q = The quotient bit as determined by comparing DV_s with $R_{(i+1)s}$ according to equation (2)

$$Q = \overline{R_1}\,\overline{DV_s} \cdot \overline{B} + \overline{R_1} DV_s\, \overline{B} + R_i \cdot \overline{DV_s} \cdot B + R_i \cdot DV_s \cdot B$$

$$= \overline{R_i} \cdot \overline{B}\,(\overline{DV_s} + DV_s) + R_i \cdot B\,(\overline{DV_s} + DV_s)$$

$$= \overline{R_i} \cdot \overline{B} + R_i \cdot B$$

The equation used in generating the new remainder, R_{i+2}, is obtained by expanding equation (2) as follows:

$$R_{(i+2)} = 2R_{(i+1)} + \left[1 - 2Q_{(i+1)}\right] DV$$

$$R_{(i+2)} = 2\left[R_i + (1 - 2Q_i)\, DV\right] + \left[1 - 2Q_{(i+1)}\right] DV$$

$$R_{(i+2)} = 4R_i + 2\,(1 - 2Q_i)\, DV + \left[1 - 2Q_{(i+1)}\right] DV$$

As $R_{(i+2)}$ is being generated, the next iteration of divide is started by generating, as already described, the borrow and carry for $2R_{i+2} \pm DV$.

No dividend register is described because it is considered to be the first remainder. Both multiply and divide operations require more time for execution than the rest of the computer operations. A special counter is used to keep track of the multiply-divide progress and stop the operation when completed. The product-quotient register has been assigned an address and is addressable from the operand address of the instructions SUB, AND, ADD, XOR, STO, RSU, and CLA. (Refer to Table 15.4-2 for a description of instruction codes.) The answer will remain in the product-quotient register until another multiply-divide is initiated.

Ultrasonic delay lines are utilized for short term storage. The delay medium is zero temperature-coefficient glass. One bit of information is a 0.2-microsecond pulse which propagates through the delay medium at the speed of sound in the medium. Ceramic transducers are used for energy conversion. Glass delay lines provide very reliable and stable short-term storage along with simple instrumentation.

The maximum data rate of the delay line in this computer is 2 megahertz. Thus, only one delay line, delay line driver, and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier combination are required for storage of up to four different logic channels. This time-sharing of the delay line, plus driver and sense amplifier, is easily implemented by gating the driver input and sense amplifier output with the four computer clocks.

The delay line input is actually provided by the delay line clock output of the clock generator and the delay line driver acts only as a logic gate. This scheme helps to increase the read-out timing margin and greatly simplifies the delay line driver circuitry.

SECTION 15.5

DESCRIPTION OF

THE LAUNCH VEHICLE DATA ADAPTER

15.5.1 GENERAL CHARACTERISTICS

The Launch Vehicle Data Adapter is the input/ output device for the Launch Vehicle Digital Computer and the central station for the signal flow in the Saturn Astrionics System.

The LVDA includes the following circuits:

- Various registers for buffering input and output signals.
- Delay lines for real time, accumulating accelerometer pulses, storing interrupts, line interrupt counters, and switch selector interrupt counters.
- Power supplies for the LVDA and LVDC.
- Digital-to-analog and analog-to-digital converters.
- Redundancy checkout circuit including channel switching, discrete output switching, and power supply switching.

The LVDA transforms input and output signals to a form that is compatible with the characteristics of the receiving equipment, controls the data flow in the IU, performs certain simple computation and logical operations on data, and provides temporary storage of data.

Communication with the computer is carried out through 512-kilobit per second serial transmission. The PIO instruction permits the specification of either input or output operations and addresses the device to be affected. A single 26-bit word is transferred to the computer accumulator or from the accumulator or memory.

The characteristics of the LVDA are listed in Table 15. 5-1.

15.5.2 DATA ADAPTER INPUT/ OUTPUT SIGNALS

The interconnections between the LVDA and the LVDC are shown in Figure 15. 5-1. Connections between the LVDA and equipment in the IU may be seen in Figure 15. 5-2.

The LVDA accepts discrete input signals from the stage Switch Selectors, IU Command Receiver, ground launch computer, Telemetry Computer Interface Unit, Telemetry Data Multiplexer, Control Distributor, and other vehicle equipment. It has output registers to provide discrete output signals to the above mentioned equipment. It also accepts and processes LVDC interrupt signals from the ground launch computer and the IU equipment.

The LVDA accepts 2-phase resolver analog signals from the ST-124M Inertial Platform Assembly and converts these signals to a digital number proportional to the electrical rotation of the resolver. It accepts and accumulates incremental velocity inputs from gray code incremental encoders on the platform accelerometers and converts digital signals to analog signals for use in the Flight Control Computer.

The LVDA interface has been standardized as much as possible. Digital inputs and outputs will be 0 and 28 Vdc, except for inputs from the optisyns, telemetry transmitter, and Computer Interface Unit. The signal characteristics, along with the input and output circuits, are listed in Table 15. 5-2.

Table 15. 5-1 Data Adapter Characteristics

Item	Description
Computer input-output rate	512 kHz serial
Power supplies	6 duplexed regulated dc supplies 2 ac resolver power supplies
Switch Selector	8-bit Switch Selector input 15-bit Switch Selector output
Discretes	7 interrupt inputs from the IU 13 discrete outputs 32 discrete inputs
Buffer register Tab register Mode register	26 bits 8 bits 6 bits } Provide communication with the RCA-110 Ground Control Computer, telemetry transmitter, and DDAS
Digital-to-analog converter	8 bits plus sign, 2. 5 millisecond operation, three attitude commands, and two spare outputs
Analog-to-digital converter	Equivalent of 17 bits from a 2-speed resolver
Platform	4 two-speed gimbal angle resolver inputs
Spares	10 single-speed resolver inputs
Delay lines	3 four-channel delay lines for normal operations 1 four-channel delay line for telemetry operations (DOM)
Telemetry	
Command Receiver data transmitter	14 bits for input data 38 data and identification bits plus validity bit and parity bit
Computer Interface Unit	15 bits address plus a data request bit for output data 10 bits for input data plus data ready interrupt
Output to launch computer	41 data and identification bits for output data plus discrete outputs
Input from RCA-110 Ground Control Computer	14 bits for input data plus interrupt
Number of components (estimated)	38,000 silicon semiconductors, cermet resistors, and other special components
Reliability	0. 99 probability of success for 250 hours of operation; uses TMR logic, duplex special circuits, duplex power supplies
Packaging	125 electronic page assemblies, plus special electronic assemblies
Weight	80 kilograms (214 pounds)
Volume	0. 1 cubic meter (3. 6 cubic feet)
Power (without computer)	320 watts

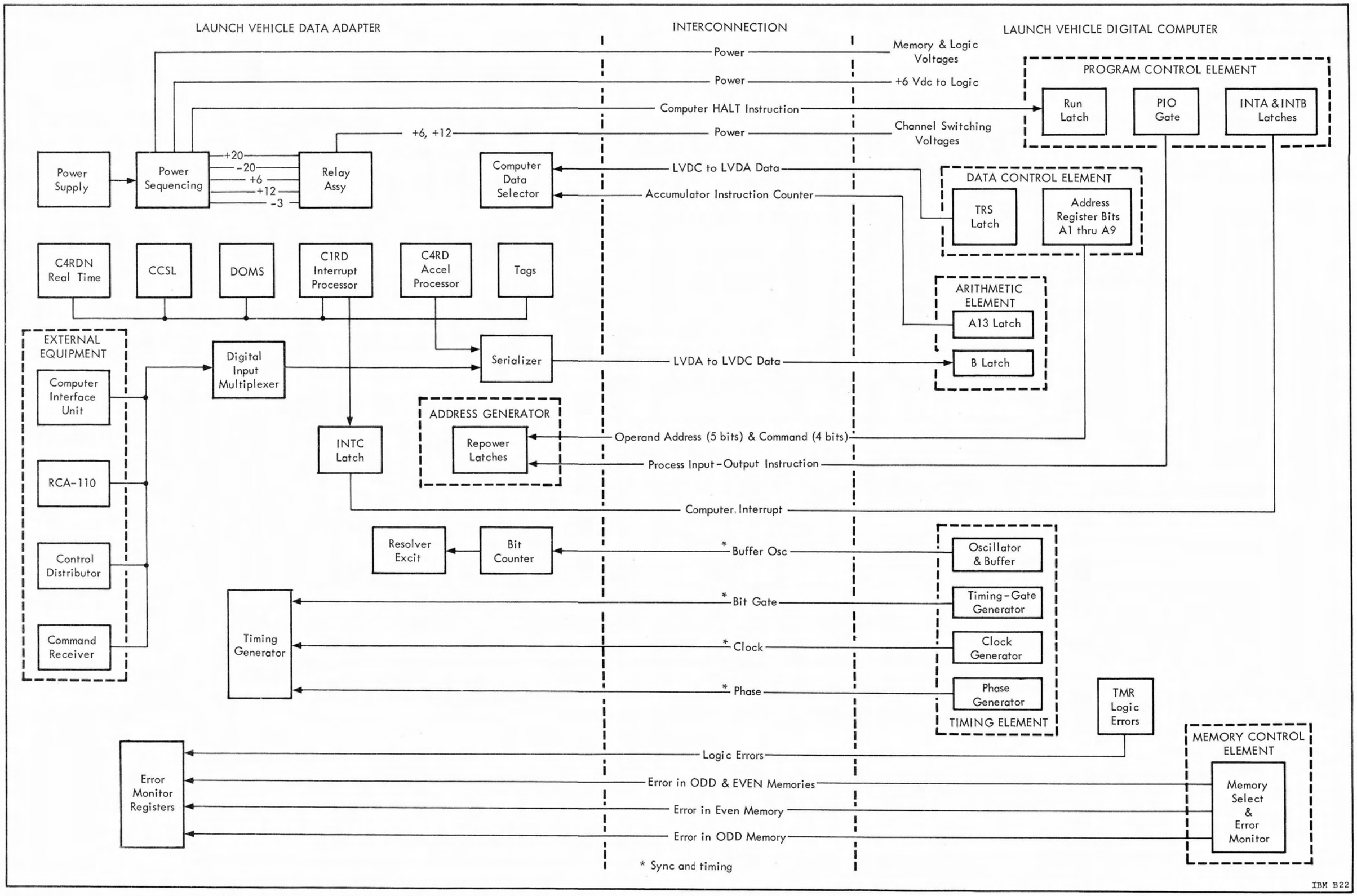


Figure 15.5-1 LVDA-LVDC Interconnection Block Diagram

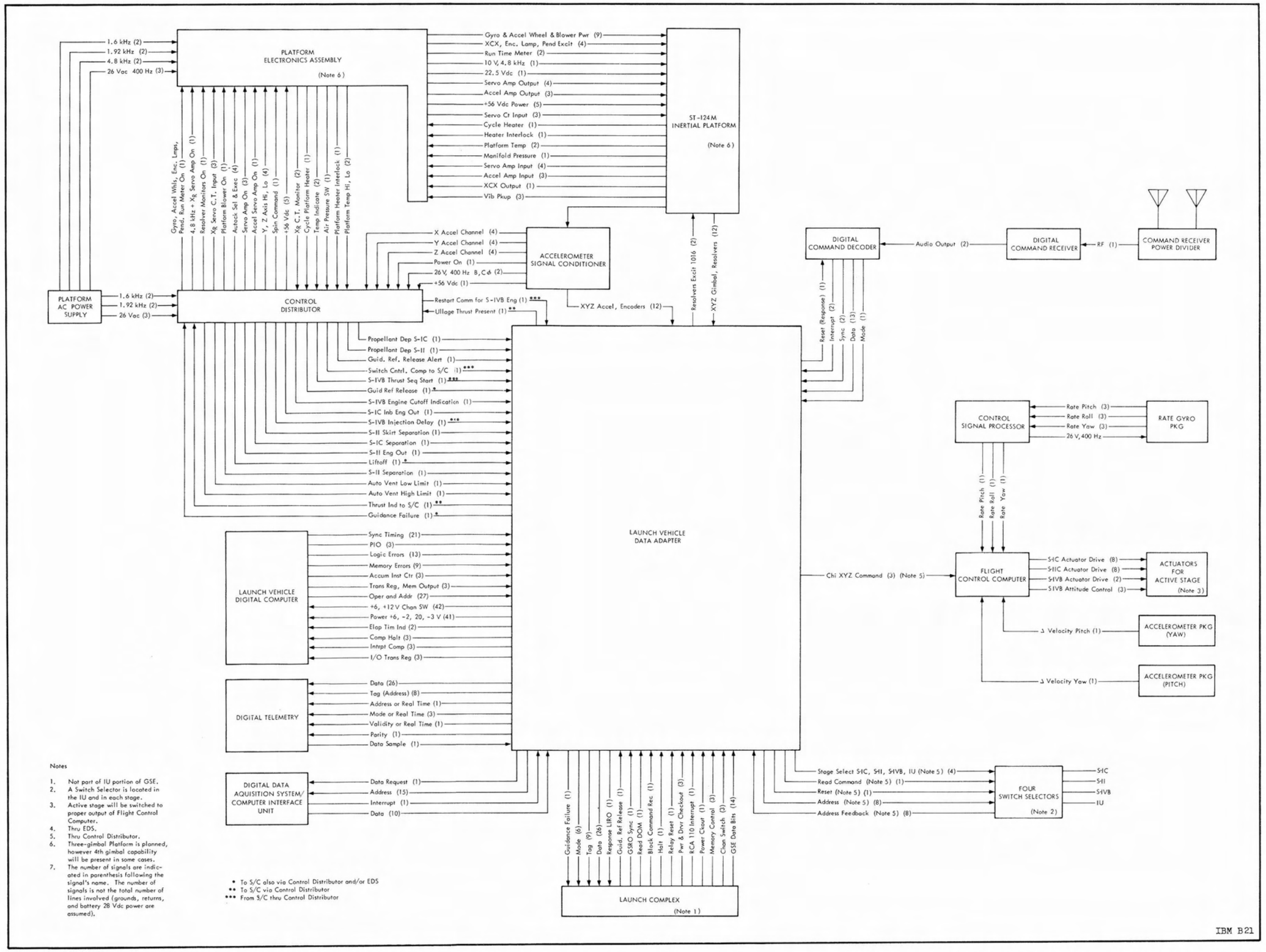


Figure 15. 5-2 LVDA-IU Equipment Interconnection Block Diagram

Table 15. 5-2 Signal Characteristics

Signal Name	Signal Characteristics	Internal Load Impedance (kilohms)	External Load Resistance to Ground	Design Goals	
				Rise	Fall
Resolver excitation	26 V ±5% rms at 1016 cps 12 volt-amps at 0. 9 power factor drive per excitation	17. 3			
Inputs from resolver secondaries	5 V±8% rms at 1016 cps	20. 9			
Ladder outputs	+12. 24 to -12. 24 Vdc		6k (min); < 0. 1 uf		
Inputs from Command Receiver	Down level: 0±8 Vdc* Up level: + 24±8 Vdc	≥10			
Switch Selector feedback	Down level: 0±8 Vdc* Up level: + 24±8 Vdc	≥10			
Inputs from ground computer	Down level: 0±8 Vdc Up level: + 24± 8 Vdc	≥10			
Discrete inputs	Down level: 0±8 Vdc Up level: + 24±8 Vdc	≥10			
Interrupts from IU except DDAS	Down level: 0±8 Vdc * Up level: + 24±8 Vdc	≥10			
Inputs from Computer Interface Unit	Down level: 10 mA="0" Up level: 0± 50 uA="1"	≥ 2			
DOM sync pulse from telemetry	Down level: 0 ± 1 Vdc Up level: 7. 0 ±1. 0 Vdc 100 us duration rep rate 240/s ± 5% evenly spaced	≥10			
Inputs from optisyns	Down level: 0 ±1 Vdc Up level: 7. 0 ±1. 0 Vdc	≥50			
Switch Selector outputs					
Reset and read command drivers	Down level: ** Up level:≥ 21. 5;≤29. 7 Vdc		≥ 75Ω ≤ 0. 045 uf	≤ 0. 1 ms	≤ 1 ms
Stage drivers	Down level: ** Up level: ≥ 21. 5;≤29. 7 Vdc		≥ 122 Ω ≤ 0. 045 uf	≤ 0. 1 ms	≤ 1 ms
Address drivers	Down level: ** Up level: ≥ 22. 5;≤29. 7 Vdc		≥ 270 Ω ≤ 0. 0225 uf	≤ 0. 1 ms	≤ 1 ms
TDL drivers to CIU & telemetry transmitter	Down level: 0±2 Vdc Up level: ≥ 22. 5;≤29. 7 Vdc		≥ 2. 5k≤100k ≤ 0. 005 uf	≤ 5 us	≤ 50 us

Table 15. 5-2 Signal Characteristics (Cont)

Signal Name	Signal Characteristics	Internal Load Impedance (kilohms)	External Load Resistance to Ground	Design Goals	
				Rise	Fall
Command Guidance Decoder	Down level: 0±2 Vdc Up level: ≥22. 5;≤29. 7 Vdc		≥1. 7k ≤ 0. 005 uf		
SDL drivers to telemetry transmitter	Down level: 0±2 Vdc Up level: ≥22. 75;≤29. 7 Vdc		≥1. 5k ≤0. 00375 uf	≤5 us	≤50 us
SDI, SDL, SDH drivers to ground computer	Down level: ** Up level:≥23;≤29. 7 Vdc		SDI≥1. 125 k ≤0. 045 uf SDL≥1. 5k ≤0. 045 uf SDH 300Ω ≤ 0. 045 uf	≤0. 1 ms	≤1 ms
TDM discrete outputs	Down level: ** Up level: ≥21. 5;≤29. 7 Vdc		≥122Ω±10% ≤0. 0375 uf	***	***

* or open.
** Output current at down level is equal to 0 ±100 uA.
*** Not determined.

15.5.3 CIRCUITS AND FUNCTIONS IN THE LVDA

Typical functions performed in the LVDA are the following:

Category I Control data flow, including temporary storage.

Category II Transform data into a form which is compatible with the characteristics of the receiving equipment.

Category III Perform certain simple computational and logical operations on the data.

The following functions are typical of those included in Category I:

- The storage of telemetry data from the LVDC and LVDA in the buffer registers.
- The temporary storage of CIU addresses during orbital checkout.
- The transmission of guidance data from the LVDC to the analog Control Computer.

Operations which require a change in the form of the data include (typical of those in Category II).

- Digital-to-analog, analog-to-digital, and signal level conversions.
- The formation of 40-bit launch computer and telemetry words from 26-bit LVDC words.
- Buffering of communications between the LVDC and the ground-based launch computer to reconcile the difference in clock rates.

The LVDA contributes to the efficient operation of the LVDC by performing many simple, though time-consuming, logical and computational tasks, such as (typical of those functions performed in Category III):

- Keeping track of real time.
- Decoding of operand address in PIO operations.

CIRCUIT DESCRIPTIONS

For the following description of various circuits in the LVDA, refer to Figure 15.5-3.

Delay Lines. The LVDA contains three glass delay lines which serve as temporary storage. The delay lines will be connected together as follows:

- Three delay lines are used in a redundant manner for normal LVDA operation.
- One delay line is used for telemetry operations.

The triple modular redundant delay line is organized around the LVDC timing such that the information it contains remains synchronized with the LVDC operation cycle. The total circulation time of the delay line and its associated electronics is equal to the basic LVDC operation cycle time of 81.9 microseconds (42-bit times). The delay line is divided into three 14-bit word times corresponding to the three LVDC phase times. Furthermore, the four clock times into which each LVDC bit time is divided are used to time-share the delay line among 4 "channels" of 512-kilohertz serial information. Hence, twelve 14-bit words can be stored in a single delay line by operating the line at a 2.048-megahertz rate. Table 15.5-3 illustrates how these word locations are used.

In performing a PIO operation, the LVDC sends out or looks for information only during phase B and C times. Real time is assigned to a phase A word time to facilitate the use of real-time information in the data output multiplexer. However, real time is made available to the LVDC during phase B via the digital input multiplexer register and the serial latch.

The velocity accumulations, which are the processed outputs of the accelerometer optisyns, are arranged to provide duplex redundancy, matching the duplexed optisyns. One line contains outputs X_1 and Y_2, another Y_1 and Z_2, and a third Z_1 and X_2. When the LVDC calls for a given velocity accumulation, it receives the processed output of one of the optisyns on the selected accelerometer during phase B and the outputs of the other optisyns on the same accelerometer during phase C. These 2 values are processed separately in the LVDC such that any one of the delay lines or any optisyn could fail without failing the system.

The real-time accumulation is voted upon in TMR voters during every circulation; thus the values in all 3 lines will always agree. The duplex operation of the accelerometer processors does not allow voting, so there is no guarantee that the absolute value of the 2 readings will agree. Real time is accumulated in 246.1-microsecond increments, while the least significant bit in the velocity measurement has a weight of 0.05 meter per second.

The delay line channels with data written at X (channel 3) and W (channel 2) clock times are used to time two of the functions in the computer program. Both of these functions occur during phase B. Time-to-go until the next LVDC interrupt for Switch Selector operations is counted down in channel 2. Time remaining before the start of the next minor loop is counted down in channel 3. These 2 countdowns occur at a rate of one count every 492.2 microseconds, and will generate an interrupt when they pass through zero. The length of the count will be determined by the LVDC,

Table 15.5-3 Use of Word Locations in the Delay Line

Channel Number	Write Time	Phase Time			Digital Computer Use
		Phase A	Phase B	Phase C	
1	Z clock	Spare	Spare	Interrupt storage	Read channel
2	W clock	Spare	Switch select or interrupt countdown	Interrupt limiting	Write channel
3	X clock	One-millisecond countdown	Minor loop interrupt countdown	Interrupt inhibit	Write channel
4	Y clock	Real-time accumulation	Velocity accumulation X_1 (Y_1, Z_1)	Velocity accumulation Y_2 (Z_2, X_2)	Read channel

which loads a value of time-to-go to initiate each count. Also, during phase A of channel 3, a 0. 8-millisecond delay for use in the digital-to-analog converter is generated by counting 10 circulations of the delay line.

LVDC interrupts are stored during phase C of channel 1. Once the LVDC recognizes an interrupt, it will set the corresponding bit in phase C of channel 2, and will reset this bit in channel 1. The associated circuit will prevent a new interrupt from being recognized in this bit position until the previous interrupt has disappeared. The only constraint, therefore, on the length of the interrupt signal will be that it must last for at least 81. 9 microseconds, the circulation time through the delay line and associated circuits. Interrupts may be stored without being recognized by setting the corresponding bits in phase C of channel 3.

Channel 1 may be conveniently read by the computer, while channel 2 may be conveniently written into from the computer. As many as 3 of the normal 14 bits may be sacrificed if it is desired to use either of these 2 channels in the opposite manner.

Interrupt Register. As a means of notifying the LVDC that immediate attention be given to an external operation, an interrupt line is wired from the LVDA to the LVDC. The interrupt register (delay line) is capable of accepting 12 different signals and storing them until the LVDC has acted upon them. The signals are OR'ed together so that only one interrupt line to the LVDC is required. After an interrupt, the LVDC branches to a subroutine to read the interrupt register by means of a PIO operation. A computer analysis is then made, testing the highest priority bit positions first in case more than one interrupt signal is stored in the register. During this testing, the LVDC stores the contents of the memory address register and the instruction counter and branches to an interrupt subroutine. While in this subroutine, the LVDC does not recognize further interrupts. The next to last instruction of the testing the highest priority bit positions first in case more than one interrupt signal is stored in the register. During this testing, the LVDC does not recognize further interrupts. The next to last instruction of the interrupt subroutine is a PIO instruction addressed to the interrupt register to reset the particular bit causing the interrupt. The hardware provides a time delay to prevent further immediate interrupts from the same source. The source must disappear and return before another interrupt is honored from that source. This prevents slow-acting devices such as relays from regenerating interrupts while they are being activated by discrete outputs which occur during the interrupt subroutine. Each interrupt signal must be at least 84 microseconds in duration to assure storage in the delay line.

The LVDC is also capable of inhibiting the interrupt, as commanded by the program, with PIO instructions whenever the function of the subroutine warrants this precaution. Examples of interrupts are:

- An interrupt which is timed to ensure regular processing of guidance data;
- An interrupt from the CIU indicating that requested data are available.

Nine of the interrupt signals will be generated external to the LVDA and LVDC and three will be generated internal to the LVDA and LVDC.

Interrupt Circuits. The operation of the interrupt circuits is as follows. Upon receipt of an interrupt signal, the LVDA will insert a bit in a time slot reserved for this particular interrupt in a TMR delay line register called the interrupt storage register. When the bit is placed in the register, the LVDA signals the LVDC that an interrupt has been received. Upon receipt of the LVDA interrupt signal, the LVDC will read the interrupt register and determine which interrupt has been received. The LVDC will then insert a bit in the corresponding time slot in another delay line register, called the interrupt limiting register, to indicate that the LVDC has acknowledged that particular interrupt. The logic of the interrupt storage and inhibit registers will be so arranged that once a particular interrupt appears, at the LVDA interface and interrupts the LVDC, it will not be capable of causing another interrupt unless it disappears and reappears again. Another delay line storage register, called the interrupt inhibit register, is provided. When the LVDC places a bit in a particular time slot, this bit will prevent the corresponding bit in the interrupt storage register from interrupting the LVDC. Any combination of bits may be placed in the interrupt inhibit register.

Switch Selector Register. This register is loaded by the LVDC whenever the computer wishes to give commands to specific vehicle devices such as fuel valve controls. The register has a 15-bit storage capacity and is loaded by a PIO instruction. The register thus controls the outputs of 5 Switch Selectors located within the stages of the vehicle. The 15 bits are used as follows:

- Eight bits make up a relay code which is distributed in parallel to each of the 5 Switch Selectors.
- Five bits determine which Switch Selector will be activated (no more than 2 selectors may be addressed at once).
- One bit commands the assigned Switch Selector to activate the device selected by the relay code.
- One bit resets all Switch Selector relays which were turned ON by the previously described bits.

The Switch Selector register contains both TMR and simplex circuits. The characteristics of the outputs are as follows:

- One reset output is TMR.
- One read output is TMR.
- Five stage-select outputs are TMR and capable of driving the stage-select input of one Switch Selector.
- Eight Switch Selector code outputs are simplex and capable of driving simultaneously 2 Switch Selector code inputs.

Switch Selector Feedback Inputs. When the Switch Selectors are operated as previously described, the relay tree feedback lines are tested to assure that the code was set properly by the LVDA. Eight lines from a separate set of contacts on the code relays contain the complement of the data word used to set the code relays. These lines are inputs to the LVDA which do not require storage and are addressed by the LVDA in the same manner as other discrete inputs. This feedback word is separated from the other discrete inputs so that the word may be processed more easily in the computer when comparing it with the word used to "set" the relay code.

Discrete Output Register. Certain functions within the vehicle, excluding those controlled by the Switch Selector register, are controlled by a 13-bit TMR discrete output register. An example of one function, which is controlled by the discrete output register, is a signal to the launch computer.

To ease programming requirements for changing specific discretes while not affecting others, the discrete output register is not loaded in the same way as the other registers. If certain discretes are to be activated, a PIO instruction is set up to address the "set" side of all latches in the register. Conversely, if certain discretes are to be deactivated, another PIO instruction selects the opposite or "reset" side of all latches in the register. The desired bits in the register are changed by placing "ones" in the corresponding bit locations of the data word transferred to the register from the LVDC, while the unchanged bit positions have "zeros" in the data word. Thus, the state of any output may be changed without momentarily or permanently affecting the state of the other outputs.

Buffer Register. The telemetry buffer register is a 26-bit storage register capable of providing 26 outputs in parallel. The register has 11 simplex bits and 15 TMR bits. It will be loaded by LVDC PIO operations or by the LVDA data output multiplexer. The register provides part of the interface required for transferring data to the telemetry data multiplexer and ground computer, and stores addresses for communication with the CIU. The CIU will be driven by the TMR portion of the register. Separate output drivers will be provided for driving the ground support equipment.

The output of the buffer register is provided in parallel to the telemetry multiplexer, the ground computer and the CIU. These systems read data from this register asynchronously with respect to LVDC timing.

Mode Register. The mode register is similar to the buffer register and other 1-word registers loaded by the LVDC. It provides storage for a 6-bit computer word which defines the computer mode of operation. While communicating with the launch computer, these 5 outputs are read in parallel by the launch computer. The telemetry data multiplexer reads three of these outputs when transmitting computer telemetry words, but real-time information data is substituted for these bits when LVDA data is transmitted. A PIO instruction loads the mode register from the LVDC. Three of the bits are loaded into the mode/real time register whenever the LVDC loads telemetry data into the buffer register. All six of the bits are transmitted to the ground computer or other ground support equipment through separate line drivers.

Tag Register. The 8-bit tag register is used to transmit identification bits for data being sent from the buffer register to the ground launch computer and to the telemetry data multiplexer.

Mode/Real-Time Register. The 5-bit mode/real-time register performs the following functions:

- When data is loaded into the buffer register from the LVDC, the mode/real-time register contains one validity bit, three mode bits and one address bit.

- When data is loaded into the buffer register from the LVDA data output multiplexer, the mode/real-time register contains 5 bits from the real time counter in the LVDA (except during time error identification operation at which time it will contain 5-bits from the real time counter). All outputs of this register are transmitted to the telemetry data multiplexer. The real-time/address bit is transmitted to the ground launch computer.

Validity Bit Generator. Since the telemetry data multiplexer addresses the LVDA asynchronously with respect to LVDC timing, it is possible for telemetry words to be read while they are being changed by PIO operations. However, data read at this time are invalid. Therefore, a signal must be included in the telemetry word which indicates the validity of the word. The validity bit generator performs this function. Data are invalid any time the computer mode register, tag register, and buffer register are being loaded.

The validity bit generator is a 1-bit simplex register which is turned ON whenever LVDC telemetry data is being loaded into the buffer register. This bit shares a bit position in the mode/real-time register with one of the real-time bits.

Data Request Generator. The LVDA has a 1-bit TMR data request generator as an output to the CIU. The presence of this bit informs the CIU that an address for it is in the buffer register. The bit is turned OFF by an interrupt from the CIU.

Parity Generator. To ensure that LVDC data sent out over the radio frequency telemetry link to ground equipment is received without error, a parity bit is included in each 40-bit data word sent out by the LVDA.

The telemetry data word is formed from 3 subwords plus a validity bit. The validity bit however, is not included in the parity check. Odd parity is used. This means that, excluding the validity bit, all the "ones" in the 3 subwords, plus the parity bit, add up to an odd number. The easiest way to generate total parity is to generate an individual parity bit for each subword. The three parity bits are then checked for total parity and a resultant parity bit is generated.

Ready-Bit Generator. During orbital checkout, the computer examines various parameters which are monitored by the telemetry system. The LVDC obtains one of these inputs by sending a CIU address to the buffer register. This 15-bit address is compared in the CIU address comparator. When comparison occurs, the telemetry word is stored in a 10-bit register which is read by the LVDA. Another line interrupts the LVDC to notify it that data are available.

Since the buffer register is continuously connected to the CIU address comparator, as well as the telemetry data multiplexer and the launch computer interface, it is necessary to indicate to the address comparator when the buffer register data are ready for comparison. This is the function of the ready-bit generator. The "ready-bit" is turned ON after the 15-bit address is loaded into the buffer register, under control of a special PIO instruction. The bit remains ON until after the address has been compared and the 10-bit data word has been stored; it is turned OFF by the line causing the computer interrupt.

Error Monitor Register. The error monitor register is a simplex register for storing disagreements between the inputs to the various voters in the LVDC and LVDA. It also stores some disagreements between the duplex circuits. The LVDA has the capability of addressing this register upon command from the LVDC through the data input multiplexer and telemetering it through the data output multiplexer. This register contains 26 bits.

Time-Error Identification. To ensure proper error identification, the computer program location, bit time, word time, and the source of error are telemetered.

Address Generator. During PIO operations, the LVDC must select a register in the LVDA which contains or receives the input-output data. The address of the selected register and the correct data are determined by the operand bits of the instruction word along with the PIO control lines from the computer. These functions are performed by the address generator. The address generator is TMR and decodes nine address lines from the LVDC upon receipt of a PIO instruction. The decoded address selects a register, or other circuit in the LVDA that the LVDC desires to send data to or receive data from.

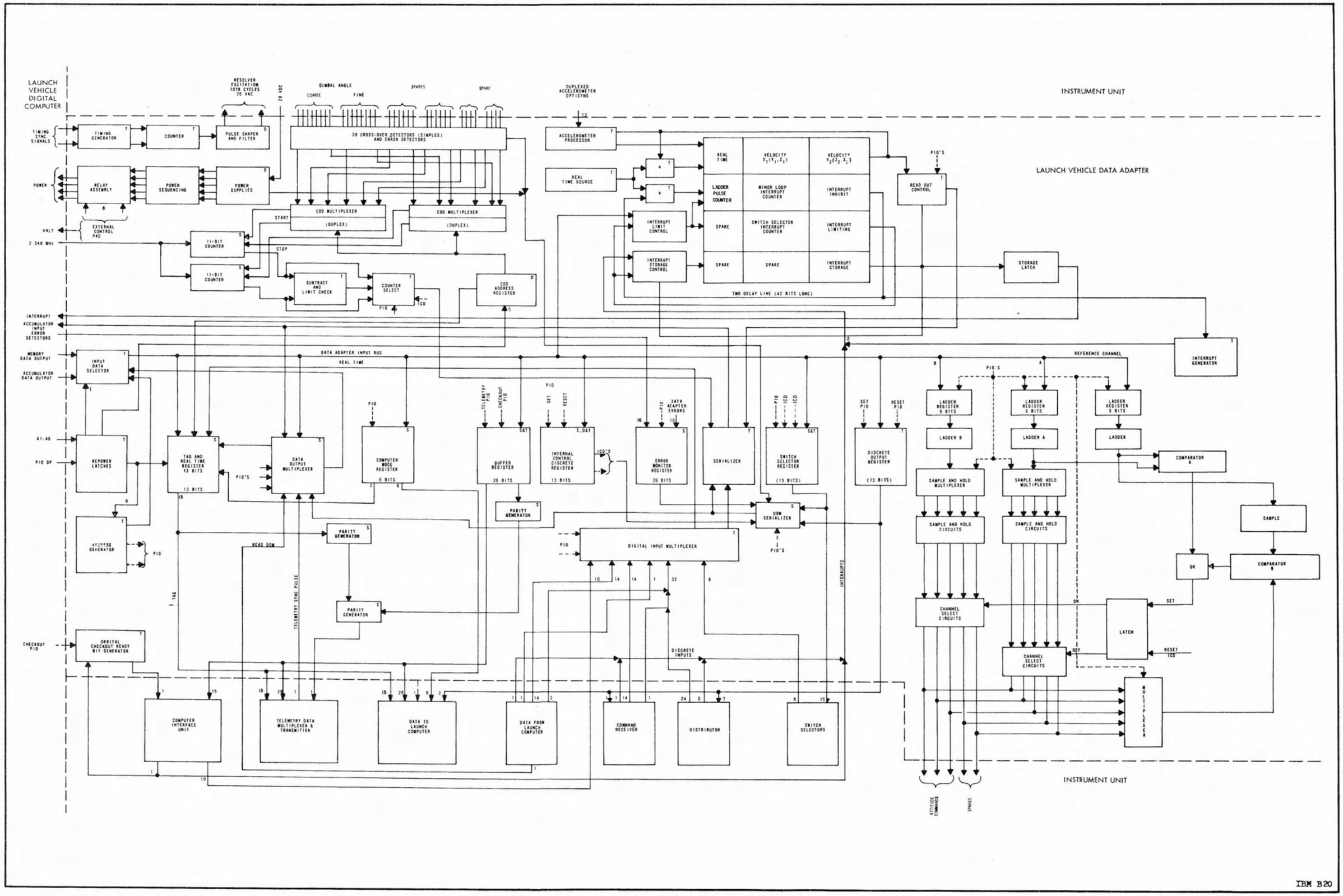


Figure 15.5-3 Launch Vehicle Data Adapter Block Diagram

Timing Generator. The timing generator is TMR and generates timing gates for the LVDA circuits as follows:

- Each word time is approximately 82 microseconds in duration and is divided into three phase times of equal duration.
- Each phase time is approximately 27.3 microseconds in duration and is subdivided into 14-bit times of equal duration. The subdivision is accomplished by eight timing gates.
- Each bit time is approximately 1.95 microseconds duration and is subdivided into four equal clock times of 0.488 microsecond duration.

The timing generator receives four clock pulses, one bit gate, and one phase gate per TMR channel, as synchronizing signals from the LVDC.

Internal Control Discrete Register. Certain functions within the LVDA must be controlled by the LVDC. A 13-bit register, very similar to the discrete output register, is included to provide these controls.

Some of the functions of these discretes are:

- Control switching of duplex delay line channels.
- Selection of the duplex analog output channels to be used.
- Selection of coarse resolvers as backup of fine resolvers.

This register is so constructed that the state of any output can be changed without momentarily or permanently affecting the state of the other outputs.

Discrete Inputs. Discrete inputs are signals which do not require storage within the LVDA. The LVDA is designed to handle 32 of these inputs. The LVDC reads the discretes periodically and performs the necessary program steps.

Examples of discretes are:

- A signal from the Control Distributor indicating vehicle stage separation.
- A signal from the Spacecraft indicating a command to start the thrust sequence of the S-IVB Stage.

The discrete signals will be read in through the digital input multiplexer which is TMR. Groups of these discrete inputs are treated as words by the LVDC – one 24-bit word and one 8-bit word. Each word is read by the LVDC as requested by a PIO address.

Digital Input Multiplexer and Serializer. The digital input multiplexer accepts and serializes parallel digital input words. The word that is to be serialized will be selected by a PIO command from the LVDC. The selection of the word is determined by the configuration of the nine address bits accompanying the PIO instruction from the LVDC. The input selected is serialized at a 512-kilohertz rate and is fed to the LVDC accumulator.

The digital input multiplexer is connected with the following equipment:

Computer Interface Unit
Ground Computer
Control Distributor
EDS Distributor
Command Guidance Receiver
Switch Selectors

The digital input multiplexer also provides temporary storage of real time and gating signals from the TMR delay line and the crossover detector counters to the LVDC accumulator.

Channel Switching. To check the individual channels within the TMR logic sections of the LVDC and the LVDA, both in the laboratory and on the launching pad, a means of evaluating each channel separately will be provided. The channel-switching function will be under the control of external ground support equipment or the laboratory test equipment. Signal lines from this control equipment will operate the LVDA relays, which control bias voltages on the 3 channels of voters in the LVDC and LVDA, allowing TMR or simplex operation.

15.5.4 POWER SUPPLIES

The LVDA contains six duplexed dc power supplies and one pair of ac resolver supplies. It can tolerate supply voltage transients of ±50 volts, 1 millisecond half-period duration.

The pulse-width modulated duplex power supplies provide regulated dc power to the LVDA and LVDC by means of a dc-to-dc converter, from the vehicle +28 Vdc supplies.

An example of a duplex redundant power supply is shown in Figure 15. 5-4. Two regulated power supplies are connected in parallel. In each power supply, two feedback amplifiers are used in a duplex arrangement because they have the lowest reliability of the circuit. If one of the amplifiers fails, the isolation diodes allow the parallel amplifier to continue the regulation of the power converter. To further increase reliability, dc-to-dc power converters in the same duplex supply are connected to different +28 Vdc vehicle supplies. This allows one +28 Vdc vehicle supply to fail without a duplex supply failure. The regulated voltage supplies are: one +20 Vdc supply, one +12 Vdc supply, two +6 Vdc supplies, one -3 Vdc supply, and one -20 Vdc supply.

The ac power supply generates a well-filtered sine wave for excitation of various resolvers in the IU. The 1016-hertz frequency needed to drive the resolvers is obtained by counting down from computer timing pulses. This is accomplished with a 3-stage ring counter followed by a latch.

A variable clipper controls the amplitude of the 1016-hertz square wave obtained from the counter. The clipping level is set by level-sensing detector-amplifier circuitry. The fundamental component of the square wave is obtained by filtering, and is amplified to a 26-volt level which is adequate to drive the resolvers. The 26-volt level is maintained by an amplitude sensitive feedback circuit. The harmonic content is reduced by filtering. This filtering is accomplished by incorporating frequency selective feedback techniques in the amplifier circuitry.

The resolver frequency source is duplexed in a sense, i. e., each source supplies power for half of the resolver inputs in such a manner that fine and coarse resolver excitation for any input parameter is not supplied by the same source. Since fine and coarse inputs serve as a backup for each other (under the proper program control), duplex redundancy is used for the excitation source.

Associated with the power supplies are controls to:

- Provide channel switching (method of selecting one of the TMR channels for checkout) in the LVDA and LVDC.
- Provide power sequencing where required under ground equipment control.

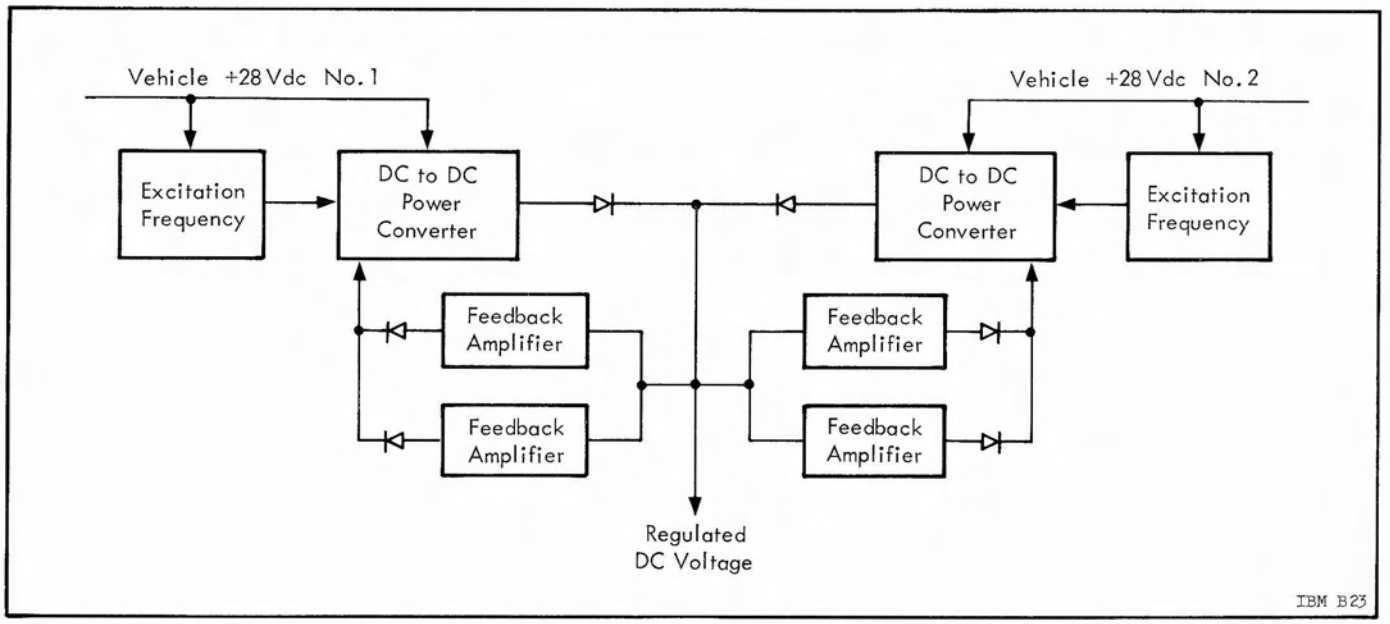


Figure 15.5-4 Redundant Power Supply Block Diagram