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DESIGN CONCEPTS OF GROUND DDAS IN SATURN 1B/V ESE

BY

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ABSTRACT

In the Saturn IB/V programs the sheer quantity of data required for computer processing and ESE display makes it necessary to provide an efficient data aquisition system. For much of the data originating in the launcher this requirement is satisfied by the Ground Digital Data Acquisition System (DDAS). This paper provides a technical description of the Ground DDAS with emphasis placed on the unique design concepts of this telemetry system.

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DESIGN CONCEPTS OF GROUND DDAS IN SATURN IB/V ESE

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The size and complexity of the Saturn IB/V systems place new and demanding requirements on the Electrical Support Equipment (ESE) design. The amount of information that must be acquired, processed, and evaluated prior to vehicle launch is so great that partially automated ESE is necessary. In order for the ESE to function effectively, it must have access to vast quantities of current and accurate data. This requirement has been satisfied by the Ground Digital Data Acquisition System (DDAS) which allows the myriad of analog and discrete data originating in the launcher to be made available for real-time computer processing and Launch Control Center display.

This paper provides a technical description of the Ground DDAS with emphasis placed on its unique design concepts. It should be noted that the DDAS is an extremely flexible telemetry system that can be adapted to numerous applications. However, this paper only covers the aspects of the system as they apply to the Ground DDAS.

Description of Ground DDAS

The Ground DDAS transmits analog and discrete data from the launcher to the Launch Control Center (LCC) for computer processing and ESE display, refer to Figure 23. All discrete inputs to the Ground DDAS Transmitter are recorded for post flight analysis by the Digital Events Evaluator. Analog signals, which do not have the characteristics required by the transmitter are converted by the Analog Signal Conditioner to acceptable transmitter inputs. The analog and discrete inputs are sequentially scanned by the transmitter and the data formatted into a 72 kilohertz (kHz) pulse code modulated wavetrain. This digital wavetrain frequency modulates a 600 kHz carrier and is routed to the Line Driver for distribution to the Digital Receiving Station (DRS) in the launcher and transmission to the DRS in the

LCC via video cable. The PCM/FM signal is received by the Line Receiver in the LCC where it is demodulated and routed to the LCC DRS. Both the launcher and the LCC DRS's demultiplex the signal and makes the reconstructed data available to the Computer Interface memory where it is continously updated as new data becomes available. The computer has instantaneous access to any data stored in Computer Interface, which is the prime data source used by the computer for pre-launch checkout. The DRS's also convert the digital data to analog and discrete signals, which are proportional to their associated transmitter inputs. These signals are made available to the ESE for display and recording.

Ground DDAS Discrete Inputs

Discrete signal inputs to the Ground DDAS are derived from the stage ESE, the Instrument Unit (IU) ESE, the power ESE, and the launch equipment. The launch equipment provides its own signal distribution, therefore, these discretes can be routed to the Discrete Patch Distributor for distribution to the Ground DDAS Transmitter and Digital Events Evaluator (DEE) for recording. The Discrete Patch Distributor provides versatility in assigning telemetry and DEE channels by means of jumpers within the distributor.

Figure 1 illustrates a typical discrete input to the Ground DDAS. A discrete is made available to the transmitter when an ESE relay energizes applying a positive voltage to the base of the input transistor. The emitters of all discrete input transistors are connected to Single Point Ground via a 500 MCM cable which provides the return path for all discretes to their power sources. This common return for all discrete inputs to the transmitter is required for compatibility with the DEE.

Ground DDAS Analog Inputs

Analog signal inputs to the Ground DDAS originate from the same sources as the discretes. These signals are routed to the Analog Patch Distributor for distribution to the Analog Signal Conditioner

or Ground DDAS Transmitter. The Analog Patch Distributor is similar to the Discrete Patch Distributor and allows selection of telemetry channels and signal conditioners.

Certain Analog Signals are compatable with the Ground DDAS Transmitter and, therefore, do not require signal conditioning. These signals are routed directly from the distributor to the transmitter. However, most analog signals do not have the characteristics required by the Ground DDAS Transmitter and must be routed to the transmitter through the Analog Signal Conditioner.

ANALOG SIGNAL CONDITIONER

The Analog Signal Conditioner converts the analog signals into proportional voltages in the range of 0 to 5v dc and references them to the same ground potential as the transmitter, refer to Figure 2. These are the characteristics required for all analog input signals to the transmitter. In addition the Analog Signal Conditioner provides a means of remotely verifying the proper operation of the Ground DDAS. Figure 20 is a photograph of the Analog Signal Conditioner installed at the Saturn V System Development Breadboard Facility.

DC Magnetic Amplifier

The essential feature of each DC conditioning circuit in the Analog Signal Conditioner is an extremely linear and stable differential DC magnetic amplifier. The amplifier selected for this application has undergone extensive testing, which indicates that the following accuracies can be expected:

Linearity 0.02%

Gain Stability 0.20%

Null Stability 0.01%

Ripple and Nosie . . . . . less than 1.5mv p/p

No long term gain or null drift could be detected.

Common Mode Rejection

The DC magnetic amplifier provides the necessary amplification for low level signals and rejection of common mode signals. A common mode signal is one which is present on both input lines of the amplifier and contains no pertinent information. An example of common mode rejection is the measurement of dc current, as shown in Figure 3.

The current measurement is made across a 50 millivolt (mv) shunt in the positive output of a power supply.

The pertinent signal information is the 50mv between 27.950 and 28.000v dc, which is amplified and referenced to ground. The common mode signal is between 0 and 29.950v dc and is rejected by the amplifier. The rejection of common mode signals also eliminates ground potential differences between the signal return and the transmitter's analog signal common which is referenced directly to Single Point Ground via a 500 MCM cable. This arrangement eliminates inaccuracies due to variations in ground potentials and insures an extremely stable ground reference for the transmitter. Input noise is dampened out by the very low response, approximately 2 Hz, of the amplifier.

Gain Adjustment

The gain range of the magnetic amplifier used in the Analog Signal Conditioner is varied by limiting the current in its input control winding with series resistance, which is provided by R_g in Figure 4.

For a maximum output of 5v dc, an input of 50 microamps (μa) to the control winding is required. The selection of Gain Resistor, R_g, is determined by the maximum input voltage, $E_{in}(Max)$; e.g. when $E_{in}(Max)$ = 50mv dc

$$R_g = \frac{50 \times 10^{-3}}{50 \times 10^{-6}} = 1000 \text{ ohms}$$

Similarily when $E_{in}(Max)$ = 100v dc

$$R_g = \frac{100}{50 \times 10^{-6}} = 2 \text{ megohms}$$

Zero Offset

For signals which can have both positive and negative values, the amplifier zero can be offset by an auxiliary control winding. This winding can be biased so that the maximum negative input does not cause the output to go negative as illustrated in Figure 5.

Expanded Scale

Many analog signals are required to be displayed on expanded scale meters, i.e. meters which are scaled for only a portion of the signal's range. The 28v dc

power supply voltage is an example of an expanded scale measurement. The supply's automatic voltage protection does not allow it to drop below 20v dc or rise above 40v dc. Therefore, only the range between 20 and 40v dc is of interest. Figure 6 illustrates a typical expanded scale conditioning circuit in the Analog Signal Conditioner.

With E_{in} at the minimum expanded scale voltage, the zener is selected to break down at a lesser voltage, and the divider can be adjusted for zero differential input to the amplifier. The maximum expanded scale voltage is obtained by adjusting the amplifier gain. Figure 7 illustrates the characteristic curve for this circuit.

Verification

The verification circuit shown in figure 8 allows a calibrated reference voltage to be substituted for the analog signal for remotely verifying the Ground DDAS channels.

At low signal levels conventional dry contact relays exhibit contact resistance in excess of 1000 ohms which would result in severe loading errors. To prevent such errors, mercury-wetted relays whose contacts are kept wet with mercury by capillary action, are used in the low level verification circuits. The resulting contact resistance is negligible at low signal levels.

GROUND DDAS TRANSMITTER

The Ground DDAS Transmitter consists of rack mounted components identical to those used in the vehicle, see Figure 21. It sequentially scans the analog and discrete inputs and formats this data into a 72 kHz pulse code modulated wavetrain. This digital wavetrain in turn frequency modulates a 600 kHz carrier for transmission to the LCC. Figure 9 is a functional block diagram of the Ground DDAS Transmitter.

Analog Multiplexer

The two Analog Multiplexers accept analog signals of 0 to 5v dc from the ESE or Analog Signal Conditioners. These many independent signals are combined on a non-interfering basis into a serial wavetrain. The serialization is accomplished by commutating, i.e. sequentially sampling, the multiple inputs of continuous analog data to produce a series of pulses whose amplitudes represent the levels of the successive inputs at the time of sampling. This operation is known as time division multiplexing and results in a pulse amplitude modulated waveform.

Figure 10 is a simplified representation of time division multiplexing. Each input level is briefly sampled and becomes part of the single output. The Analog Multiplexer in the Ground DDAS Transmitter employs highly reliable solid state selection switches which are controlled by binary counters. The timing circuits can operate from an internal clock, but in the Ground DDAS Transmitter, they are synchronized by the Pulse Code Modulator. The selection switches or gates sequentially connect the analog inputs to the output of the multiplexers on commands from the timing curcuits. The timing circuits provide the signals that open and close the data gates at the desired times and in the desired sequence. In the Analog Multiplexer twenty-seven of the thirty primary channels are data channels while the remaining three are utilized for amplitude reference and PAM frame identification. Twenty-three of the data channels are sub-multiplexed to provide 230 data channels, which are sampled at 12 sample per second (sps).

The remaining four data channels cannot be sub-multiplexed internally; and, therefore, are utilized as 120 sps channels.

Discrete Multiplexer

The Discrete Multiplexers in the Ground DDAS Transmitter recognize discrete input signals of approximately 0 to 9v dc as logic "0's" and 21 to 36v dc as logic "1's". These multiplexers increase the digital data handling capability of the Pulse Code Modulator. Each multiplexer can accept up to 100 discrete inputs, which are sequentially sampled in groups of ten. This arrangement results in ten data groups each consisting of ten discretes that provide the PCM with ten digital words of ten bits each. The sampling sequence and rate, 4 or 12 sps, are controlled by timing signals from the modulator.

Pulse Code Modulator

Figure 11 is a functional block diagram of the Pulse Code Modulator. In a programmed sequence, the PAM scanner combines the PAM wavetrains of the two analog multiplexers into a single output PAM wavetrain. The analog to digital converter (ADC) encodes the PAM wavetrain into a parallel 10-bit digital word by the successive approximation method. Since the operation of the ADC is non-synchronous, the digital word is stored in a parallel data register until required. The digital multiplexing and formatting logic combines the ADC digital words, the Discrete Multiplexers digital words, and the frame identification codes into a serial output format. This 72 kHz data signal frequency modulates the 600 kHz voltage controlled oscillator (VCO) for transmission to the LCC.

The clock, programming, and timing logic provide all timing signals required by the modulator as well as timing signals required to synchronize the Analog and Discrete Multiplexers.

Line Driver/Line Receiver

The Line Driver accepts the PCM/FM signal from the

Ground DDAS Transmitter and provides two outputs. One output is a demodulated PCM digital wavetrain, which is routed to the DRS in the launcher. The other output is the original PCM/FM signal, which is amplified for transmission via twin video cables to the Line Receiver in the LCC. Both the input and output of the Line Driver can be remotely monitored. The Line Receiver provides the proper termination for the video cable and demodulates the PCM/FM signal for the LCC DRS.

MULTIPLEXED DATA FORMAT

Figure 12 is a mechanical analogy of the electronic multiplexers in the Ground DDAS Transmitter. The rotary switches shown in Figure 12 represent the counters in the Analog Multiplexer and Pulse Code Modulator with the switch positions corresponding to the number of steps for each of these counters. Referring to Figure 13, the two position switch is analogous to the ÷2 group counter, the 30-position switch is analogous to the ÷30 channel counter, the 10-position switch is analogous to the ÷10 frame counter, and the three position switch is analogous to the ÷3 mux scan counter. All three contacts of the mux scan switch are tied together to indicate that the same data is sampled into all three of the multiplexer time slots. Other ten-position switches should be arranged around the two large switches, but for simplicity, they are not shown.

Figure 13 is a block diagram showing the multiplexer counters. Each counter after stepping through its full count, sends a stepping pulse to the next counter causing it to step one count. Consequently, the group counter steps one count for every tenth count of the word length counter. Similarly, the channel counter steps one count for every twentieth count of the word length counter. The frame counter and mux scan counter step one count for each thirtieth count of the channel counter. The gated counter outputs control the multiplexers, which provide a data format identical to the one produced by the mechanical analog of Figure 12.

Figure 14 is a sampling sequence chart showing the various time slots. The word counter continually counts off ten-bit words at 72 kilobits/second. During each count of ten, all other counters remain in the same position and allow all ten bits of a word to originate from the same source. These ten bits may be ten separate discrete signals or they may be a digital word which represents a sample of an analog signal.

The mechanical analogy in Figure 12 consists of two groups of commutators; i.e. multiplexers. One is called Group A (GPA) and the other is called Group B (GPB). The group counter, a ÷2 counter, continually selects one and then the other multiplexer making a change at the end of each ten-bit word.

Each multiplexer commutates thirty points called channels. Since the channel counters step on every other count of the group counter, they remain on the same count while both multiplexer groups are being sampled; i.e., if the channel counters are on 1, they are sampled as GPA.CH1, GPB.CH1; then both channel counters step to 2 to give GPA.CH2, GPB.CH2, etc.

Channels 1 through 23 each provide 10 sampling points called frames. It should be noted that a sampling cycle discussed later is also customarily called a FRAME. The sampling cycle FRAME is spelled in upper case letters to differentiate it from the sampling points described as frames. The frame counter is stepped one count for each thirtieth count of the channel counter so, if the frame counter is in the first frame for the first thirty channels, etc.

In the Saturn IB/V format, three multiplexer time slots per group are employed. These are referred to as Mux 1, Mux 2, and Mux 3 and are controlled by the mux scan counter, a ÷3 counter. However, in the actual hardware only one multiplexer per group is used and it is called Mux 0 with the understanding that any one sample is commutated into all three multiplexer time slots. Since the frame and mux counters step at the same rate, but have different counts, their relationship is as shown in Figure 14. Any given combination of frame time slots and multiplexer time slots is repeated once for each 30 FRAME time slots. A FRAME occupies 30 channel time slots (one revolution of the commutator) and a MASTER FRAME consists of 30 FRAMES.

As stated previously, the bit rate is 72 kilobits/second or one bit per 13.9 microseconds. The time

required between steps of the timer channel is 20 X 13.9 microseconds or 278 microseconds to allow for the group switch to interlace 10 bits from each of two groups. The commutators step around the 30 channels in 30 X 278 microseconds or 8.34 milliseconds, which is one FRAME time. If a transducer output is sampled directly from a channel, i.e., from an address consisting of GP CH (group and channel), it is sampled once each FRAME, i.e., one sample per 8.34 milliseconds or 120 samples per second. Similarly, if the transducer is sampled from a channel containing frames, the same frame occurs once every 10 FRAMES, see frame row of Figure 14, resulting in 1 sample per 83.40 milliseconds or 12 samples per second. If three multiplexers per group were used and a transducer output were commutated by only one of them, the sampling rate would be reduced to 1/3. With one multiplexer per group, a measurement is actually being sampled in every multiplexer time slot to provide the 12 or 120 samples/second. Thus, a 12 samples/second measurement might occupy the following time slots:

GPA.CH19.FR2.MUX1. GPA.CH19.FR2.MUX2, and GPA.CH19.FR2.MUX3

As can be seen from Figure 14, these frame and multiplexer combinations occur every tenth FRAME. Similarly, a 120 samples/second measurement occupies all frame time slots in addition to all mux time slots. If an increase in sample rate is desired, a transducer must be connected to more than one sampling point. In any event all 900 sampling points are sampled during a MASTER FRAME or approximately every ½ second.

Channels 23, 25, 26, and 27 are not sub-multiplexed due to the physical limitations of the equipment; therefore, any measurement introduced on these channels occupies all 10 frame time slots associated with one of these channels. Channels 28, 29, and 30 are used for introducing calibrate voltages and FRAME and MASTER FRAME sync codes in the two groups as labelled in Figure 12. A transducer output voltage can be

sampled at any point except channels 28, 29, and 30 and the PAM sample quantized to an equivalent 10-bit binary PCM code. Each of the 10 frames associated with a particular channel may be sub-multiplexed further into 10 sampling points. These points are actually part of the discrete sub-multiplexer, but can be programmed into time slots such as shown in Figure 12 and used for discrete measurements. Since any frame occupies 10 bit times through digitizing of the sample when any frame is sub-multiplexed into 10 sampling points (bits), each bit is programmed into the format without digitizing. The Group A and B switch serves to interlace the Group A and B 10-bit word times. If this diagram were completely representative of the actual equipment, the interlaced group PAM signals would be coupled to the Pulse Code Modulator for digitizing into 10-bit words per group.

During the first nine frames of Channel 28 in both groups, a 0v level is sampled and converted to a 10-bit binary code to provide a zero level calibrate word. Every tenth frame a 5v level is sampled and digitized to provide the complement of the zero level calibrate word. This sample is called the full scale calibration, and since it occurs every tenth frame, it can be used for tenth frame identification during multiplexer test. The 5v level sampled during frame 10 is provided by a precision voltage source that receives its input from the same source from which the analog multiplexer develops its internal voltage. In practice the two ten-bit calibrate words are offset from all 0's and all 1's to provide transitions for the receiving equipment to synchronize on.

All ten frames of channels 29 and 30 in both groups are connected to a 5v source. The samples which are taken during channel 29 group A are coded into a 10-bit word but the receiver logic is such that these samples are not used. During channel 29 group B and channel 30 groups A and B, FRAMES 1 through 29, the transmitter inserts a total of thirty bits in a certain combination of 1's and 0's which comprise

three FRAME sync words. On FRAME 30 these bits are complimented to form the three MASTER FRAME sync words. The next count after the last MASTER FRAME sync word is GPA.CH1.FR1.MUX1, which starts a new multiplexing cycle. Therefore, by recognizing a MASTER FRAME sync code, identical counters in the receiving station can be set to this address and so begin counting in synchronism with the counter in the transmitter.

DIGITAL RECEIVING STATION

The 72 kilobit per second serial wavetrain derived in the Ground DDAS Transmitter is routed from the Line Receiver to one of two inputs to the Digital Receiving Station (DRS). The other input is connected to either the tape recorder or simulator.

A photograph of the Digital Receiving Station is shown in Figure 22 and a functional block diagram is shown in Figure 15. Referring to Figure 15, the input stages of the synchronizer operate on the demodulated wavetrain from the Line Receiver to provide a clean, stable data pulse train which is applied to the first stage of a 40-bit serial shift register. This pulse train is also used by a phase-lock loop in the synchronizer to generate a 72 kilobit rate clock that is in synchronism with the data pulse train. The bit rate clock is used to step the serial data pulse train bit by bit through the 40-bit serial shift register. It is also used to clock the address counters which are the same as the address counters in the transmitter.

Synchronization of Address Counters

After the 40-bits have been shifted into the shift register, the first 30 of these bits are examined in the FRAME and MASTER FRAME sync correlation filter for correlation with a predetermined code. This correlation established the presence of either the FRAME or MASTER FRAME sync code from the transmitter. Accordingly, an output pulse is produced when either the FRAME or the MASTER FRAME code is present. This action occurs at only one clock time. On the next clock time a new bit is shifted into the first stage of the register and all other bits are shifted to the next stage. In order to insure that the sync signal is genuine, the system passes through several sync modes before final synchronization (FRAME or MASTER FRAME Lock) is reached.

When the first FRAME sync code is detected, the resulting pulse causes the sync reset logic to generate a sync reset pulse which sets the address counters to

a GPA.CH1 address. The Frame and Mux Counters remain in the same state as before sync reset, which places the address counter in a configuration equivalent to the beginning of any one of the 30 FRAME counts. At this time, the system is placed in the FRAME sync acquisition mode. The Channel Counter then counts thirty counts during which time 600 bits are shifted through the shift register placing the next 30-bit sync code in position for correlation. If FRAME sync correlation occurs, the system is switched from the FRAME sync acquisition mode to the probation mode. By this time the address counter has returned normally to a GPA.CH1 count and the Frame and Mux Counters fall into whatever count they are in their cycle. On the third FRAME sync reset pulse, the system is switched to the FRAME lock mode and the address counter begins another cycle starting at a count of GPA.CH1 and the existing frame and mux count.

If a sync indication is not received at the proper time, the system is returned to a prior mode; the selection of which depends on the present mode. The modes can then advance again as described above. As long as FRAME sync reset pulses keep occuring at the expected time (i.e. at GPB.CH30 time), the system remains in the FRAME lock mode. In the FRAME lock mode the receiving station address counter is in FRAME synchronism with the transmitter but may be shifted by any number of FRAMES from synchronism with the MASTER FRAME.

Absolute synchronism is achieved in the MASTER FRAME Lock mode. In this mode, the correlation of the MASTER FRAME sync code with the preset code in the correlation filter causes a pulse on the MASTER FRAME sync line. This pulse is used by the reset logic to provide a sync reset pulse to the address counter causing the Frame and Mux Counters to be set to a count of one. Since the Group and Channel Counters have now counted to GPA.CH1 because of FRAME synchronization having been achieved, and the Frame and Mux Counters have been set to one; the receiver senses that the transmitter counter is beginning a count in FRAME 1. The receiving station then begins its count in FRAME 1, stepping count by count with the clock which is synchronized

with the transmitter data bits. If 30 FRAMES later, another MASTER FRAME sync pulse occurs, the receiving station is placed in the MASTER FRAME lock mode.

With the system in both FRAME and MASTER FRAME lock, the out-of-sync signal to the data valid section is cut off. If the other inputs to data valid indicate that certain other functions are within tolerance, a data valid signal is generated.

Outputs to ESE

After every 10 bits a data word from the next address has been shifted into the first 10-bit section of the shift register and the previous words have been shifted into the next sections. The bit rate clock causes these words to be set into the 10-bit parallel register. Thus, at each word time, the 10-bit data word from the next address is set into the register. These data words are made available to data registers and digital to analog converters. Each data register consists of eight 10-bit registers, and each D-A converter has a capacity for converting up to fifty 10-bit (only the 9 MSB are used) data words to corresponding analog voltages. To expand the capability, several data register and D-A converters can be driven from the same 10-bit parallel register.

The output of the 10-bit parallel register is coupled to all eight registers of the data register and all converters of the D-A converter. Thus, data from all addresses is made available to each portion of the data register and D-A converter. Through the use of a data switch any one portion of these devices responds to data from only one address.

The input to the data switch is derived from decoded counts from the address counter. Therefore, there are 30 channel inputs to the data switch. One input is used to indicate a channel 1 count, another a channel 2 count etc. The data switch logic combines these counts so as to provide a pulse (called a transfer pulse) each time a certain count (address) appears at its input. A data switch has patching capability

to provide a pulse for each of 64 different addresses. Fifty of these pulses are provided to a D-A converter and 8 are provided to a data register.

After a 10-bit word has been clocked into the first section of the serial shift register, it is in turn set into the 10-bit parallel register. At the same time the decoded address from which the data was derived appears at the input to the data switch. If the data switch has been patched to respond to this address, a transfer pulse results causing the 10-bit word either to be set into that register of the data register to which the transfer pulse is wired or to be converted into a corrsponding analog voltage by the D-A converter to which the transfer pulse has been wired. Normally, transfer pulses to data registers are derived from addresses which are assigned to discrete data (that is, RDSM's) rather than analog data. It is noted that even though less than 10 discretes may be assigned to a particular address, all 10 stages of an individual register of a data register must still be used for that address, thereby, "wasting" the unused stages.

Figure 16 illustrates a typical discrete output signal from the Digital Receiving Station to the ESE. Discrete signals are transmitted as individual bits within the digital wavetrain at a repetition rate of 4 or 12 samples/second. A flip-flop holds the discrete as a fixed level and provides an output from the DRS of OVDC for a logic "0" and -12VDC for a logic "1". The discrete signal conditioner amplifies the -12VDC signal to drive a relay which provides a contact closure to the ESE.

The discrete signal conditioner is required (1) to prevent loading the DRS discrete output signals (2) to convert these signals to levels compatible with the ESE, and (3) to provide isolation between the DRS and ESE.

The sampled and digitized data from multiplexer addresses selected by the data switch are converted to a 0 to 10-volt analog voltage by the D-A converters. These analog voltages are provided to the ESE for

display on meters for status monitoring or to analog recorders. Each group of 50 analog voltage outputs is provided with a reference voltage output for calibrating the meter or recorder to null out the voltage drop caused by line resistance between the D-A converters and the displays.

Calibration and Sync Error Verification

As each bit enters the serial shift register, it is coupled serially to the calibration and sync error verification logic. Here, during the proper intervals, the bits are compared bit by bit with internally generated codes to determine if any errors in the calibratibration and sync words are within tolerance. The words are examined at the proper times by means of pulses, which occur at time slots CH28 FR1 through 9 for zero level calibration verification; CH28.FR10 for full-scale calibration verification; and GPA.CH29 for verification of the sync words, which occur during GPB.CH29, GPA.CH30 and GPB.CH30. These times are derived from decoded address counts provided by the counter decoder. Once the system is in FRAME and MASTER FRAME lock, it is certain that incoming bits being examined during these times are the codes rather than data. If the calibration codes are out of tolerance (that is, not within a few millivolts of nominal equivalent voltage), a calibration error pulse is generated and a warning lamp is lit. If either sync or calibration verification is not realized, a signal is anded in the data valid logic with the out-of-sync signal from the sync reset logic to prevent a data valid signal from being sent to the computer via the computer interface unit. Thus, if the system is not in FRAME and MASTER FRAME lock, the computer is notified by means of the data valid output, that the data which it is receiving could be from a transducer at an address different from the address indicated. Further, if the FRAME and MASTER FRAME sync codes are sufficiently within the threshold tolerance, but not in exact correlation, the computer is notified by means of data valid that the data it is receiving may not be valid for reasons such as noise or wrong address. In addition, if the system is in FRAME and MASTER FRAME lock and the calibration voltage errors are out of

tolerance, the computer is notified by data valid that the data which it is receiving is not calibrated. Data valid does not indicate to the computer which of the causes is generating the invalid data effect.

Outputs to the Computer Interface Unit

Assuming that the MASTER FRAME sync code is occupying its proper place in the register for correlation, the data bits in the input section of the serial shift register are from the GPA.CH1.FRI.MUX1 address. At this time, if correlation is accomplished, the resulting sync reset sets the address counter to the above address. Twenty bit times later the data associated with this address has been shifted down to occupy the third section of the serial shift register. At this time the second section of the register is occupied by data from the address GPB.CH1.FRI.MUX1. Thus the middle section of the register is occupied by data from CH1 in both groups. At this point a data transfer pulse is generated. The pulse is used to set the 40 bit data portion of the output register to transfer the 40 bits of data contained in the serial shift register and set the 11-bit address portion of the output register to the address indicated (CH1.FR1.MUX1, in this instance) by channel, frame, and mux stages of the address counter. The data transfer pulse is also coupled to the Computer Interface Unit to indicate that new data is available at the output register.

After the output register has been set, and 278 microseconds after the address counter is set to the beginning of the CH1 count, the address counter reaches a CH2 count. The cycle then repeats every 278 microseconds. Data that is in the first two sections of the shift register at the time of one transfer pulse has been shifted into the last two sections of the shift register at the time of the next transfer pulse. Therefore, the same data appears at the output of the output register (although in different locations) during two transfer pulse times.

The 14-bit address coupled to the Computer Interface

consists of the selection of any one of the eight different combinations of bits provided by three 2-position switches, plus five channel bits, four frame bits, and two mux bits. The switch selections identify the source of the data and must be different from the combination provided by any other output register providing data to the same computer interface. These bits are generally called memory section address bits. The total address is then specified by 14 address bits.

COMPUTER INTERFACE UNIT

Referring to Figure 17, the Computer Interface Unit (CIU) may be conveniently thought of as being divided into two parts; the read side and the write side. On the write side it interfaces with output registers of the DRS or Telemetry Checkout Station. The CIU has eight input connectors to provide a capability of individually handling up to eight digital receiving stations. On the read side, the CIU is compatible with the Input/Output Data Channel (IODC) of the RCA-110 Computer.

The Computer Interface is essentially a storage device that periodically receives and stores data from the DRS's. On command from the computer, the data is read into the computer.

Write Side

Eight source selection gating pulses are generated in the gate generation logic by internal timing. It proved convenient to make these pulses 20 microseconds wide, and since each is sequential with respect to the pulse for the previous source, the pulse train for each source has a period of 160 microseconds. These pulses are asynchronous with respect to the transfer pulse from a specific source.

The transfer pulse from a source is effectively stored until the next occurence of the gating pulse assigned to the source. At this time, a 20-microsecond sample of each of the 54 bits at the input to the source selection gates is gated in parallel through the source selection gates. Depending upon the time relationship between transfer pulses and gating pulses, the gating can occur as soon as approximately 20 microseconds following the transfer pulse or as late as 160 microseconds. Each input will be sampled once every 278 microseconds and samples can occur between 160 microseconds and 320 microseconds apart.

Additional logic in the gate generation function provides a write strobe (WS) output on a single line. This

gating pulse is 1.25 microseconds wide and occurs just before the end of the 20 microsecond long gated input. With eight input sources being scanned, a WS will be generated every 20 microseconds during a scan of the eight sources. The 1.25 microsecond sample of the parallel data and address bits will then be gated through to their respective inputs at the memory information register (MIR) and memory address register (MAR). The WS input to the memory serves to initiate timing within the memory in order to write the data into the memory at the location specified by the address.

It should be noted that there are 900 possible combinations of channel, frame, and mux addresses for each source. For eight sources there will be 7200 address locations. These locations can be described by the combinations of 13 bits (2^{13} = 8192 combinations). Thus, the write address lines (WAL) must be reduced from 14 to 13 before being set into the MAR. This operation (address code conversion) is only suggested in the block diagram. This also applies to the read address lines (RAL).

Read Side

On the read side, the Computer Interface will operate in three modes; single channel repeat, block transfer, and sequential on the basis of receiving mode control signals from the computer.

With a single channel repeat mode control signal at the input to the read control logic and a new read address signal from the computer, the bits on the read address lines (RAL) specifying the address from which the computer desires a readout, will be set into the memory section register and read address counters. The new read address signal will also be processed by the Computer Interface and sent back to the IODC to indicate that it has been received. The new read address signal also permits the Computer Interface to recognize a change to another mode as desired by the computer.

When the continuously changing (every 278 microseconds) write address becomes the same as the stored read

address (as seen at the input to the compare logic), the WS that gates the write address in will cause a compare (CMP) signal to be generated, thereby indicating a good comparison. The CMP signal is coupled to the read control logic to generate an R_o signal, providing the computer has send a read request, which indicates that the Computer Interface is in a read cycle. With the computer interface in a read cycle, a read strobe (RS) will be generated on timing such that it can occur no sooner than approximately five microseconds after the write strobe.

The read strobe will initiate a sequence of events in the memory, which includes setting the read address into the MAR and causing a data read out from this address. Thus, immediately following the loading of data into an address, the data can be read out of the address. A load output register (LOR) signal will be sent to the output register from the read control logic to set the 40-bit readout of the memory into the output register. This signal is generated on timing on receipt of the R_o signal and is timed to occur approximately four microseconds after the RS signal. This occurence of LOR is then well outside the memory acess time.

The LOR signal causes a data ready (DAR) signal to be sent to the computer to notify it that the request data is ready for readout. It should be noted that up to 0.25 seconds can be taken between a read request and actual availability of the data to the computer. This is the time required for a complete scan (MASTER FRAME) by the multiplexers. The computer's read request signal is also turned off by DAR in preparation for a new read request. The DAR signal also returns the R_o signal to its original level, thereby placing the computer interface out of the read cycle. Data will continue to be read out of the same memory address with each read request and good comparison.

The data in the output register is made available to the computer as two 10-bit words at a time. Either set of the two 20-bit sets is made available to the computer, depending on the state of the group selection voltage from the computer.

The sequential mode is similar to the single channel repeat mode except that a trigger is generated in the read control logic to step the read address counter by an amount determined by the counter sequence control signals from the computer. The counter will step only when the output register has been loaded. The address from which the readout occurs is that specified by the read address counter. The counter trigger is generated from a read request and a good comparison is not required. Therefore, the computer can sequentially scan the memory without regard to obtaining latest data.

The block transfer mode is similar to the sequential mode in that the address counter advances by an amount determined by the counter sequence control signals; however, a good comparison is required for the trigger to be generated. Thus, any data made available to the computer will be new data. This mode differs from the signle channel repeat mode in that the read address continuously changes due to stepping of the read address counter.

In either the sequential or block transfer modes of operation, the Computer Interface read address counter can step in the normal, 10-frame advance, or 30-frame advance sub-modes depending on computer instructions on the counter sequence control lines. In all sub-modes, the counter trigger described above is still used to clock the counters. In the normal sequence the read address counter will step through a channel, frame, and mux count in the same manner as the counter in the DRS or transmitter. In the 10-frame advance sequence the configuration of the read address counter is changed so that the frame and mux counters are driven from the same trigger and the channel counter is driven from the overflow of the frame counter. Thus, the channel count advances on every frame 10 count. In the 30-frame advance sequence, the channel counter is advanced once on each frame 10 mux 3 count.

Memory

A core memory, see Figure 19, of the random access, coincident current type is ued in the Computer Interface. It consists of 64 cores per line arranged in 128 parallel

lines in a core plane for a total of 8192 cores in a plane. Forty-eight planes are included in two stacks with a total of 40 planes (one per bit) being used. Each of the eight sources, which can be coupled to the Computer Interface is assigned to a section (labeled "memory sections" in Figure 18). All forty-eight planes are considered to be a part of each memory section, with all of the 64 cores in a line and 16 of the 128 lines being allocated per section for a total of 1024 cores per plane in one memory section. Thus, there are 1024 possible locations in which to store the 40-data bits from 900 multiplexer addresses.

As shown in Figure 19, bits of a word are stored in cores arranged along the vertical axis in four groups of 10 bits each. Channels are assigned in two 32-bit strings for a total of all 64 cores in a line. Even numbered frames and all muxs are assigned to one 32-bit wide area and odd numbered frames and all muxs are assigned to the other half. The 40-bit core string allocated to a specific address may be determined from the illustration. For example, an address of FR2MUX1CH19 is on the MUX 1 section slightly more than 1/3 of the distance across the core stack as measured from the far side. All Channel 19 addresses for even numbered frames are illustrated in the cut-away section. The FR2MUX1CH19 address is the emphasized vertical string in the front of the stack. Data sampled at 12 samples per second would be located not only on this string but also on the other two emphasized strings in the MUX 2 and MUX 3 areas. Data from the Group A and B multiplexers is stored in two sections each as indicated in the illustration. Thus, data from a GPA multiplexer is stored in 10-core vertical lines at the top and just below the center of the core stack. This data is duplicate data and is not stored as a result of successive sampling at the multiplexer, but because of multiplexer formatting and DRS operation caused by the shifting of data in the 40-bit shift register and setting of the DRS output register every second word time.

A simplified functional block diagram of the core memory logic is shown in Figure 18. Due to a control voltage supplied by the computer interface proper, the memory system operates in the clear/write and read/restore modes.

A WS signal places the memory in the clear/write mode. In this mode, a specific core in each of the 40 planes is selected by the half-select current in the X and Y drive windings in each plane on the basis of the state of the MAR. Depending on the state of the core before it is switched to the "0" state by the half-select current, a voltage from the core sense (readout) winding may appear at the input to the associated read amplifier. The read amplifier is disabled during the clear/write mode. The core readout, then, will not be passed through the read amplifiers, and, therefore, the readout will be destructive.

All 40 selected cores will now be set to the "0" state and will be ready to be loaded with data. The write data will be set into the MIR, and the resultant output will cause write drive current from the digit drivers to flow in the digit winding of all cores in a plane if the state of the MIR is "0". At the same time half-select current will flow in the opposite direction in the X and Y drive windings to set the cores to the "1" state if no current flows in the digit windings due to the MIR being set to the "1" state. If the MIR has been set to "0", current will flow in the digit winding with the resulting magnetic field opposing the field caused by the current in the drive windings allowing the core to remain in the "0" state. Thus, by means of a destructive readout, the cores will be cleared and made ready for a write.

The operation is somewhat the same during the read/restore mode. In this mode the proper cores are selected by the read address and the MIR is reset to the "0" state by a reset pulse resulting from the read strobe. When the readout is made from a core through the read amplifiers, the MIR can be set. The resulting output appears on the data readout lines to the computer interface output register. The MIR output is also sensed by the write (digit) drivers and the same data is written back into the cores to restore them to their initial state.

Both modes require approximately 4 microseconds. Therefore, logic in the computer interface prevents an RS and a WS from occuring any closer than 4 microseconds

(actually about 5 microseconds) apart for a case where a core is written into and then read immediately. In addition, the LOR signal is prevented from occuring less than 4 microseconds after an RS to permit the memory to cycle through a read sequence before loading the output register with the memory readout.

DISCRETE INPUT

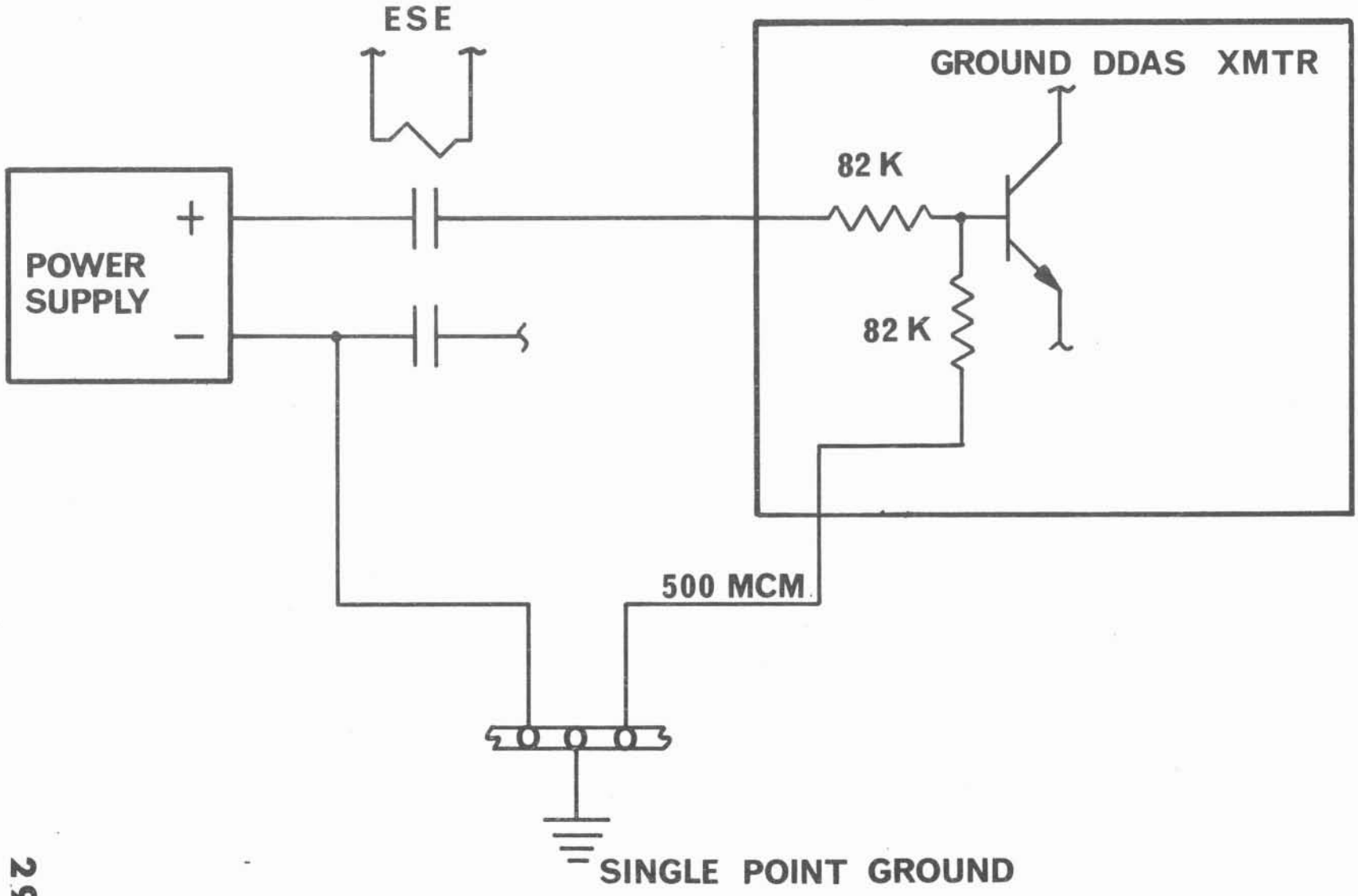


FIGURE 1

ANALOG SIGNAL CONDITIONER

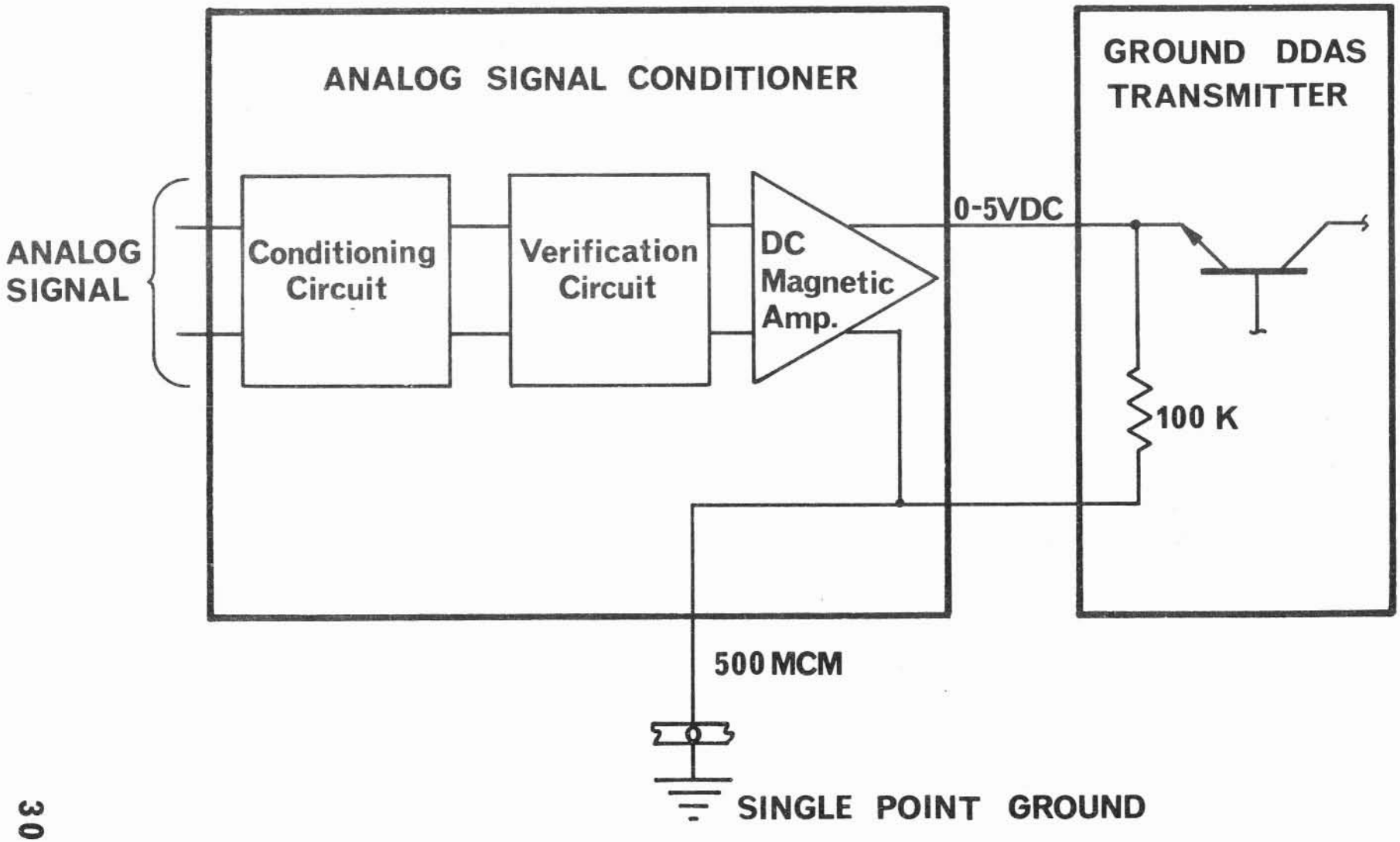


FIGURE 2

DC CURRENT MEASUREMENT

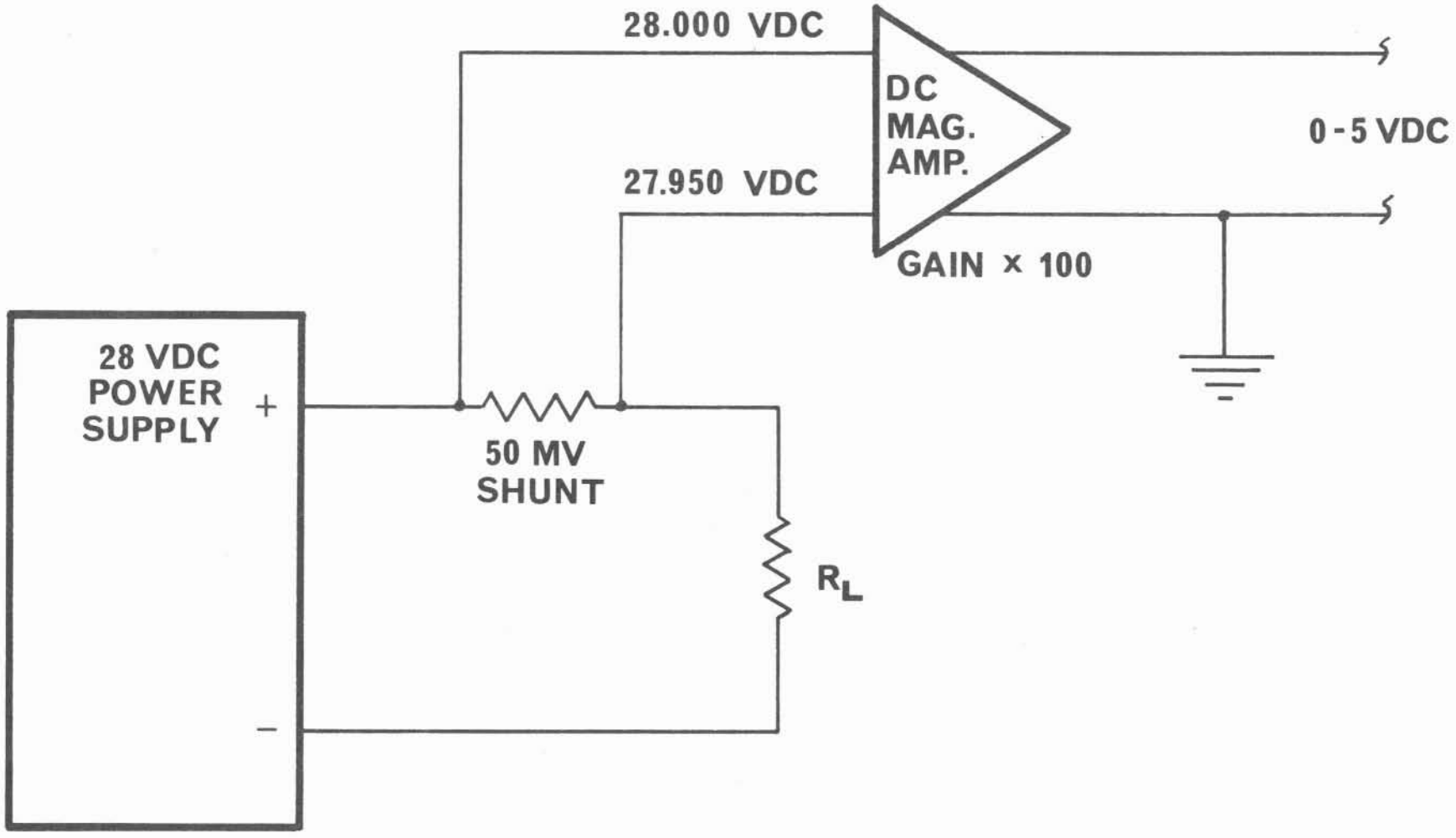


FIGURE 3

MAGNETIC AMPLIFIER GAIN CONTROL

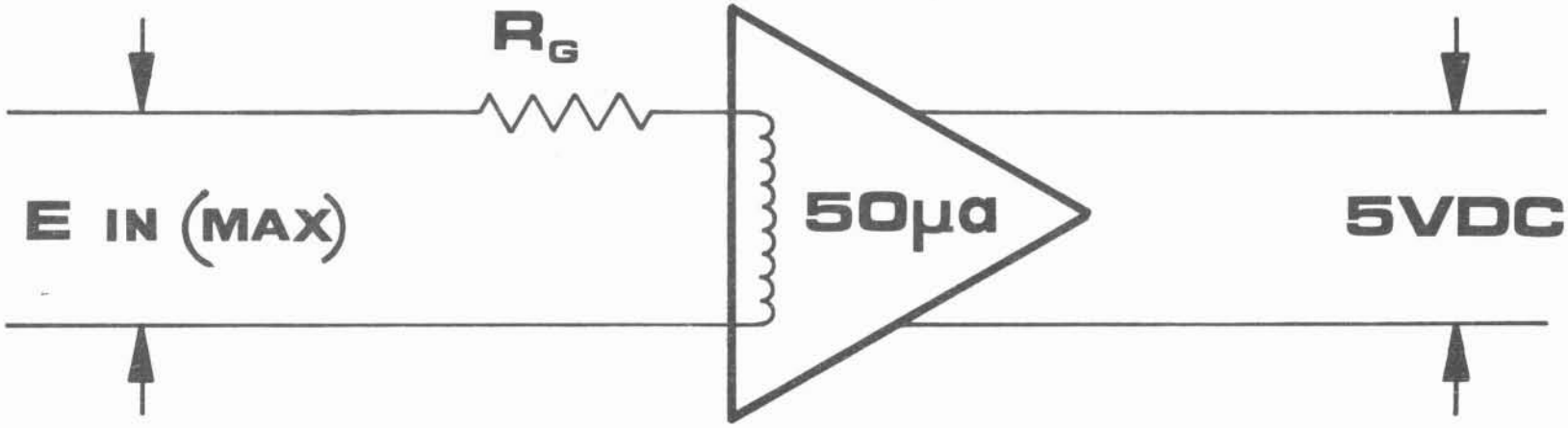


FIGURE 4

ZERO OFFSET CHARACTERISTIC CURVE

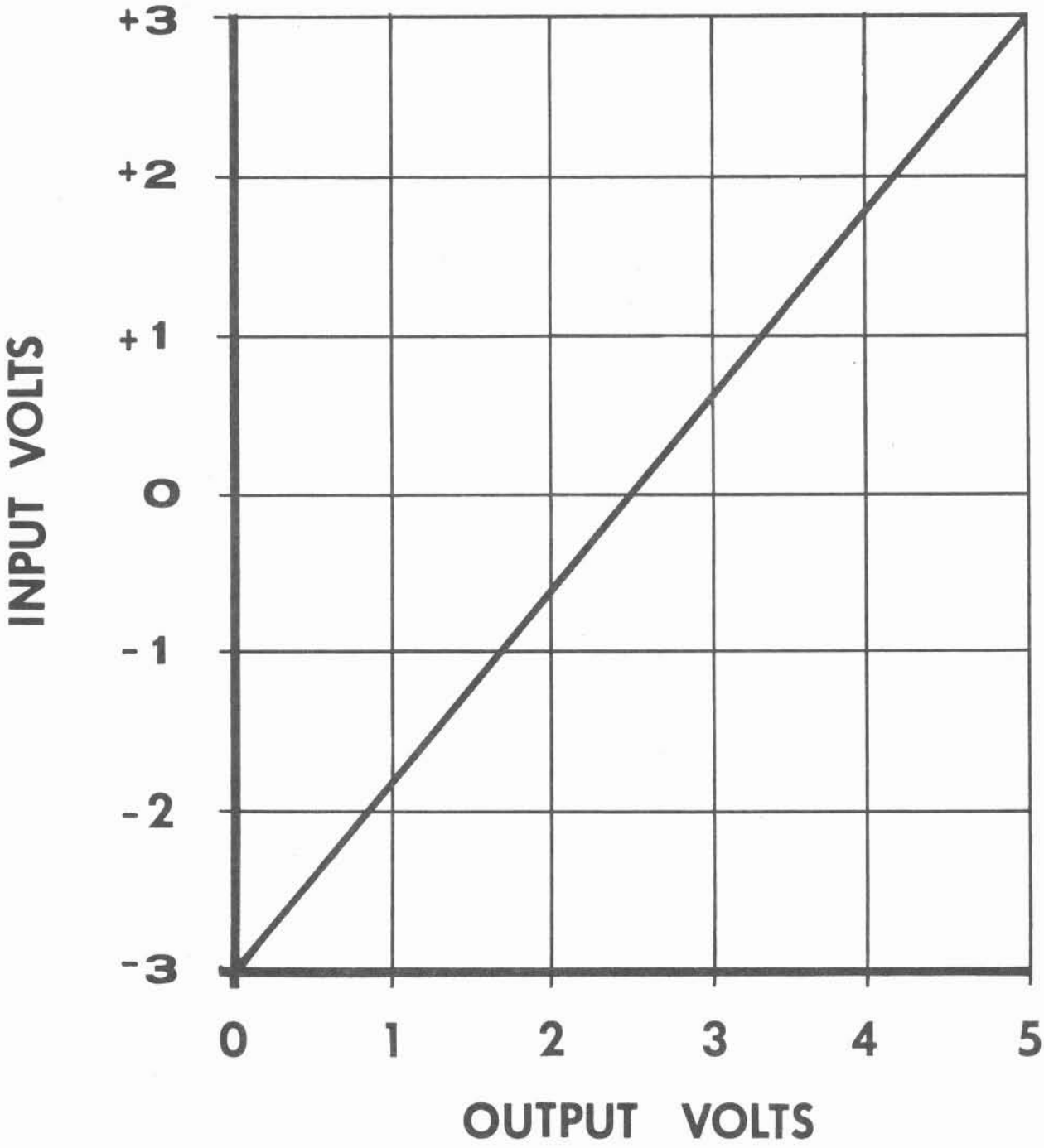


FIGURE 5

EXPANDED SCALE CONDITIONING CIRCUIT

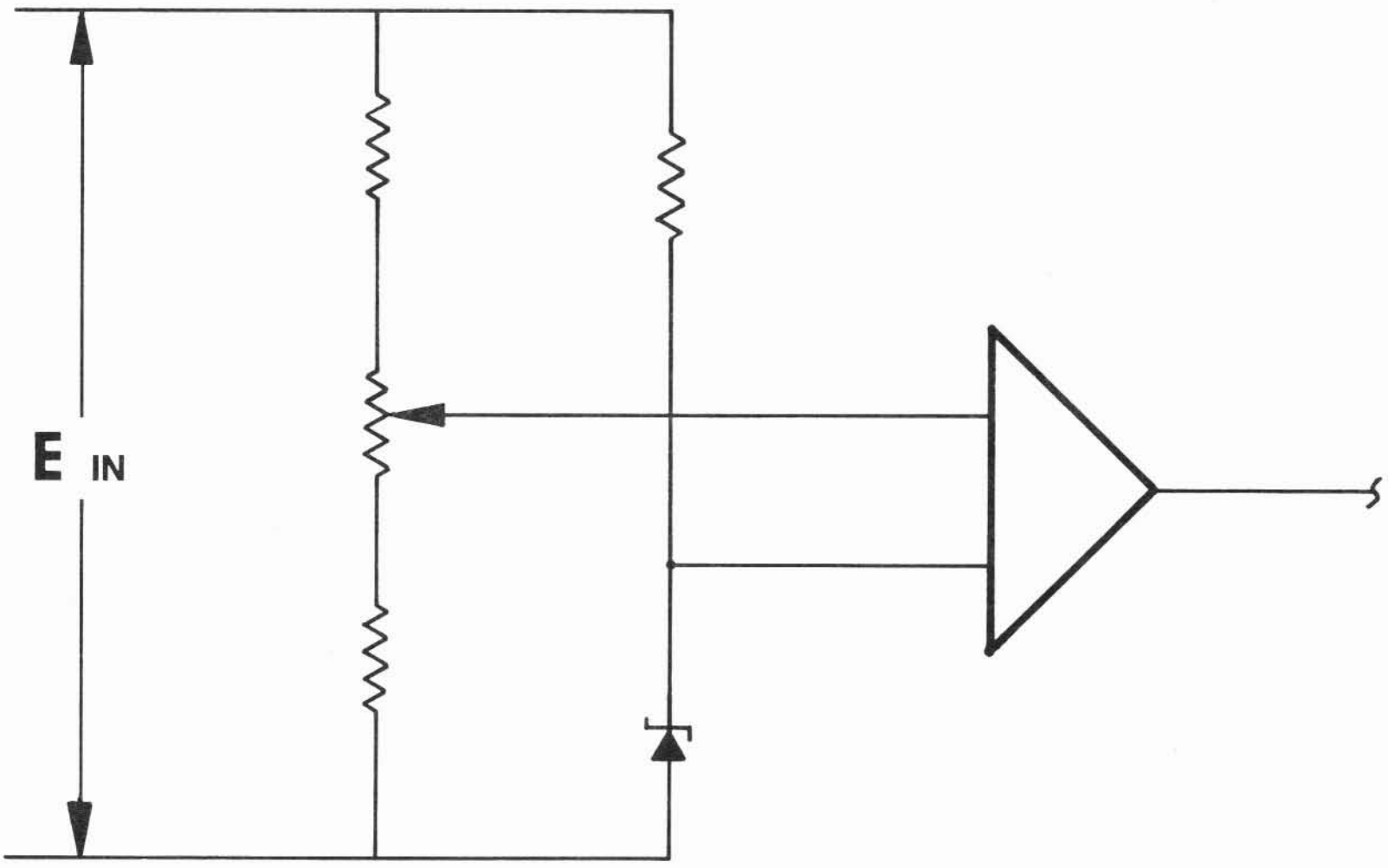


FIGURE 6

EXPANDED SCALE CHARACTERISTIC CURVE

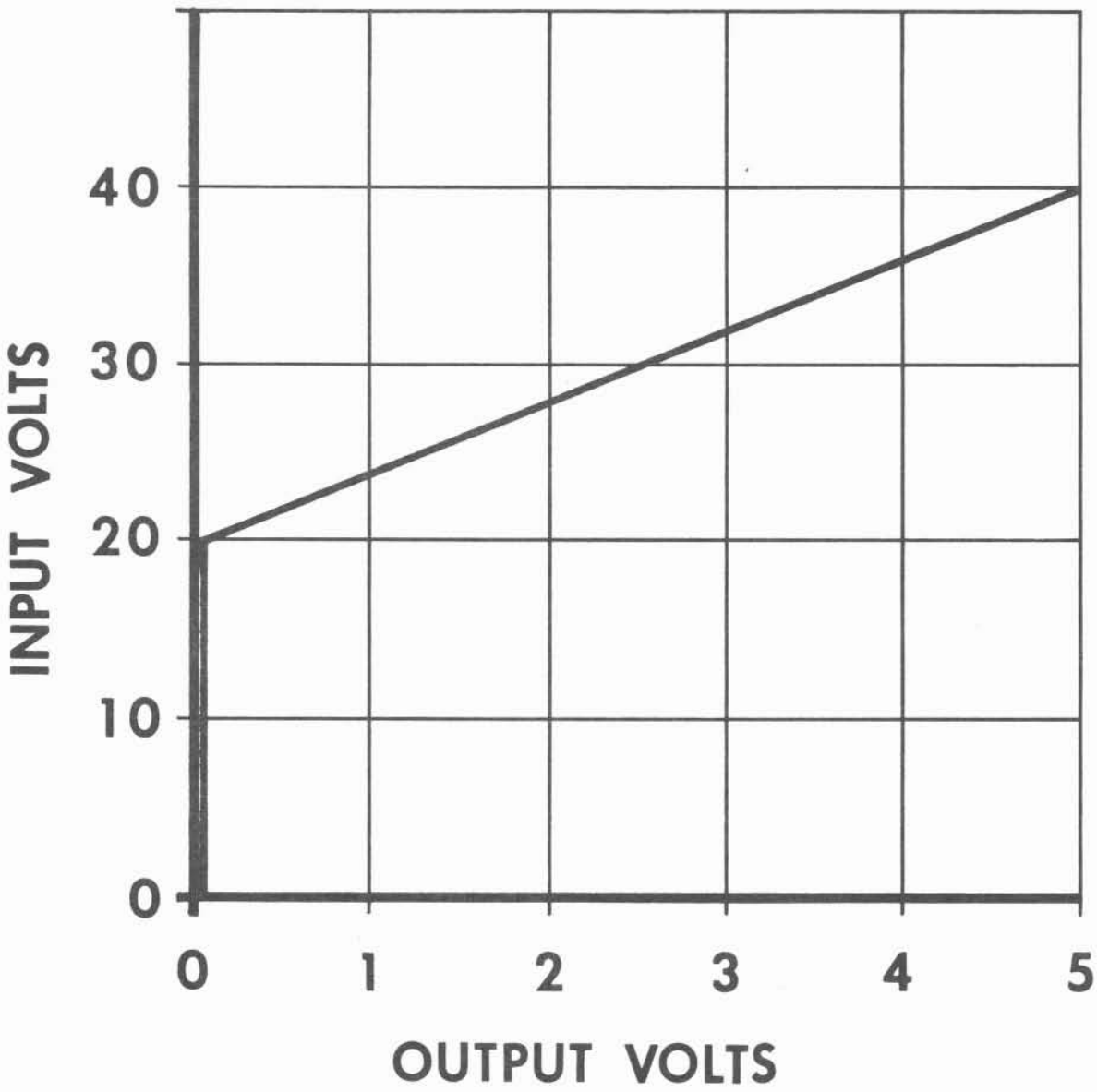


FIGURE 7

REMOTE VERIFICATION CIRCUIT

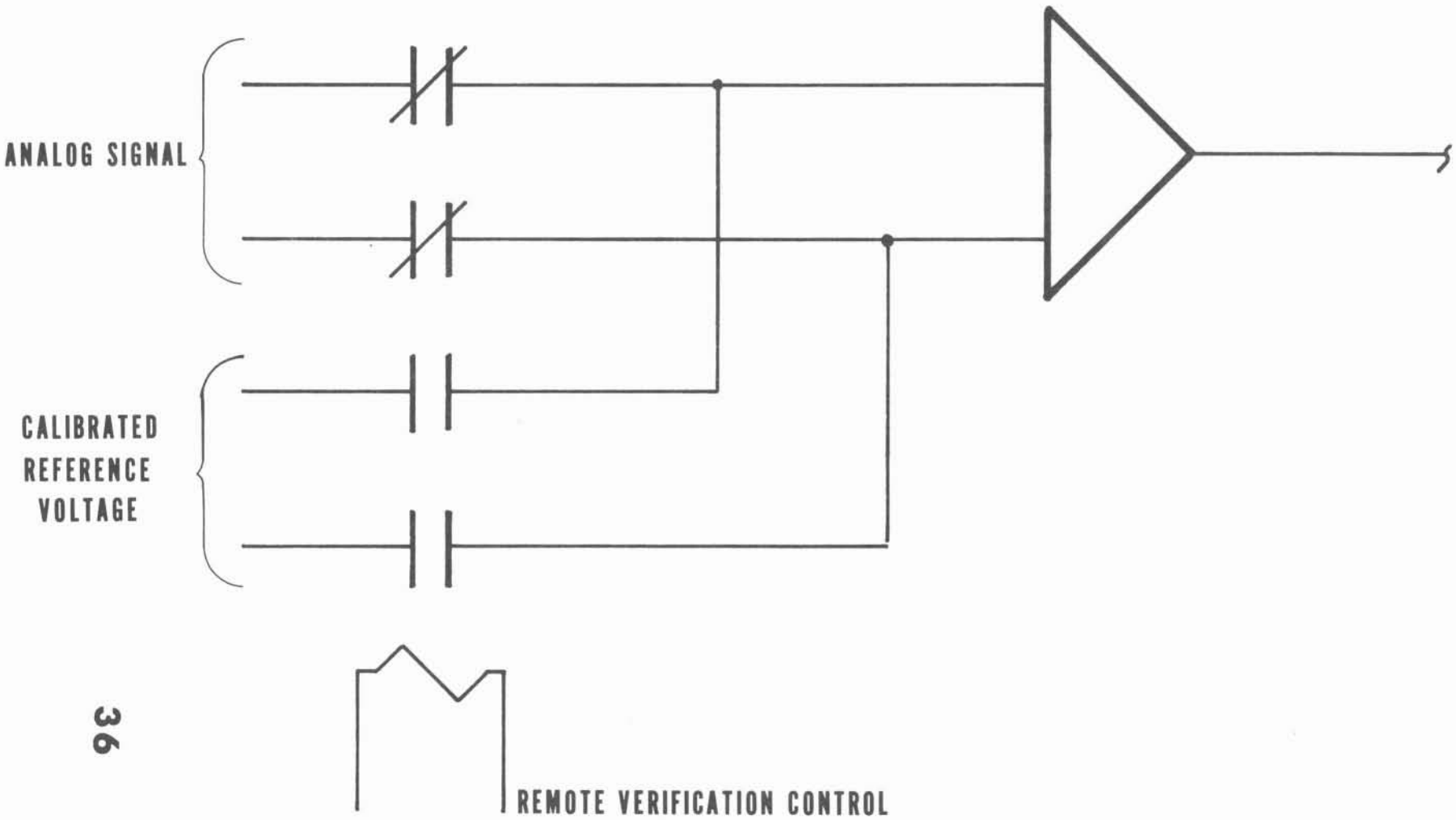


FIGURE 8

GROUND DDAS TRANSMITTER

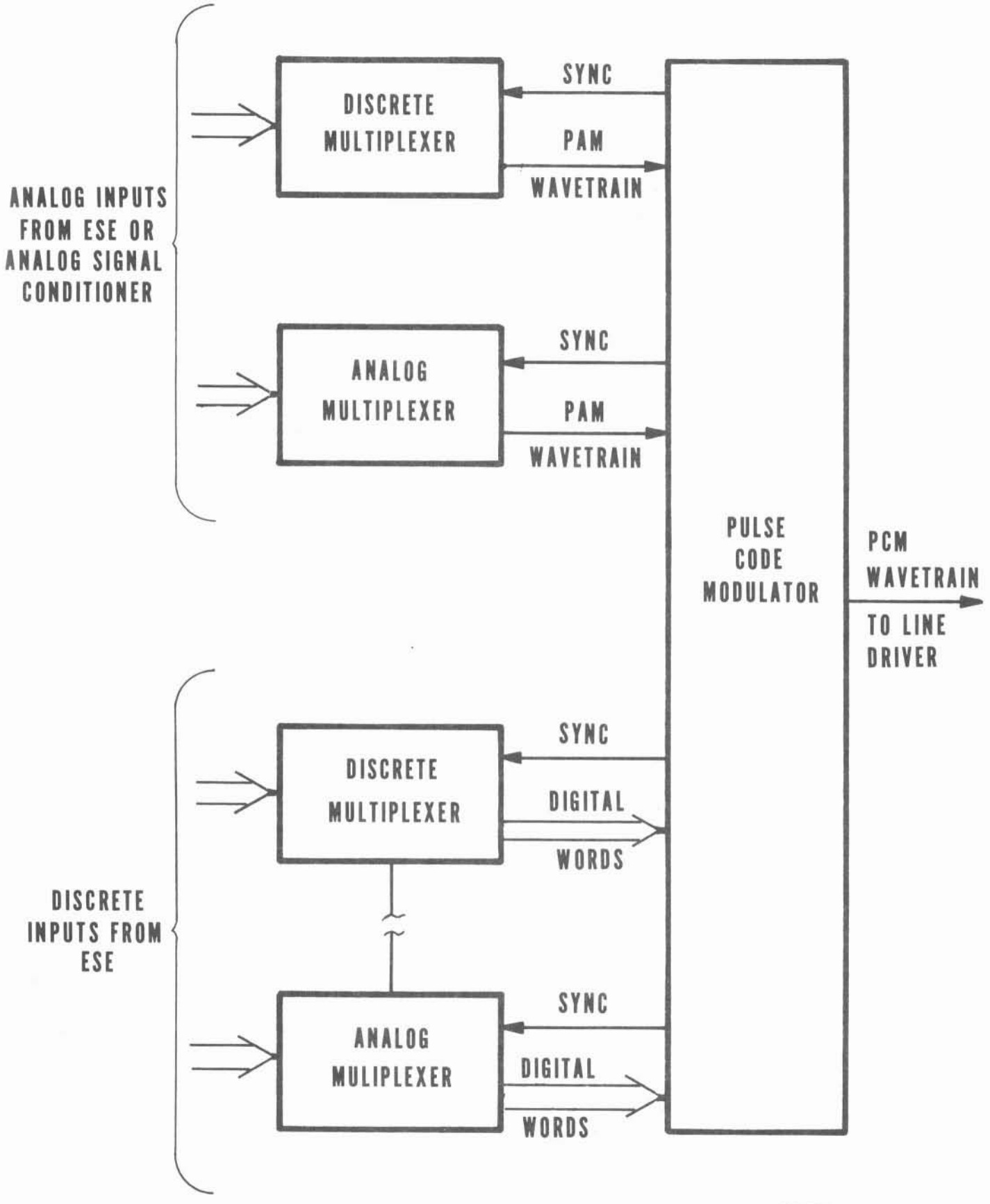


FIGURE 9

SIMPLIFIED MULTIPLEXER

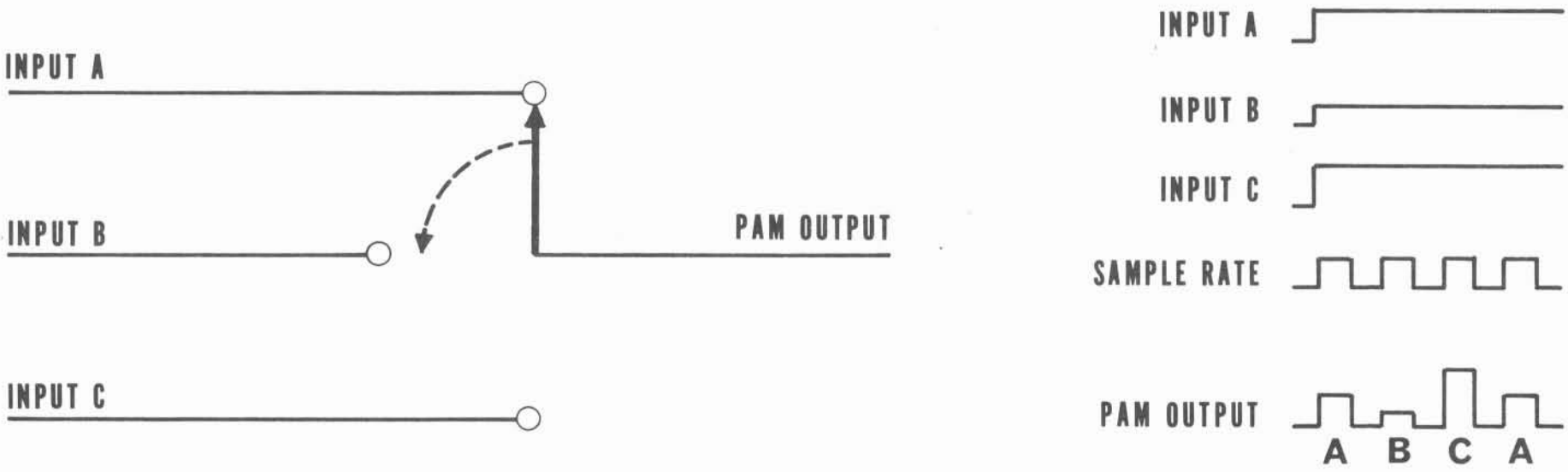


FIGURE 10

PULSE CODE MODULATOR

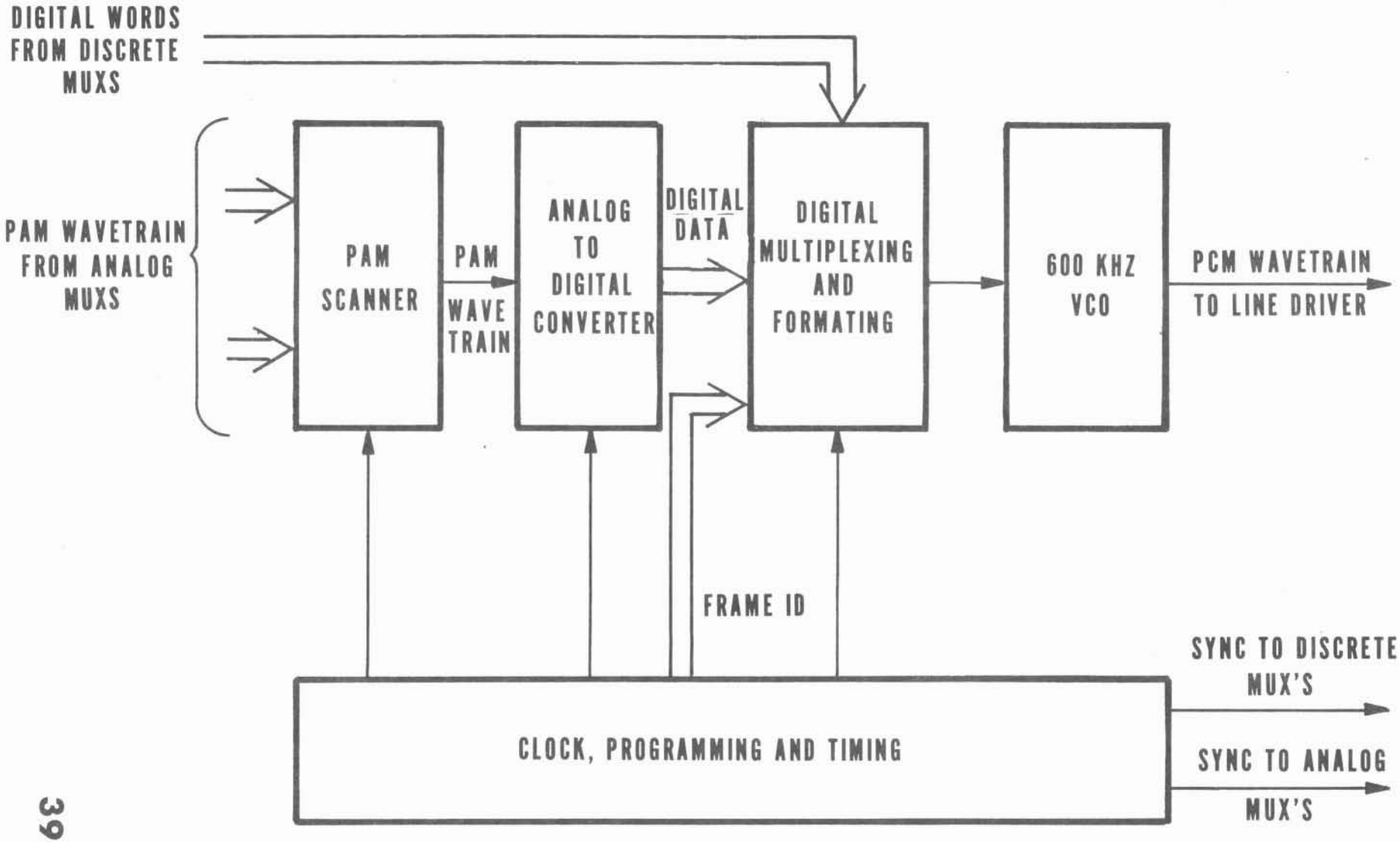
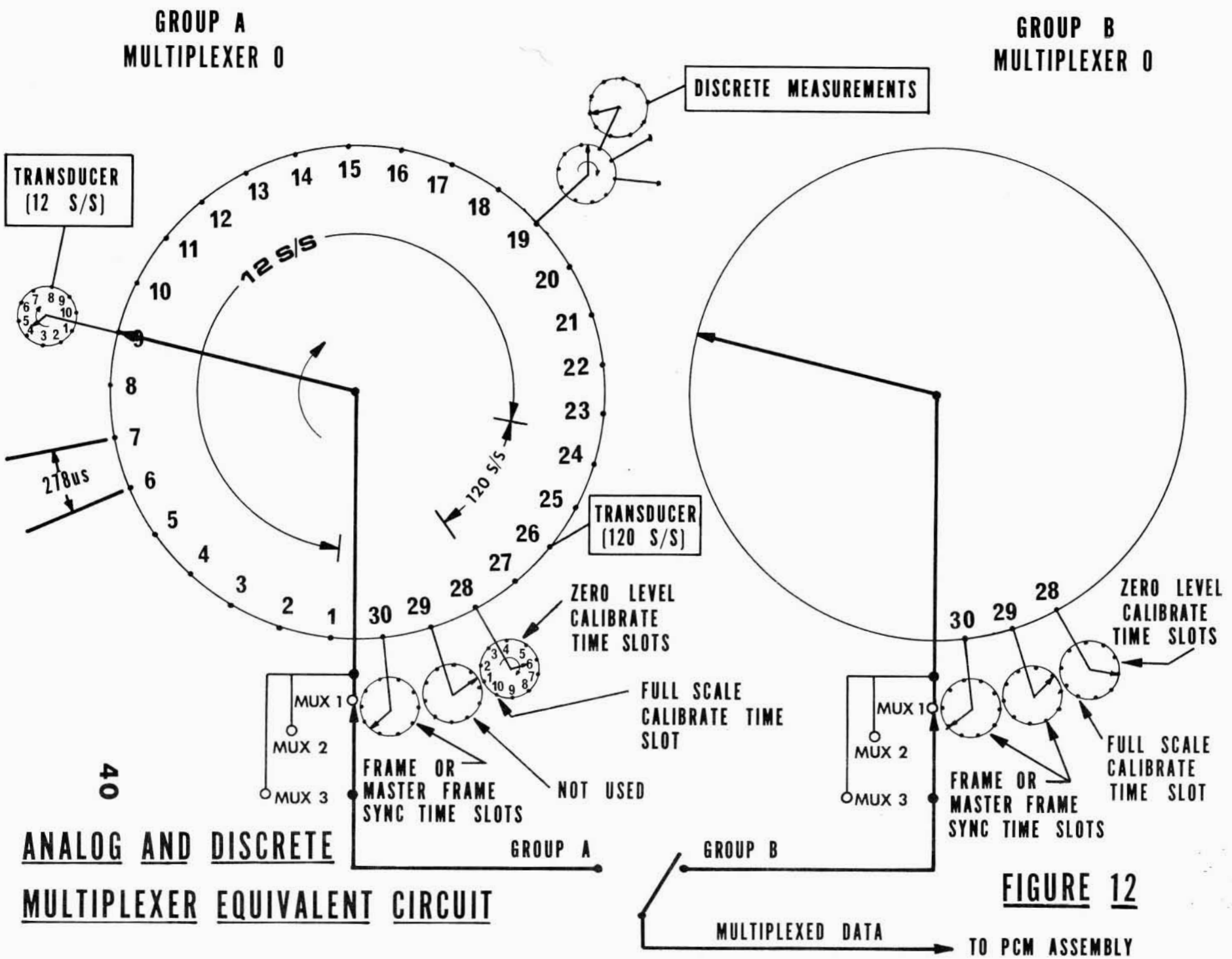
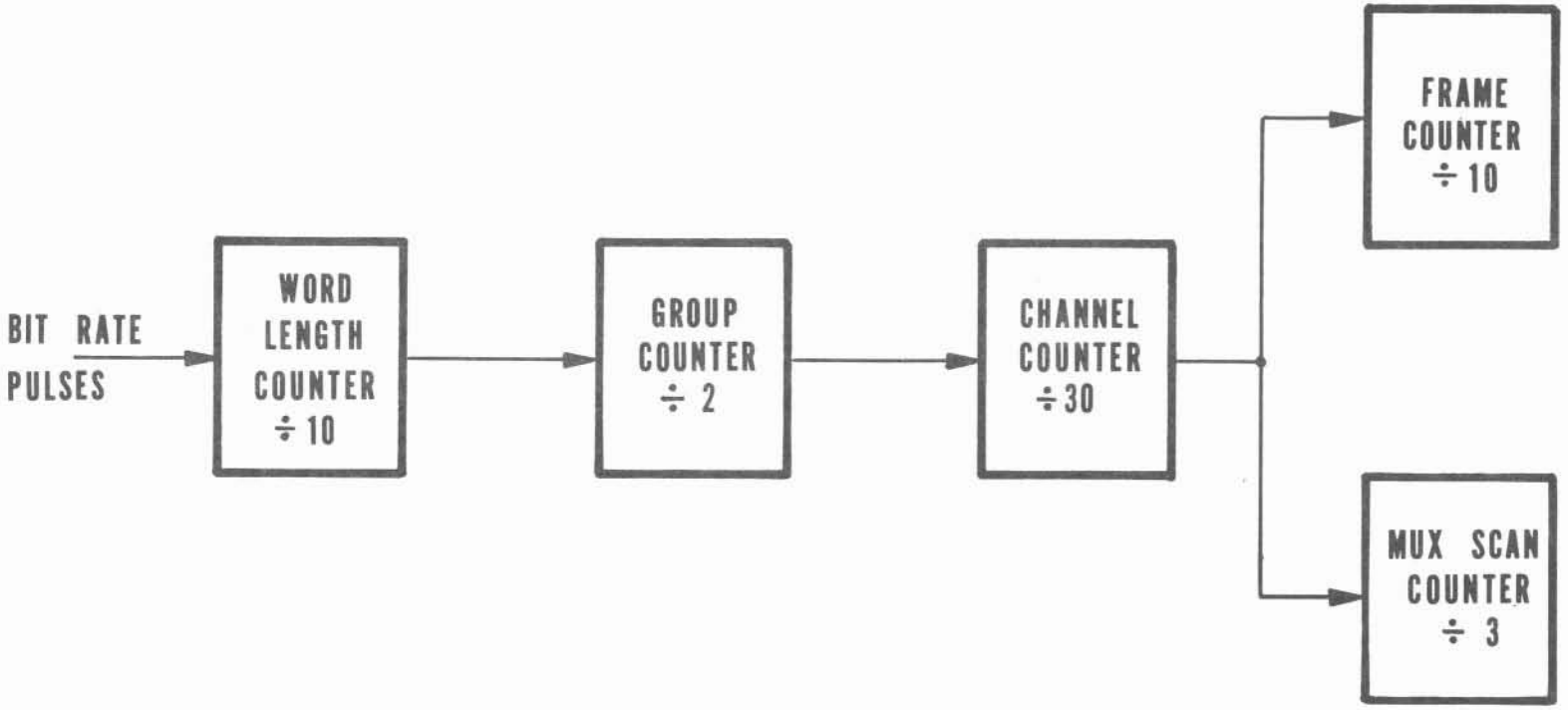


FIGURE 11



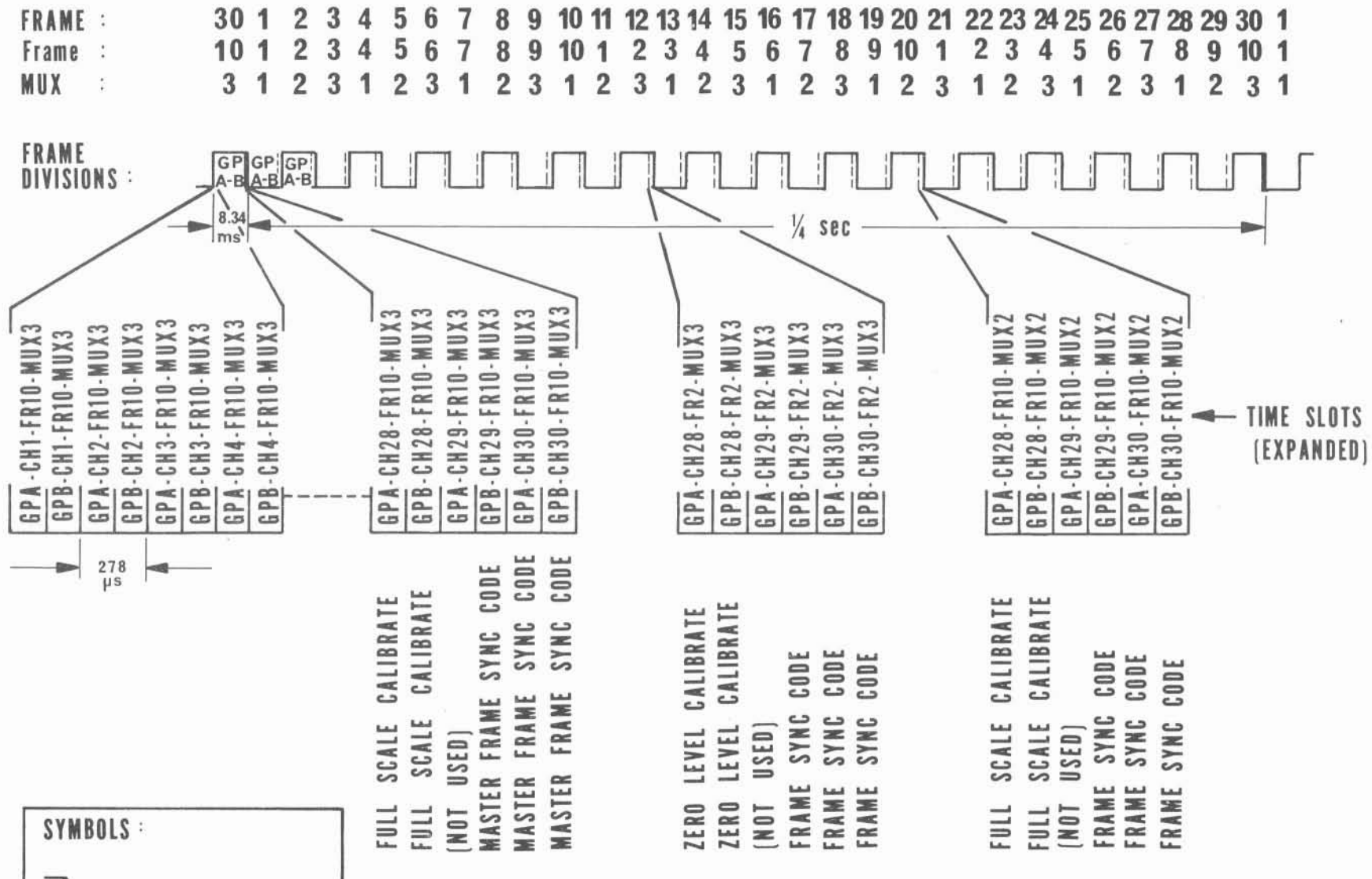
ANALOG AND DISCRETE
MULTIPLEXER EQUIVALENT CIRCUIT

FIGURE 12



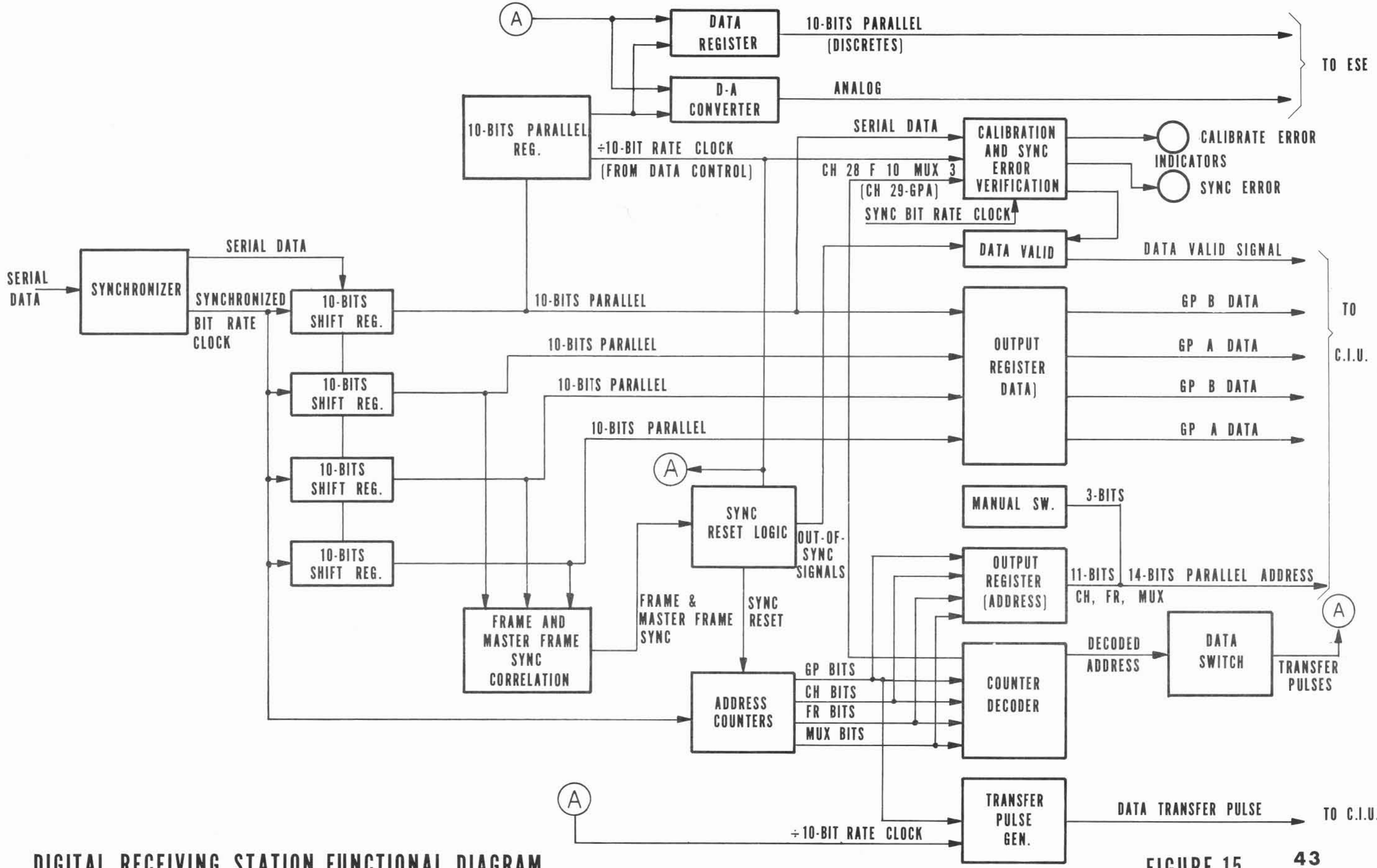
MULTIPLEXER COUNTERS

FIGURE 13



MULTIPLEXER SAMPLING SEQUENCE

FIGURE 14



DIGITAL RECEIVING STATION FUNCTIONAL DIAGRAM

FIGURE 15

DISCRETE OUTPUT

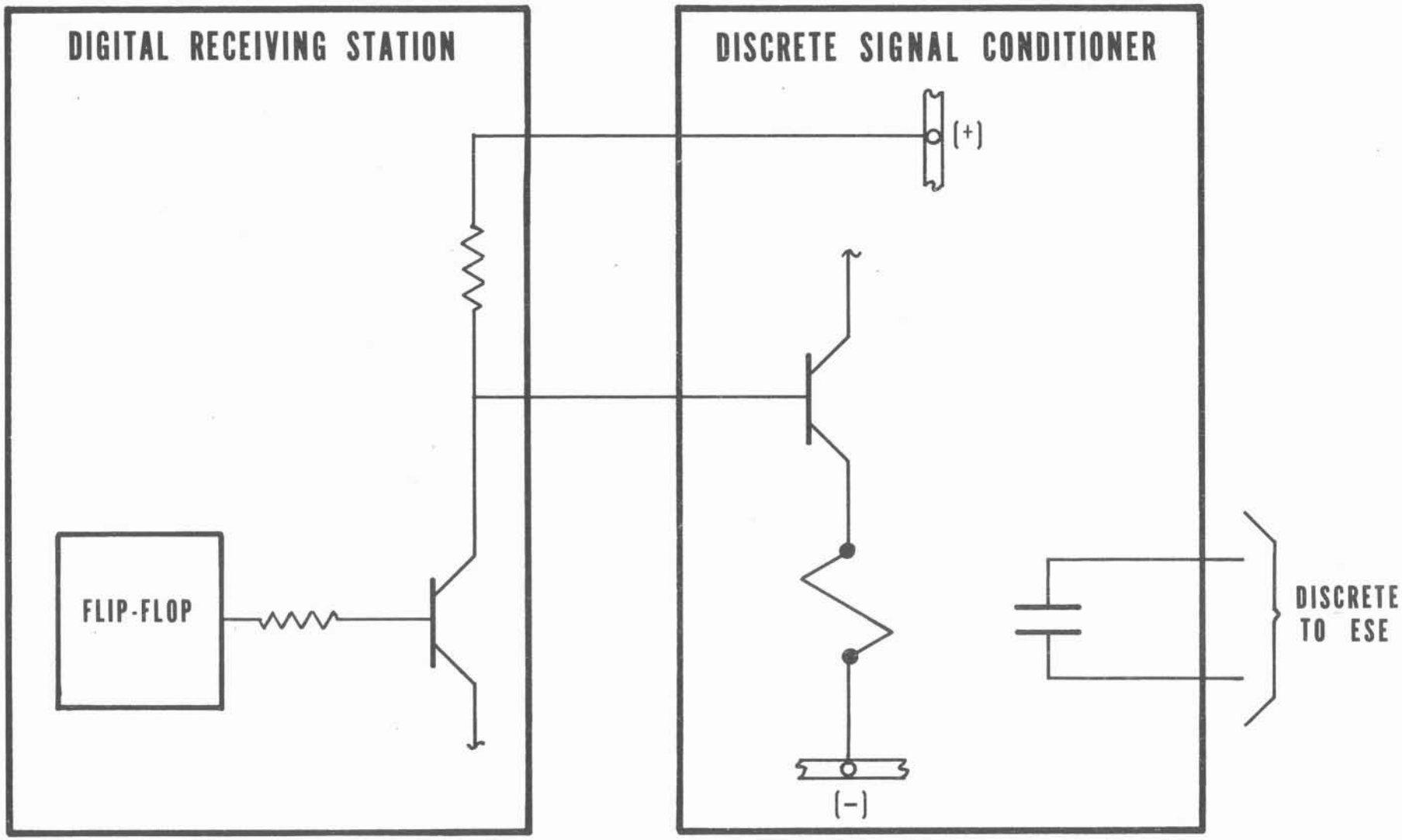


FIGURE 16

DDAS COMPUTER INTERFACE FUNCTIONAL DIAGRAM

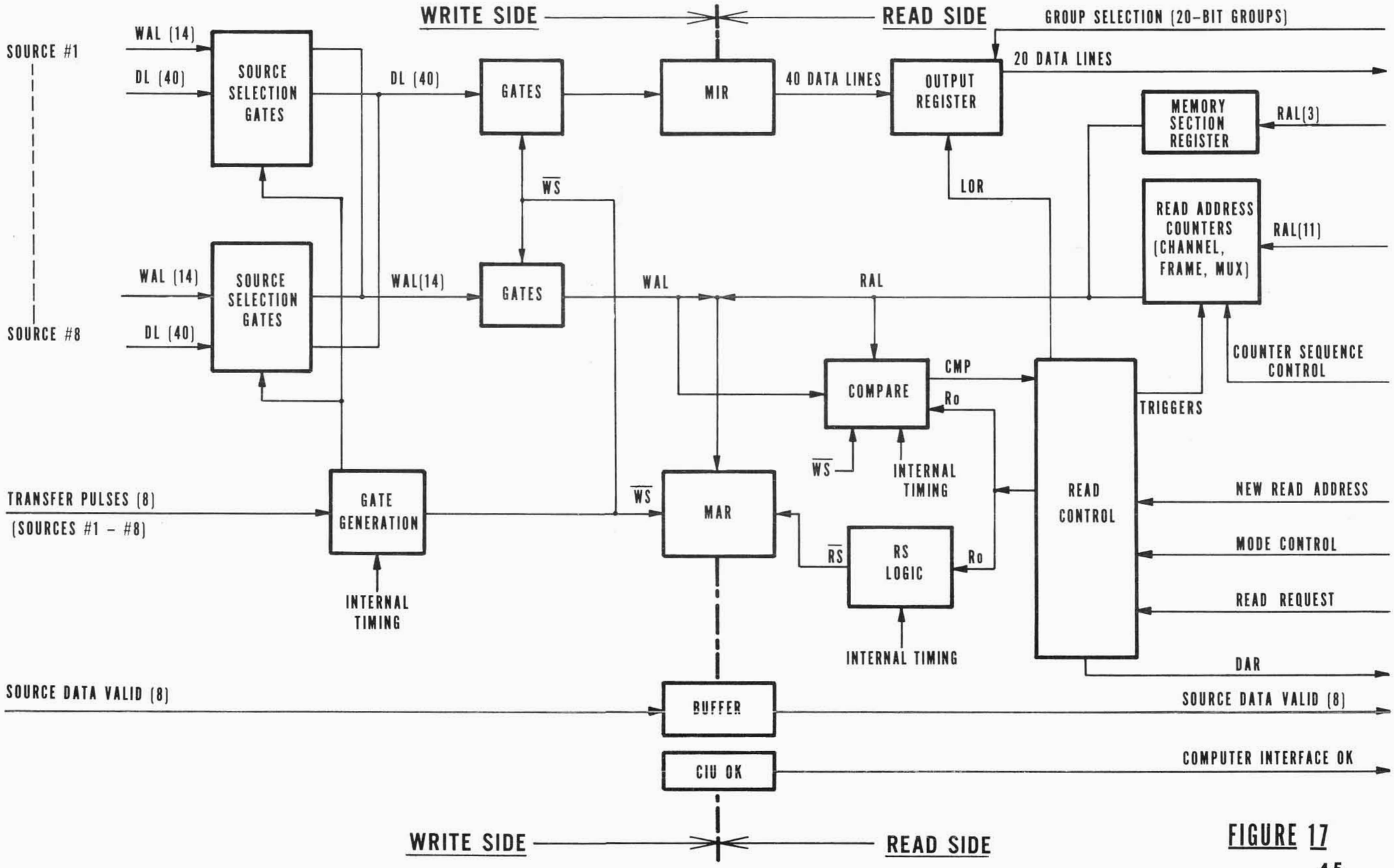


FIGURE 17

CORE MEMORY AND WRITE SCHEMATIC

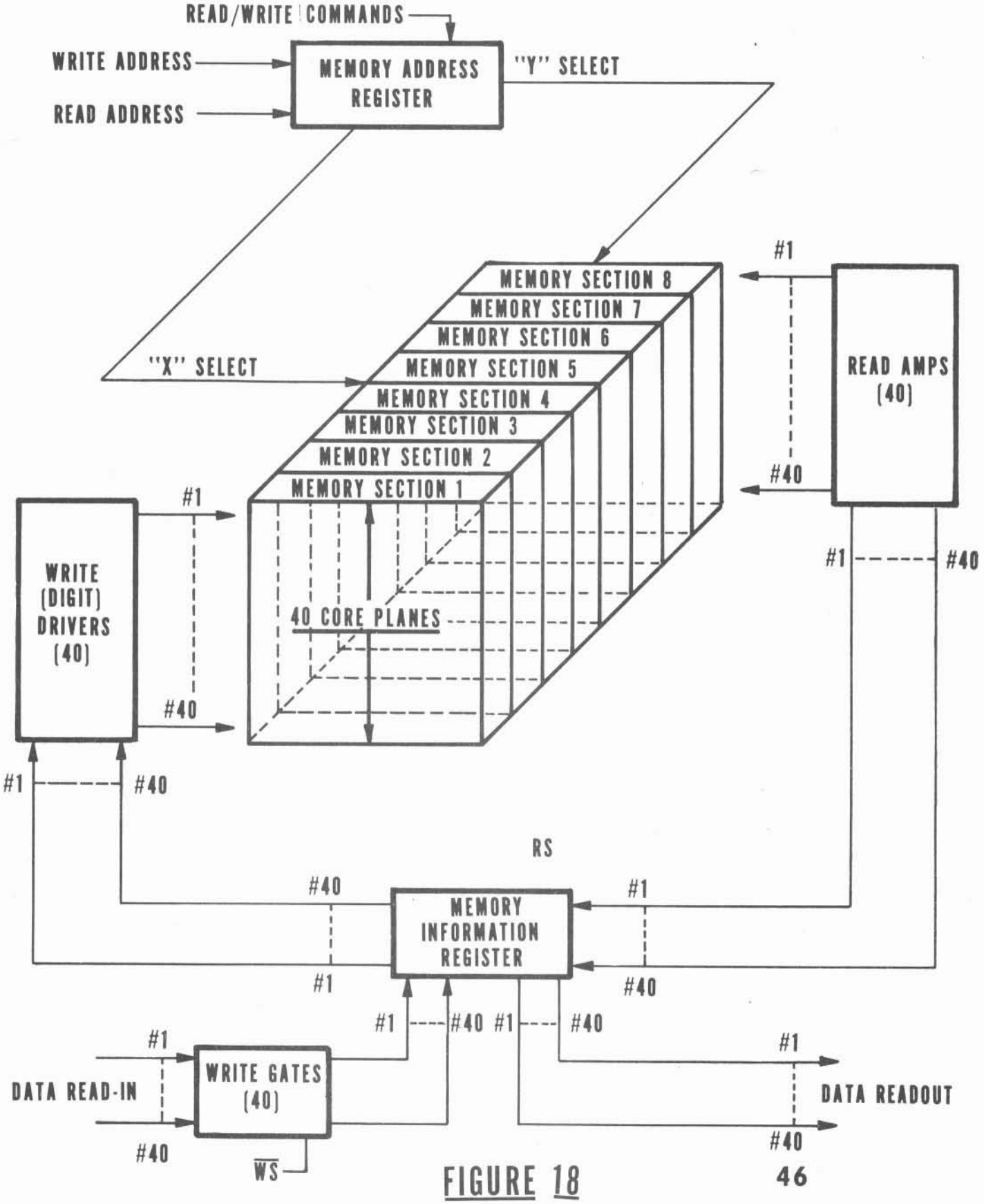


FIGURE 18

CORE MEMORY ADDRESS LOCATIONS

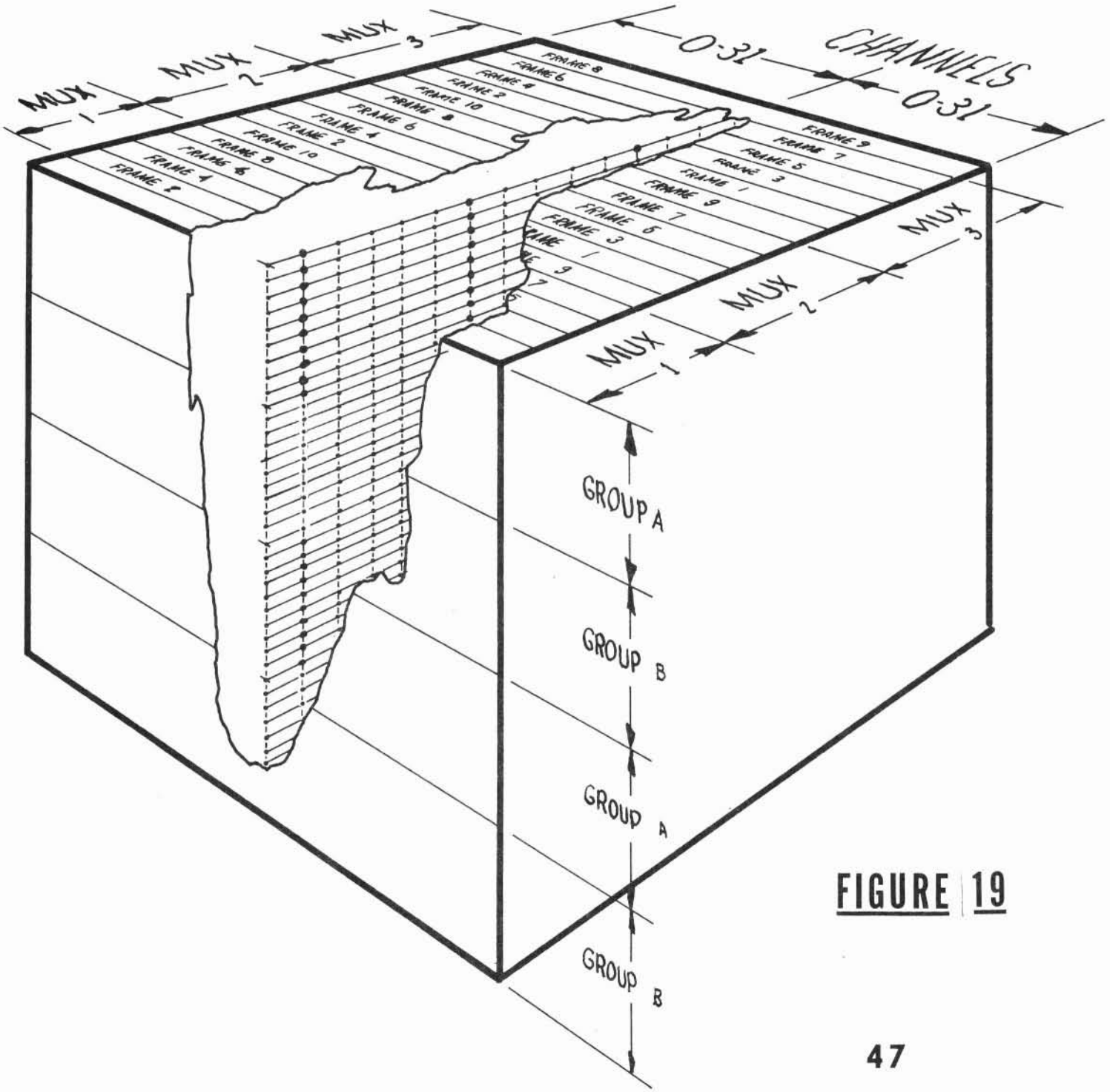
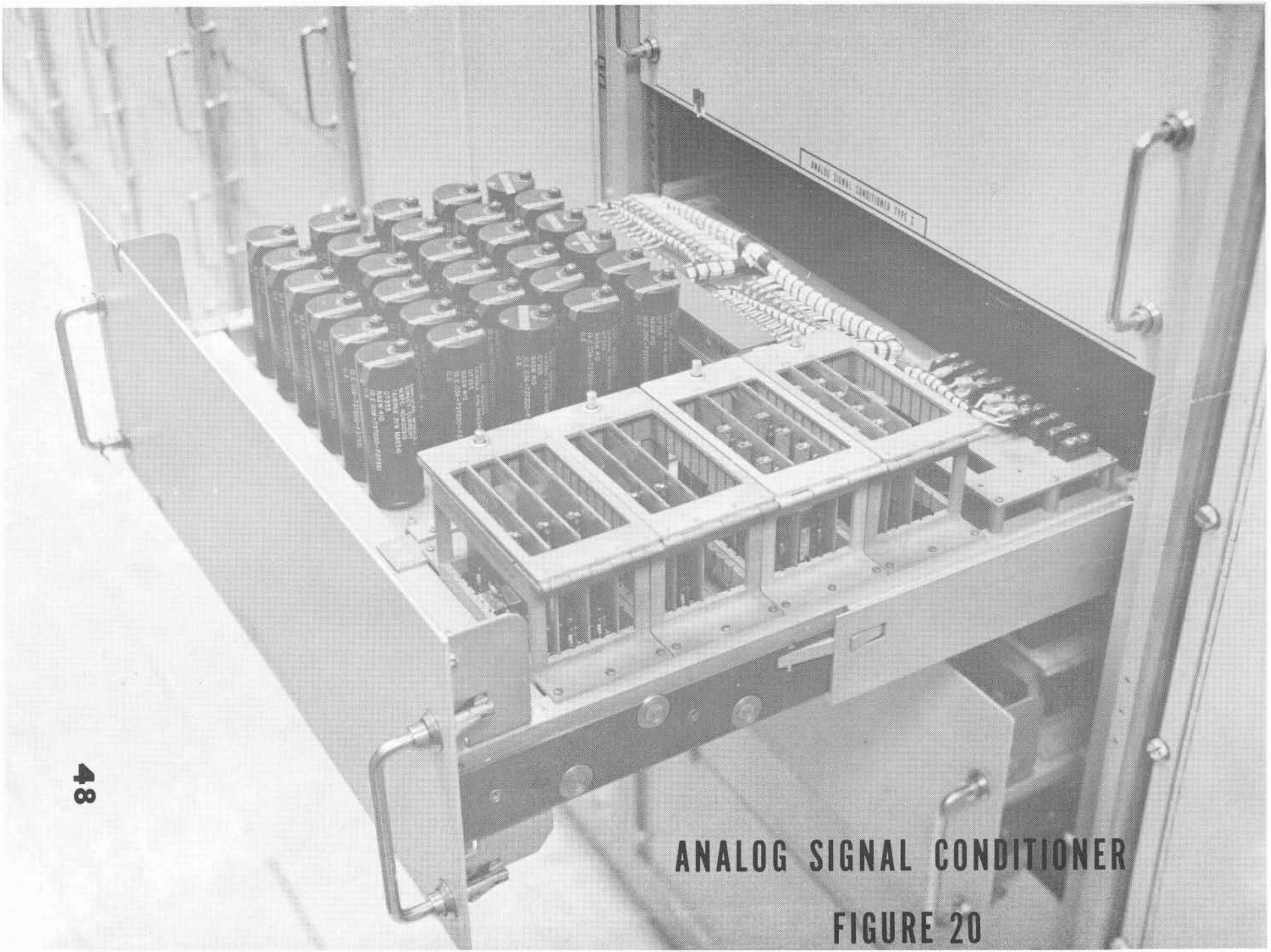


FIGURE 19

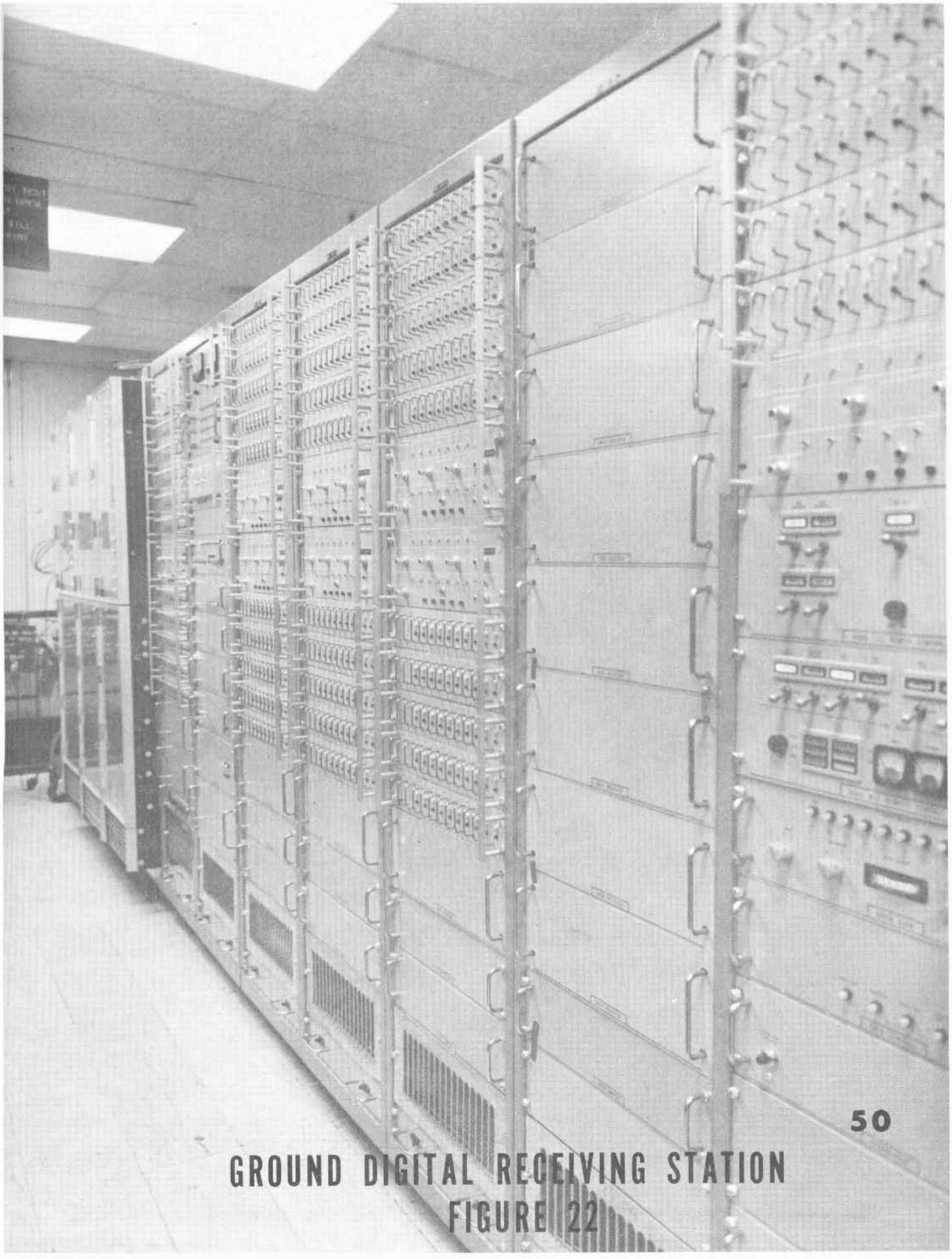


ANALOG SIGNAL CONDITIONER

FIGURE 20

GROUND DDAS TRANSMITTER

FIGURE 21



GROUND DIGITAL RECEIVING STATION
FIGURE 22

FUNCTIONAL DIAGRAM GROUND DDAS

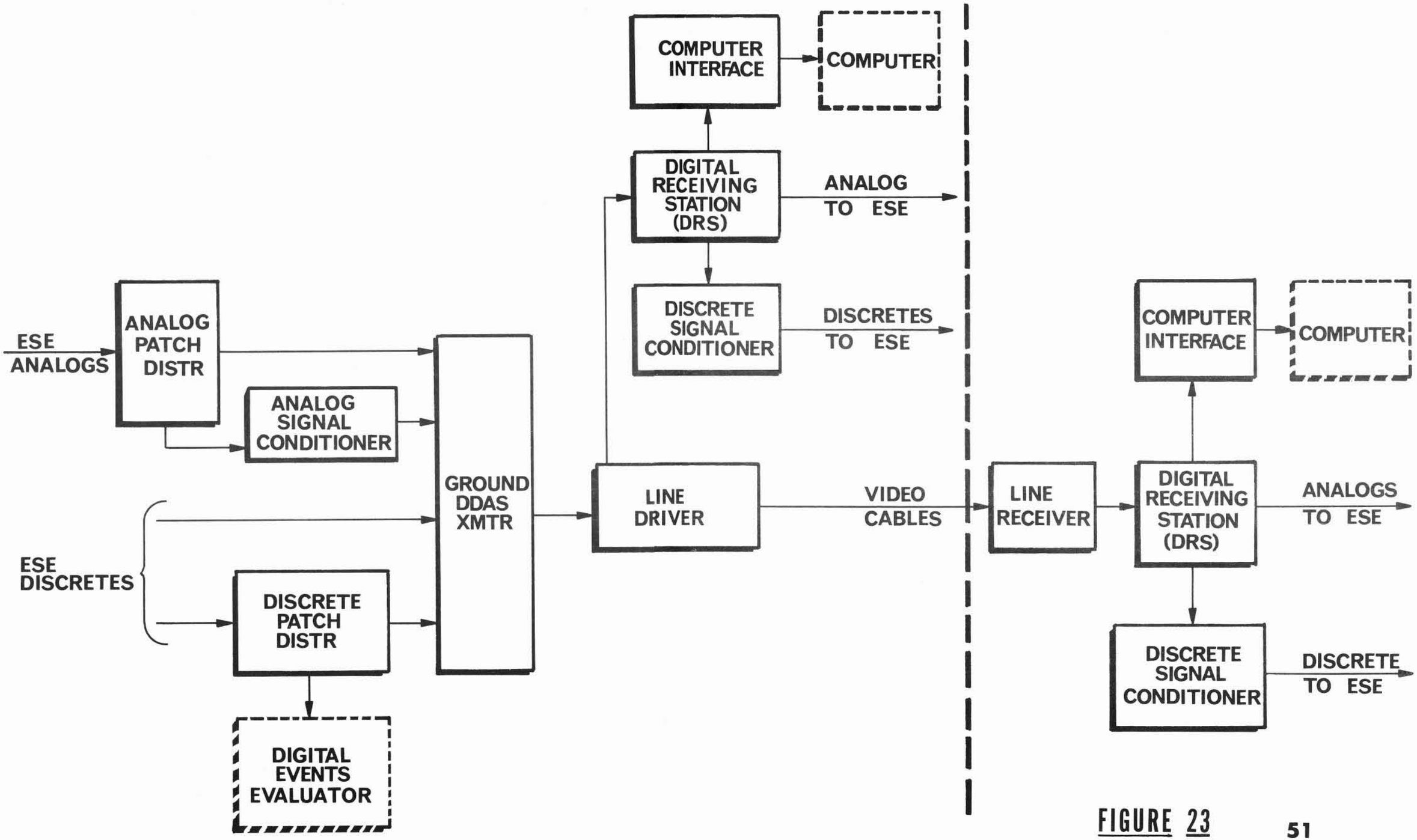


FIGURE 23

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GENERAL ELECTRIC