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TECHNIQUE FOR RELIABILITY CIRCUIT DESIGN REVIEW IN SPACE ELECTRONICS

by

P. J. Franciscovich

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Abstract

Design review is becoming a basic requirement during the design and development of military systems. The main purpose of the design review is to increase the system's inherent and operational reliability.

The major portion of this paper is the result of reliability's effort to comply with Paragraph 3.6 of NPC 250-1 Reliability Program Provisions for Space Contractors.

The design review to be discussed is a reliability circuit design review with emphasis placed on what should be reviewed and the review techniques employed.

The basic circuit design review prerequisites, component parts and their ratings, are discussed at the beginning of this paper. The remainder deals with the organization and reviewing of circuits. The review items include worst-case circuit performance, component applications, failure mode analysis, noise rejection, electrical stress, and the determination of component temperatures. Many examples are included to illustrate how each item was accomplished.

This paper is intended not only to give the reliability analyst cognizance of basic design problems and troublesome circuits, but also, to aid him in formulating a design review program.

Component Considerations

The most basic and important requirement for a thorough design review is to fully understand the function of a component and its rating.

Semiconductors

Many semiconductor failures are caused by heat. The heat may be a result of excessive current, voltage, power, misuse, etc. The maximum junction temperature is the most important rating a manufacturer should specify.

The component manufacturer will specify that his component will operate as specified for a certain set of conditions. It does not specify that it will operate in the same manner for conditions which deviate from the specified conditions. It is the customer's responsibility to operate the component below manufacturer's absolute maximum ratings. It is also the customer's responsibility to convert all of the manufacturer's component ratings into equivalent ratings which will satisfy his requirements. For example, the component manufacturer does not know at what ambient temperature a system will be operating and, more important, he does not know the type of system cooling. Therefore, the component manufacturer will, in the majority of cases, give a basic rating and other specified points from which the customer may interpolate or extrapolate the conditions he requires. Two good examples are the maximum junction temperature and the power-temperature derating slope.

A manufacturer will rate a semiconductor for an absolute maximum junction temperature. The temperature environment in which the device is rated significantly affects the power that may be dissipated to reach the absolute maximum junction temperature. Figure 1 shows a typical device's

power rating for two different temperature environments, but notice the absolute maximum temperatures are common to both.

Figure 1a shows the power that a semiconductor can dissipate in a free air environment. This plot shows that if the semiconductor is placed in a free air environment of 25°C and dissipates its rated power, the junction temperature will be at 175°C, or its absolute maximum temperature. In Figure 1b, if the case is held at a constant 25°C and the maximum power is dissipated, then the junction temperature will again be at its absolute maximum of 175°C. Although Figure 1b is an example, note the maximum power that may be dissipated in either instance. What does all of this mean to the customer or designer? It means that he will use the device somewhere between the "best case" where the device would be held constant and the "worst-case" where the device would be in free air. Therefore, it is the user's responsibility to estimate the ambient temperature of the semiconductor and to determine the type of cooling his components will have, i.e., radiation, convection, or conduction. Most space systems have conduction cooling.

The rating specified on the manufacturer's specification sheet which states, "ratings are at 25°C case temperatures", is rather an ideal case and caution must be exercised in applying that data.

The derating slope is known as the thermal resistance. This is specified as θ_{JA}, thermal resistance from the junction to the ambient air, or θ_{JC}, the thermal resistance from the junction to case.

Transistor breakdown voltage ratings are very important and must be examined before they can be properly applied.[1] The breakdown

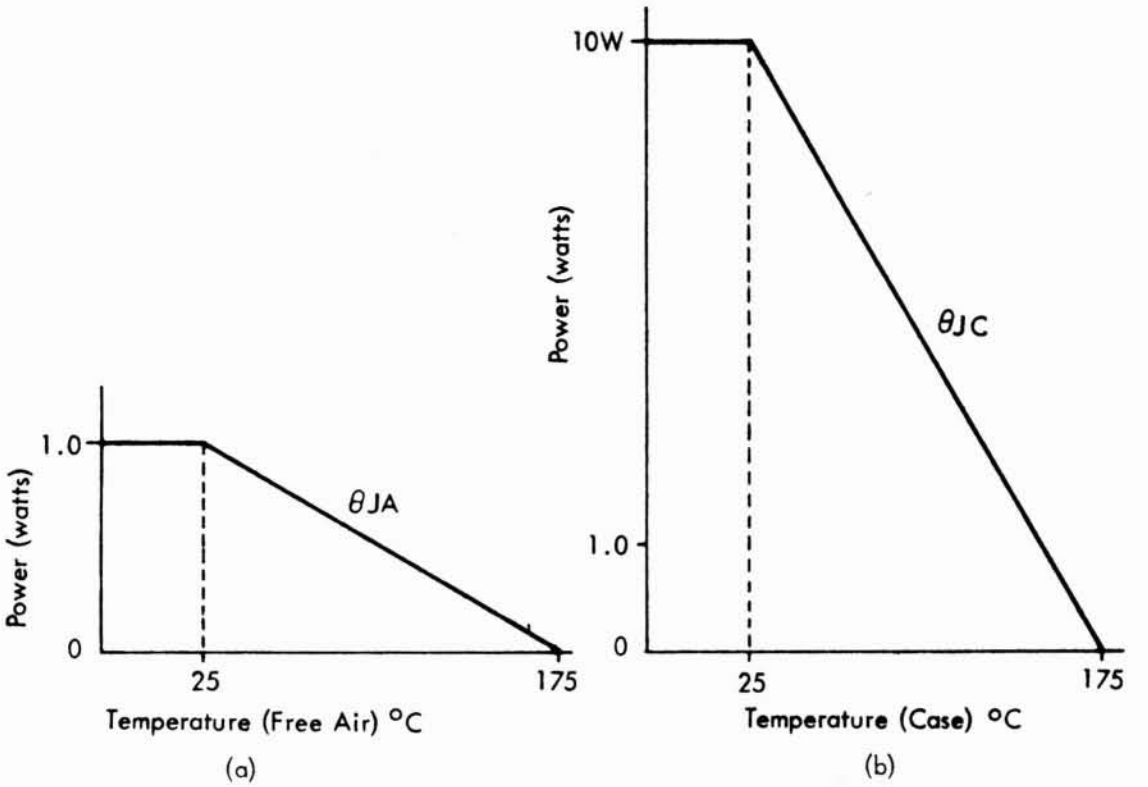

Figure 1. Two Power Ratings for the Same Device

voltages most commonly specified on the manufacturer's specification sheet are:

- BV_{CBO}
- BV_{CEO}
- BV_{EBO}

For example, BV_{CBO} is the breakdown voltage of the collector base junction with the emitter open. Since the manufacturer does not know how his customer will use the device, he must specify the "worst-case" breakdown condition. Depending on how the customer uses the device, he may have a higher breakdown voltage than the "worst-case."

For example, variations of BV_{CEO} may be BV_{CER}, BV_{CES}, and BV_{CEX}. Figure 2 shows the four cases.

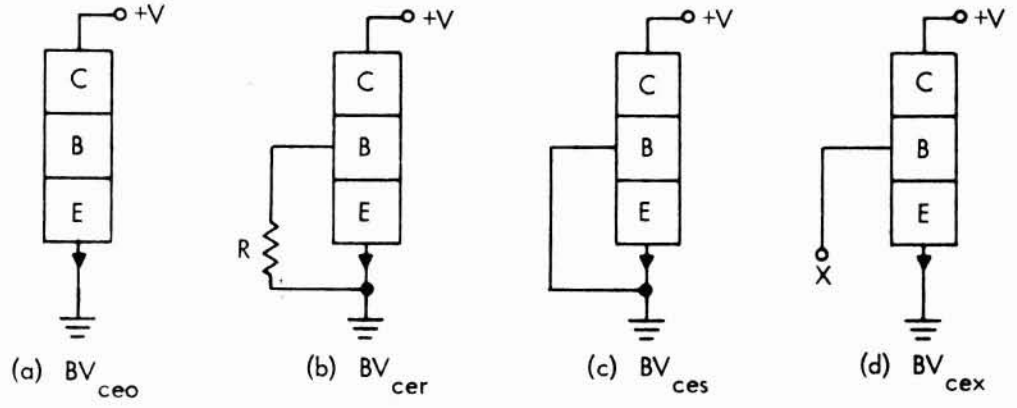

Figure 2. Voltage Variations

The parameter which affects breakdown voltage is leakage current.

In Figure 2a the collector-base junction is reversed biased and a leakage current flows to the base where it is amplified and produces a collector current. As the voltage is increased, the leakage current and the collector current increase. This process continues as a function of the applied voltage until the breakdown occurs.

The same basic principle is applied to Figure 2b except some of the leakage current is drained off via the Resistor, R. Therefore, more voltage may be applied to reach the amount of amplified leakage current which caused the breakdown in Figure 2a.

It can be noted that the smaller the R the more leakage current is drained off and the higher the breakdown voltage becomes. When R = 0 or emitter junction shorted, Figure 2c would apply.

For the highest breakdown voltage, BV_{CEX}, a negative voltage is applied to the base. In this case leakage current is drawn from the base to prevent the breakdown from occurring as easily. Figure 3 shows a typical breakdown range, neglecting the sustaining voltage for the different ratings.

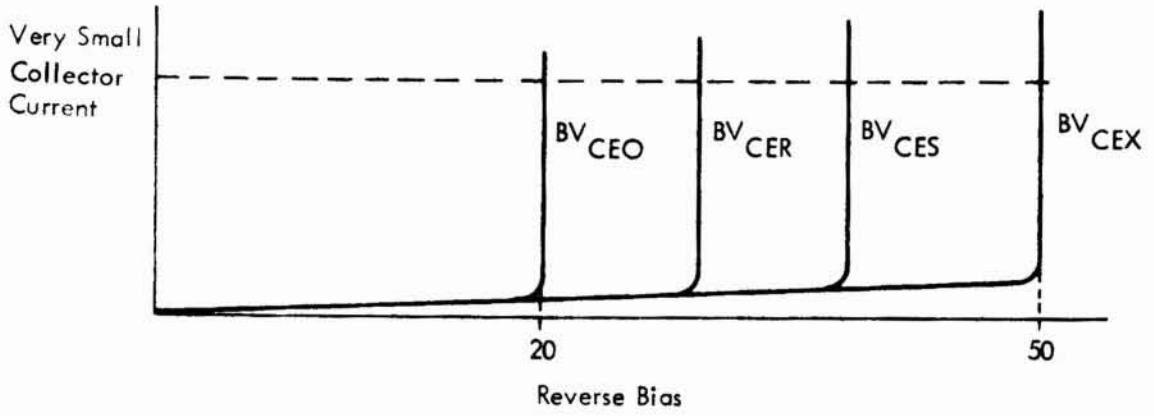

Figure 3. Typical Breakdown Range for BV_{CE}

This brief explanation of breakdown voltages was discussed to emphasize why the "worst-case" design should not exceed BV_{CEO}, BV_{CBO}, or BV_{EBO} voltages.

Aid for Reviewing Circuits with Diodes

When circuits contain many of one-type diode, the diode V-I characteristic should be plotted on semilog graph paper. This graph will speed the design review and will be very useful. The V-I plot is essentially linear on semilog paper for a forward current of about 10 ma, or when the diode contact resistance begins to affect the characteristic. Figure 4 is a typical example.

The question that arises for this type of plot is "where can the data be obtained?"

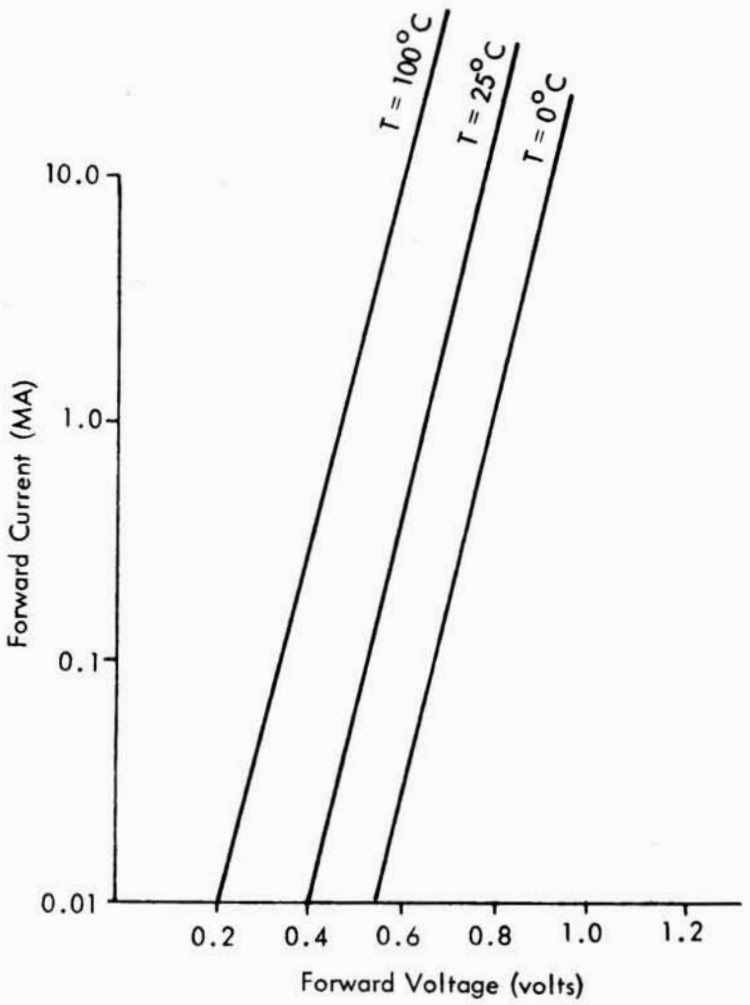

Figure 4. Voltage-Current Characteristics for a Typical Diode

If the end-of-life (EOL) data is available for the particular diode, select any two V-I points (below 10 ma) at the same junction temperature. A straight line may then be drawn through the two points.

If only one EOL V-I point is specified and the data is not conveniently available, take samples of the same diode type and measure them to find one that coincides with the specified V-I point. Then, with the

same diode, find any other V-I point. From these two V-I points, a straight-line plot on semilog paper may be made for the diode.

Another aid used is the diode equation instead of the V-I plot. The following describes how the particular diode equation may be found:

(1) Plot the straight line curve on semilog graph paper (Log = i; Linear = V)

(2) Use the following equation for determining the particular solution $i = \epsilon^{k\,1V + k2}$

(3) Find any two V-i points on the curve, call (V_1, i_1) the larger point, and (V_2, i_2) the smaller point.

Solving for the two constants k_1 and k_2

then $\ln i_1 = k_1 V_1 + k_2$

$\ln i_2 - k_1 V_2 + k_2$

subtracting $\ln i_1 - \ln i_2 = k_1(V_1 - V_2)$

or $k_1 = \dfrac{\ln i_1 - \ln i_2}{V_1 - V_2}$

and $k_2 = \ln i_1 - k_1 V_1$

Since the two constants are known, the following equation will describe the particular diode V-I curve:

$$i_F = \epsilon^{k_1 V_F + k_2}$$

where

i_F = forward diode current (milliamperes)

V_F = forward diode voltage drop (volts)

and k_1 and k_2 are the constants previously found.

For example, refer to Figure 4, the V-I curve at 25 °C.

First choose two V-I points:

at an I_1 = 10 ma, V_1 = 0.76V

at an I_2 = 2 ma, V_2 = 0.68V

secondly, solve for k_1 and k_2

$$k_1 = \frac{\ln i_1 - \ln i_2}{V_1 - V_2} = \frac{\ln \frac{i_1}{i_2}}{V_1 - V_2} = \frac{\ln 5}{0.76 - 0.68} = 20$$

$$k_2 = \ln i_1 - k_1 V_1 = \ln 10 - (20)(0.76) = 2.3 - 15.2 = -12.9$$

then

$$i_F = \epsilon^{(20)(V_F) - 12.9}$$

The equation is useful for computer circuit analysis programs, since tables and diode curve approximations are eliminated.

Resistors

Tolerances:

To review a design that has been "worst-case" designed, the reviewer must first review the Resistor EOL tolerances to verify that they are "worst-case".

Initial tolerances and load-life drift tolerances do not completely define the EOL design tolerances. There are at least four variables which affect resistor tolerances that must be considered. They are:

- initial vendor purchase tolerance
- temperature coefficient of resistance
- load-life drift
- drift due to in-house manufacturing processes.

Initial vendor purchase tolerance - The initial purchase tolerance is that tolerance for which the resistor was procured. This tolerance is a function of what the designer chooses.

Temperature Coefficient of Resistance (TCR) - The TCR is a function of temperature. It may be positive or negative and is usually specified in parts per-million per-degree Celsius (PPM/°C). The specified TCR may or may not be constant over a given temperature region. Therefore, if TCR is not constant, one must determine the TCR that will exist at the operating temperature, not at the specified temperature.

Load-Life Drift - This tolerance is a function of time, power, and temperature. The component vendor usually supplies the load-life drift tolerances.

Manufacturing Process Drift - This tolerance results from environments or processes the procurer uses in packaging the resistors. Items in this category would include encapsulation, storage, aging, and soldering. The following is a typical example of EOL tolerance for a metal-film resistor with a TCR of ±100 PPM/°C over a temperature range of 100°C:

Initial Purchase Tolerance	±1.0%
Drift due to TCR	±1.0%
Load-Life Drift (2000 hours)	±0.3%
Manufacturing Process Drift	±0.2%
End-of-Life (EOL) tolerances	±2.5%

For this example, the designer should use for his "worst-case" design a resistor that has a maximum and minimum value of $R_N \times (1.025)$ and $R_N(0.975)$, respectively, where R_N is nominal value of the resistor.

Ratings

The most important rating for carbon composition, fixed or metal film resistors, is the power rating. The important consideration for power rating is the determination of the case temperature at which rated power may be dissipated. Usually, these devices are rated at 25 C, 70 C or 125 C. If the resistor is expected to operate in an environment which is higher than its rated temperature, the first consideration is to assure the dissipation to be safely below the manufacturer's recommended rating.

Both power and voltage ratings are important for wire-wound resistors. The voltage rating is usually specified to prevent high currents in small wire and to prevent arcing from wire-to-wire. For example, a resistor manufacturer may rate a resistor for one watt, but due to the value and wire size, it may be found that only two or three tenths of a watt may be dissipated before the voltage rating is exceeded. Therefore, in that case, the power rating is meaningless and the emphasis must be placed on the voltage rating.

Carbon and metal film resistors also have voltage ratings, but in practically all space circuit applications, either the power rating dominates or the voltage rating is high enough that it is never encountered.

There are many other components whose ratings could be discussed, however, transistor diodes and resistors are the majority for space electronics.

The important consideration for reviewing any component in a design is to understand the conditions for which the rating was specified and to apply that rating to the conditions or extremes that it will be used.

Integrated Circuits

Only a few ratings accompany integrated circuits (IC). They are usually supply voltage, input voltage, and temperature range. For an integrated circuit system, the supply voltages should be chosen to be safely below the manufacturer's rating.

Thermal resistance (junction to case) and the maximum allowable current are two often neglected ratings that must be considered in any design review. Since integrated circuits are fabricated using P-N junctions, the temperature of a particular junction is a function of the power that is dissipated at that junction plus at any other junction. In other words, one thermal resistance may be specified from the chip to the case (the chip or IC itself may be considered an isotherm). The other neglected rating is the maximum allowable current density. This value should be considered in reviewing IC's, since exceeded current density ratings will create time-dependent failures such as loose or cracked metalization lands.

For example, a typical metalization, shown in Figure 5, from the lead bonding pad to a transistor may have a width of 1 mil and a thickness (X) of 12,000 A. The cross-sectional area is approximately 3×10^{-7} CM^2. It can be seen that this is a very small cross-sectional area. Since current density is expressed in current per unit area, (usually AMPERES/CM^2) the actual absolute value must either be obtained from IC manufacturer or tested by the procurer. A typical current density is approximately 200,000 AMPERES/CM^2.

For any logic IC there are only two metalization conductors for which the current density must be known. They are the output transistor's collector and emitter metalization patterns. The IC manufacturer has control over the current within the IC, but he does not know exactly how the customer will use the inputs and outputs. Therefore, it is the design reviewer's responsibility to know the IC manufacturer's rating and how the designer will use the device.

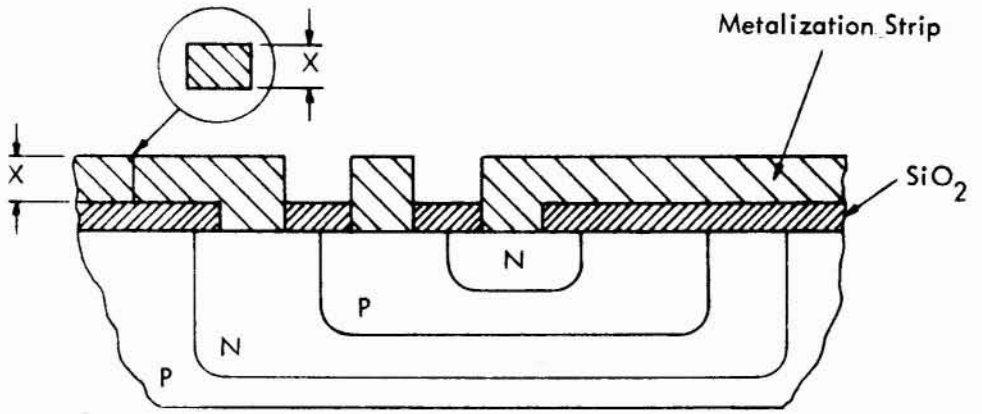

Figure 5. Typical Metalization

Beginning a Circuit Design Review

The purpose of a circuit design review is to approach an optimum design by eliminating problem and/or potential problem areas, simplifying circuits, testing for proper component applications, and performing a "worst-case" design analysis. These are the primary objectives that a circuit design review should achieve.

The depth of the design review is determined by the customer's requirements. This is usually determined by the reliability requirements that a system must attain.

Initially, a list of all component specifications, ratings, and deratings should be placed in one document for easy reference.

Also, a review of all the designer's assumptions should be made. Once this has been completed, decide what should be reviewed.

The following will show some items to review, and briefly, how to do them.

Verification of Worst-Case Analysis

A reviewer may use three approaches to verify a worst-case design. They are hand-solved equations, manual breakboard tests, or computer circuit analysis programs.

The manual type is very effective but it is also very time consuming, unless a well qualified person who is familiar with many circuit types does the review. Breadboard tests are time consuming, expensive, and the results are only fair. Obtaining worst-case components presents a problem with breadboard test. It can be done by sampling a large stock of components to obtain the desired values and using potentiometers, but in reality, all the components are never worst-case. Computer circuit analysis programs are just beginning to be accepted. They are inexpensive and the results may be poor or good. The programs are usually well constructed to work for ideal cases but when they are used on various types of practical circuits, many problems are likely to occur. The most difficult task in the preparation of a computer circuit analysis is a good workable model of an active device (transistor, diode, etc.). If a system, such as a computer, contains only a few types of active devices, then the models may be perfected to a good workable state. However, if a system contains many and various types of active devices, the time expended describing the models becomes excessive.

The most efficient program to use is one which requires very little programming time by the reviewer.

The best methods of reviewing digital circuits are the manual-type calculations and the computer circuit analysis program. The best method of reviewing analog circuits is the worst-case breadboard method or a computer circuit analysis program.

To begin the analysis, use the worst-case inputs and establish the circuit component parameters to give the worst-case output conditions.

For a typical inverter circuit, the factors to be determined are: (1) a worst-case input up level that will result in what maximum down level, and (2) a worst-case input down level will result in what minimum

up level. Then compare the specified outputs with those that were calculated. There are many ways of calculating the worst-case conditions, but nodal analysis seems to be the most effective.

Verification of Proper Component Application

Verification of the proper component values and stresses may be obtained from the circuit analysis. In addition to the proper value, the end-of-life (EOL) parameter tolerances should be compared.

For example consider Table 1.

Table 1

COMPONENT EOL VALUES

Component	Parameter	Parameter Value		
		EOL Design	EOL Specified	EOL Demonstrated
R_1	Resistance	3.2K ± 5%	3.2K ± 5%	3.2K, ≤ -4.5%; ≤ 4.0%

The Component column refers to the circuit component reference designation.

The Parameter column lists the parameter(s) which are affected by EOL tolerances.

EOL Design is the component value and its EOL tolerance used in the design.

EOL Specified is that tolerance to which a component EOL parameter is specified.

EOL demonstrated represents the observed worst-case EOL tolerances at the end of some period. The tolerances are composed of (1) initial tolerance, (2) temperature coefficient of resistance, (3) load life drift, and in-house process drift.

The EOL design value must be equal to or greater than the EOL specified and the EOL demonstrated values, e.g., if the demonstrated values were greater than the EOL design, the design was not "worst-case" due to an improper tolerance.

Component stresses must also be computed since it is usually the stress level which dictates the systems failure rate.

Table 2 is useful for comparing the actual stress for a circuit component with the maximum allowable stress specified by Reliability.

Table 2

ACTUAL STRESS AND MAXIMUM ALLOWABLE STRESS

Component	Stress Occurred at	% of Rated		Factor Causing Stress		
		Actual	Allowed	Power	Voltage	Other
Q_1	Collector Junction	40%	50%	X		

Failure Mode Analysis

The primary purpose of this analysis is to verify that a redundant circuit is redundant. The secondary purpose is to supply the circuit failure modes to the analyst who will perform the Failure Mode and Effect Analyses and determine the criticality of the effects at the functional and system levels. If the system is simplex, the primary purpose is to supply the failure mode and effect analyst with the circuit failure modes caused by the component part failures.

In performing circuit failure mode analysis, two classes of circuits are considered. They are digital circuits and analog circuits.

The digital circuits have specified input and output signal requirements (voltage, current, timing, etc.) which classify the logical state as either a "1" or "0". Resistors, diodes, and capacitors are assumed to have two failure modes. Transistors are assumed to have four failure modes, two at the emitter junction and two at the collector junction. It must be remembered that only one component is considered to fail in one mode (open or short) at any assumed failure. Both the short and open modes are considered for each component failure.

To define an open or short may be difficult. For example, a resistor may open completely (leads, element, etc.) or it may drift to a high value. Regardless of the type of open, the output will be at some signal state. It is then necessary to determine if the signal state meets the requirements for a logical "1" or "0". For the simplicity of the analysis and for the worst-case, the components are assumed to be open or shorted catastrophically instead of excessive drifts, leakages, parameter changes, etc.

After a component has been failed the following questions are answered:

- Does the input fail to a particular state?
- If so, what are the effects on the preceding circuits?
- Is there a chain-reaction (other component failures) involved?
- If the circuit is redundant, is the circuit function performed properly (proves validity of redundant scheme)?
- Does the output fail to a particular state?
- If so, what effects occur at the succeeding circuitry?
- Is the power supply(s) protected from any single component failure?

When circuit failure modes are determined for analog circuits, the same procedure that is applied to digital circuits is used, with the exception of input and output signals. These failure effects, at the input and output due to a single component failure, are described at their worst-case situation.

The importance of circuit failure mode analysis for a redundant system is to insure that the redundancy technique used is valid for any single component failure.

Table 3 is an example of a chart to be used in failure mode analysis.

Table 3

FAILURE MODE ANALYSIS

Circuit Failure Mode (Worst-Case)					
Component	Mode	Output	Input	Power Supply Affected?	Comment
R1	Open	Not Affected	Not Affected	No	
	Short	Fails to "0"	Not Affected	Yes	Will Fail Q2 Emitter Junction open

Failure mechanisms may be classified as either time dependent or threshold dependent[2].

Threshold failures and time dependent failures are almost self-explanatory. The threshold failure occurs almost instantaneously when a threshold rating is exceeded, however, a time dependent failure is a

function of time and the stress level. Examples of threshold type failures may include semi-conductor junction breakdown where there is no current limiting, exceeding a capacitor's breakdown voltage, and fractured component leads, crystal, elements. Time dependent failures may include resistor drift, semiconductor contamination, and component lead or element oxidation or corrosion.

Noise Rejection

Noise induced into a circuit may be amplified, switch the output state, propagated, or may even diminish. It is the reviewer's responsibility to determine the amount of noise a circuit will tolerate.

Many consider noise as energy which is a very accurate means, but it is also very difficult to describe the conditions that must exist. A different method, which is most commonly used, assumes noise to represent some D.C. voltage that would cause the circuit to fail, (switch state, when it shouldn't). For example, consider Figure 6.

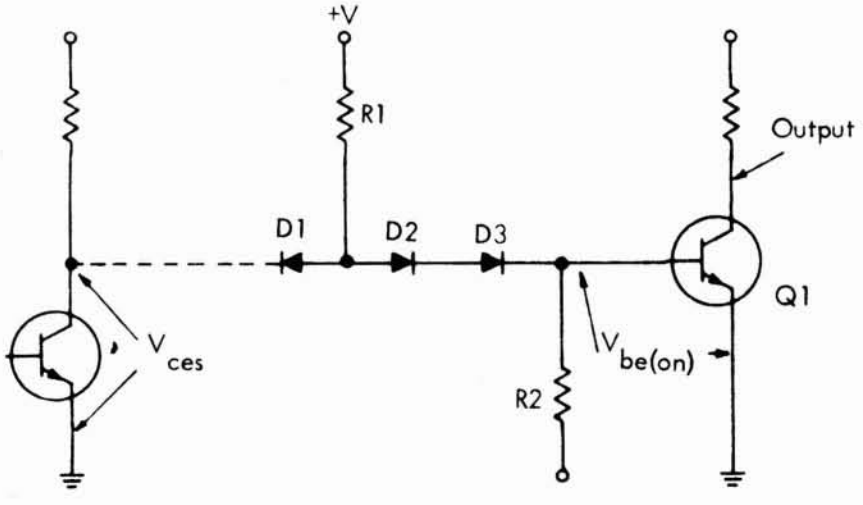

Figure 6. Noise Rejection Condition

Normally, $V_{CES} + V_{D1} < V_{D2} + V_{D3} + V_{be(ON)}$

This says, the input to D1 is at a down level or logical "0" and the inverter output would be at a logical "1", since Q_1 is "OFF".

The question to be asked, is what noise or D.C. voltage on, or in series with the input will cause the output to switch to a zero?

First consider the worst-case condition of the normal case.

$$V_{CES(max)} + V_{D1(max)} < V_{D2(min)} + V_{D3(min)} + V_{be(on)min}$$

Therefore,

$$V_{Noise} \geq V_{D2(min)} + V_{D3(min)} + V_{be(on)} - V_{CES(max)} + V_{D1(max)}$$

This is the worst-case allowable noise.

Note that $V_{D(min)}$ will occur at the maximum temperature whereas $V_{CES(max)}$ or $V_{D(max)}$ will occur at a minimum temperature. Considering the design temperature range, one should choose a realistic temperature difference between any two components in the system.

The example above was given for a down level noise rejection case. There is also an "up" level noise rejection which should also be calculated. Usually one will find that the worst-case noise margin will occur at the down level condition with the circuit of interest at its maximum temperature and the driving circuit at a minimum temperature.

The noise rejection capabilities of a circuit become important when the driving logic circuit is placed some distance from its load. If multilayer printed circuit boards are used, a careful layout of the signal lines must be considered to prevent switching signals in a line from being coupled, or induced into an adjacent line.

Circuits, such as capacitive input or capacitance coupled and low level circuits may be very susceptible to noise. Circuits with capacitive inputs should be avoided. This circuit category may include single-shots and amplifiers.

Component Temperatures

All of the designer's component parameter values, or ratings, the component failure rates, and mechanical engineers packaging and environmental design, must contend with the one big variable--HEAT.

The circuit designer must create a design which performs a function for a given temperature range. The mechanical engineer must assure that all system temperature requirements are satisfied. The failure analyst must know if the component has exceeded its thermal capacity in the particular manner it was used or stressed. The reliability analyst must know the design temperature range, component ratings, degree of cooling, and probable failure modes due to temperature. These items are needed to assure that the total design is in agreement with the failure rates used to predict the system reliability.

When power is dissipated in components, the heat generated (source) will be transferred to a cooling medium (sink). The fewer obstacles or heat resistance paths there are, the better the source heat will be absorbed by the sink. Since conductive cooling is used for most space systems, many thermal resistances are usually encountered. If, for example, the transistor junction temperature in Figure 7 were needed, the first step would involve drawing the thermal equivalent shown in Figure 8. Since the mechanical thermal equivalent of Figure 8 may not appeal to the circuit reviewer, an electrical analogy may be used.

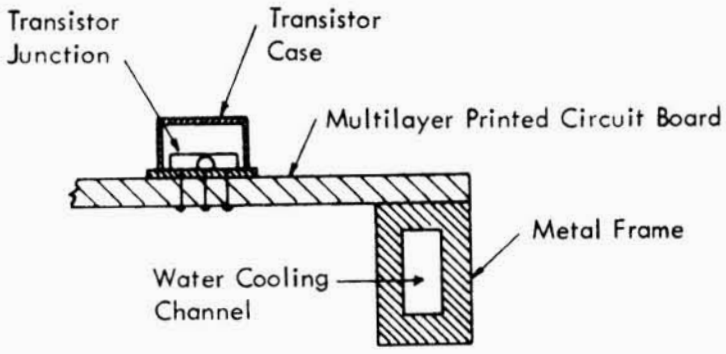

Figure 7. Typical Space System Heat Transfer Condition

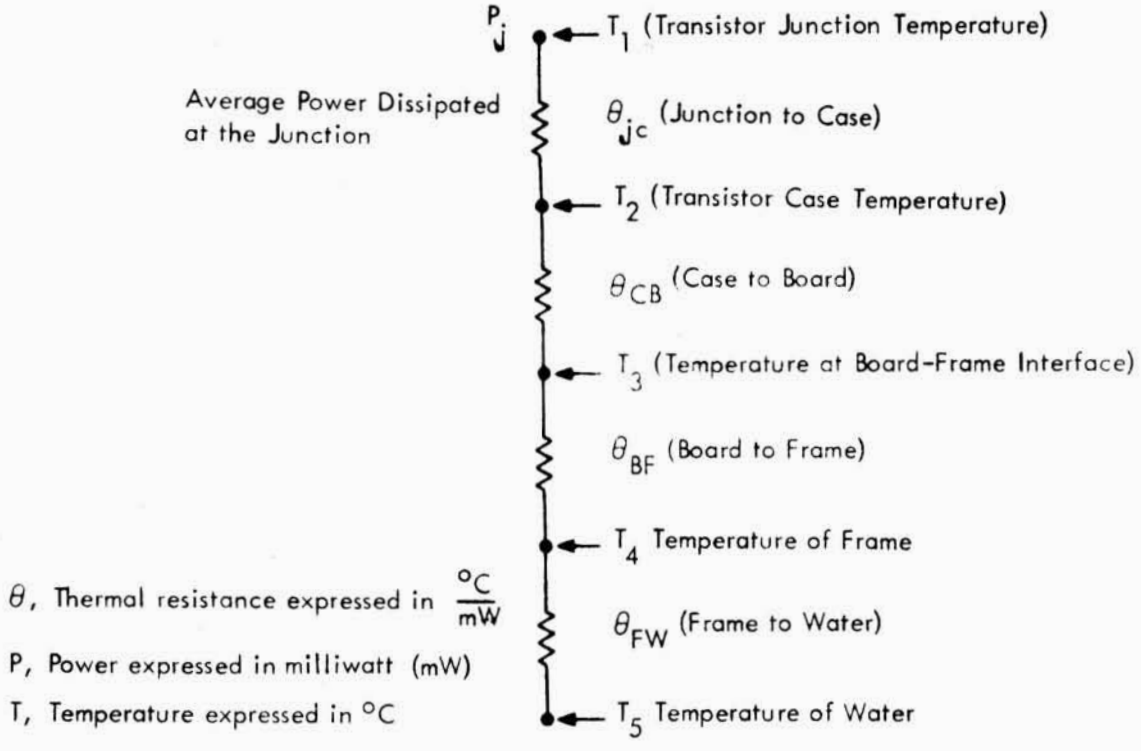

Figure 8. Thermal Equivalent

Power, temperature, and thermal resistance in heat transfer are analagous to current, voltage, and resistance, respectively, in an electrical system.

Therefore, if the junction temperature were needed:

$$T_j = P_j (\theta_{jc} + \theta_{CB} + \theta_{BF} + \theta_{FW}) + T5$$

Calculations for junction or component case temperatures in an encapsulated cordwood module become more difficult. The difficulty results from the fact that the dissipation of one component will have an effect on another component. Therefore, to find a junction temperature packaged in a cordwood type module, the total module power must be considered for determining the particular transistor's case temperature. Once the case temperature is known, one can directly calculate the junction temperature by knowing the transistor's power dissipation and the thermal resistance from the junction to the case.

In Figure 9, the derating curve means that if one has a transistor whose case temperature is held at 25°C, and that if 1000 mw were dissipated, the junction temperature would be at 150°C. Before determining if a component is applied properly thermally, one must know the maximum design junction temperature, the maximum temperature required by Reliability, and the expected mounting surface temperature (T_E).

The derating slope is the thermal resistance from junction to case (θ_{jC}). The following examples refer to space system applications where conductive cooling is inferred.

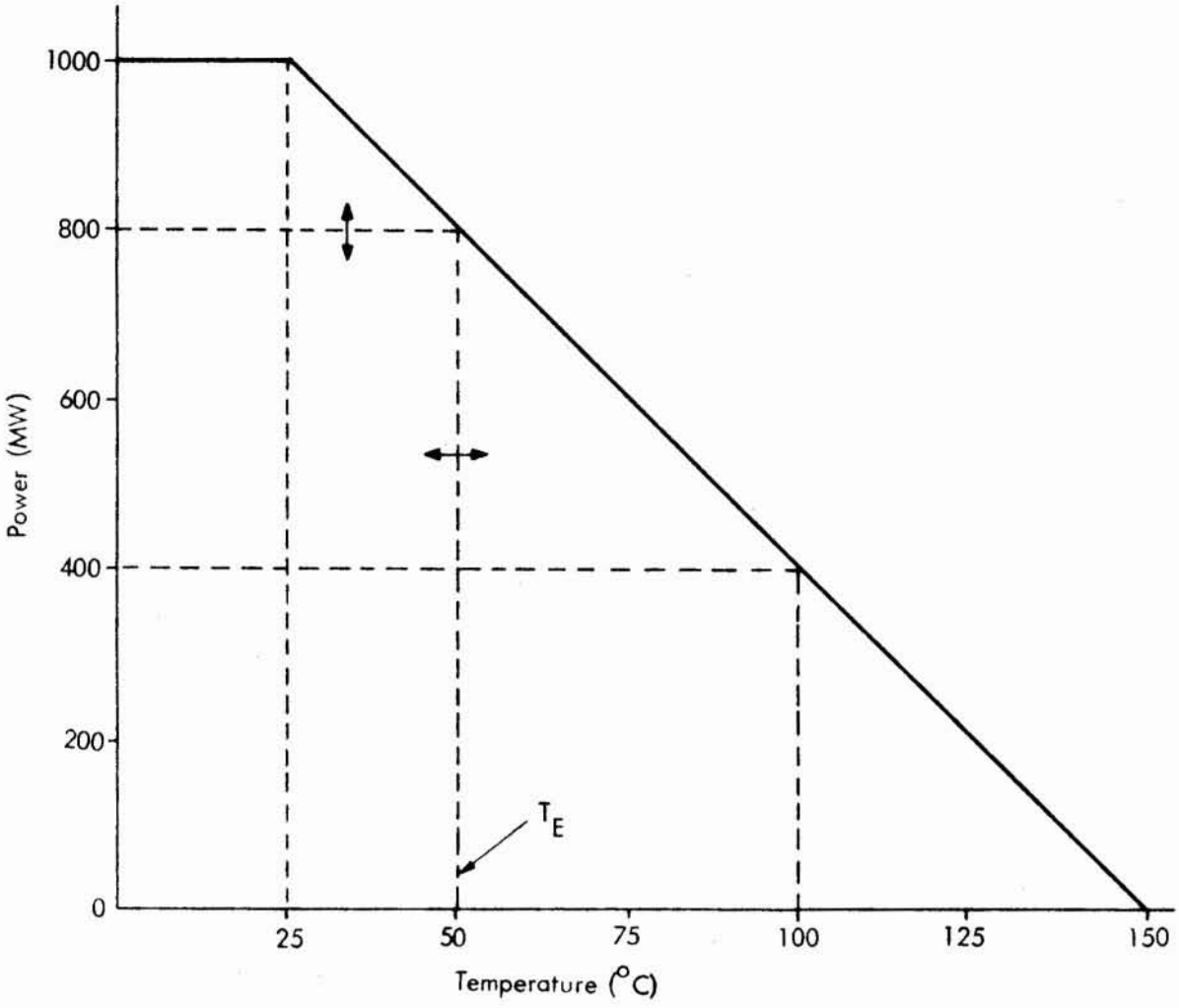

Figure 9. Typical Derating Curve

Example 1.

Let: The maximum design junction temperature be 100 °C.
The environmental temperature (T_E) be 25 °C

then, What is the maximum power that may be dissipated to assure that the junction temperature does not exceed the worst-case design temperature?

$$\theta_{jC} = \frac{\Delta T}{\Delta P} = \frac{(150 - 25)^{\circ}C}{1000\ mw} = 0.125\ \frac{C}{mw}$$

$$\therefore P_{max} = \frac{\Delta T}{jC} = \frac{(100 - 25)}{0.125} = 600\ mw$$

Example 2.

Let: The maximum design junction temperature be 100°C.
The environmental temperature, T_E, be 50°C.

then, What is the maximum power that may be dissipated to assure that the junction temperature does not exceed the worst-case design temperature.

θ jC is the same as in example 1.

$$P_{max} = \theta_{jC}\ \Delta T = \frac{(100 - 50)}{0.125} = 400\ mw$$

The most common example used for design review is shown in Example 3.

Example 3.

Let: The maximum design temperature be 100°C.
The environmental temperature be 75°C.
The power that is dissipated be 300 mw.

What is the junction temperature?

$$T_{max} = T_E + (P)(\theta_{jC})$$

$$T_{max} = 75\ C + (300)(0.125) = 75 + 37.5 = 112.5^{\circ}C$$

This example shows that a component would be improperly applied. Note that it has not exceeded its absolute junction temperature (150°C) but it has exceeded that temperature for which all parameters were

taken for the design (100°C). Therefore, the worst-case design would not be valid.

Peak power and duty cycle play an important part in justifying proper component application. Usually, the most troublesome circuit is the emitter follower. The emitter follower is a driver with good response time that is used to drive long lines or large loads. Large capacitive loads associated with the lines or leads may damage the device. For example, when the emitter follower begins to turn on there is a large collector to emitter voltage and a very high load current (charging of the line capacitance). Even though the average power may be much below its derated value, the device could be easily destroyed due to excessive dissipation during the peak power or due to excessive current.[3] Figure 10 shows the current of a typical emitter follower. A useful expression for determining junction temperature rise is:

$$\Delta T_i = \frac{P_c t}{C_j} \qquad \text{valid for } t \leq 0.2\ \theta_t$$

where

ΔT_i = increase in junction temperature

P_c = collector peak power

t = transient time

C_j = junction thermal capacity

C_j is expressed as $\frac{\theta t}{\theta r}$

where

θ_t = the thermal time constant

θ_r = the thermal resistance

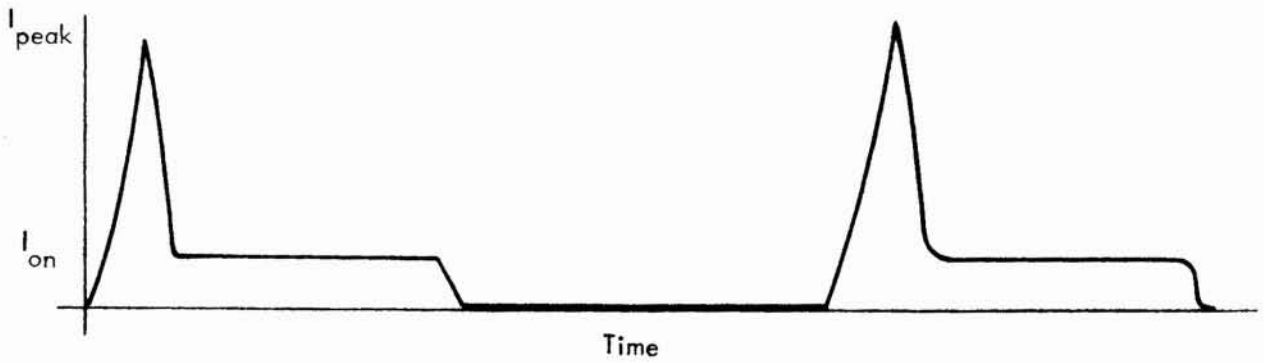

Figure 10. Emitter Follower Current Characteristics

The thermal time constant and thermal resistance may either be measured or they may be specified on the component manufacturer's specification sheet.

For example, let θ_t be 1 millisecond, θ_r be 125 °C/watt, t = 120 microseconds, and P_c be 4 watts.

$$\text{then } \Delta T_i = \frac{P_c t}{\frac{\theta_t}{\theta_r}} = \frac{(4\,\text{watts})\,(0.12\,\text{ms})}{\frac{1\,\text{ms}}{125\,^{\circ}\text{C/watt}}} = 60\,^{\circ}\text{C}$$

This says, due to the specific transient, the junction experienced a change of 60 °C above what it was initially. This may or may not destroy the device depending on what the initial temperature was. It may also exceed the maximum circuit design junction temperature. It is the reviewer's responsibility to decide these cases but they do happen and are often not found until failures occur.

Reduce Probability of System Failure

Each circuit should be reviewed with a creative approach. Question the design to see whether it can be simplified, repackaged, or even eliminated. This can be done on the component, circuit, or function (i. e. digital and analog converter) levels. For example, power supply filter capacitors may be eliminated where they are not needed and conversely they may be needed where they do not exist. Check any common item like the power supplies to assure that they will suppress transients and maintain regulation. Carefully examine all input and output circuits that will be driving other sub-systems. They must "fail safe" and must be designed against humanly induced failures. Eliminate, or design against (such as redundancy), failure modes that will cause chain-reaction types of failures. Assure compatibility among circuits.

The above are just a few items which reduce the probability of system failure. These should be done as early as possible so that the changes can be made with the minimum cost involved.

Items Found During A Circuit Design Review

The following analyzes a list of items found during two design review periods. The first review period is during the pre-release or early design phase. Some items that were found during this brief review are listed below in their order of occurrence.

- Overstressed Components – This usually occurred because good derating practices were not followed. The correction for this problem resulted in specifying a higher-rated component.
- Inputs and Outputs That Were Not Compatible With Intended Compatible Circuitry – The correction for this problem would include minor design changes, a change in specifications, or re-defined loads.

- High-Component Temperatures – During the early review, thermal analysis data is usually not available. However, by knowing the power dissipation, the hot-spot temperature may be approximated. The corrections for this problem resulted in specifying heat sinks or different components.

- Complex Circuits to Perform the Function – The correction may be a newly designed circuit with fewer components or the same circuit with the unnecessary components removed.

Some items found after the initial circuit was released are listed below. These items are more difficult to find and require a thorough review.

- Exceeded Ratings – This item is found during the worst-case analysis. It is usually the result of exceeding the recommended deratings and may be corrected by specifying a higher rating.

- Semiconductor Junction Temperatures – This item is found from a combination of the circuit analysis and the heat transfer conditions. The condition may be due to transient conditions, packaging, unexpected loading, etc.

- Non-"Fail Safe" Components -- This item is of particular importance in redundant designs. If it was found that a component failure would fail the redundant circuit, the simplest correction would be to choose the component type that would have a very slight, if any, chance of failing the circuit. For example, if a shorted resistor would fail the circuit, choose a resistor type which, when failed, has a history of failing open.

- Poor Packaging Methods – Correcting items in this category would reduce the number of connections, avoid crossing high current lines, and decrease the chance for material "out-gassing" which could harm the components.

- System Interface Problems – This type of problem is usually not discovered until the breadboard model has been built. Until that time, the review should concentrate on the system's input and output circuits. For example, output circuits were prone to human induced failures. A change was recommended, but refused since the customer wanted the original circuit for drive capabilities. Therefore, another recommendation was made to inform all testing personnel of the problem. This aided in reducing humanly induced failures during testing and avoided rework of the sub-assemblies.

Conclusions

It has been found from past design reviews that most circuits reviewed were designed satisfactorily. It is the remaining few that cause trouble and must be found before any systems is "go".

The circuits least likely to be troublesome are the circuits, or similar types, that have been designed before and have proven themselves. Conversely, the designs that are the most troublesome are the completely new designs, the complex designs, and the designs in which new components are introduced (i.e., glass delay lines, FETS, etc.). If the reviewer will concentrate on the latter case, many errors and possible trouble areas will be eliminated at the beginning.

The review should be accomplished independent of the design group to provide a truly unbiased opinion.

References

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